[White Paper]

ACVS

: Advanced Channel Verification System

Simulation NextX

Huwin

JANUARY 2025

Revision History

Ver.	Date	Author	Modification Details
1.0	2024.1.26	Charlie Jeung (CEO/Huwin)	- Initial version
1.1	2025.1.22	Ethan Cho (CTO/Huwin), Charlie Jeung (CEO/Huwin)	- 2025 update

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1. Introduction

The ACVS (Advanced Channel Verification System) was initially developed as a package (PKG) S-parameter model verification system for the leading memory chip companies in South Korea. The initial system was delivered in 2017 and has been continuously upgraded ever since. It is now being used as a sign-off system to verify frequency and time domain parameters for all newly designed PKG models.

Huwin has been continuously expanding its frequency and time domain analysis engine based PKG verification system to an automated channel verification system and commercializing it as ACVS (Advanced Channel Verification System). Notably, from 2020, it has been utilized for the verification of PKG/PCB design with NPU and Memory chip interconnections in the latest ultra-high-performance AI chips. Through our channel verification system, successful operation of new AI chips (from 14 different South Korean AI fabless companies) was possible, even with their first fab-out versions.

Huwin was founded in 2010 by Charlie Jeung (CEO, sijeung@huwin.com) as an engineering company specializing in ANSYS EM analysis. From then, Huwin established the ACVS R&D team and has been developing ACVS for 14 years to automate EM analysis and channel verification processes.

The ACVS R&D team is being led by Ethan Cho (CTO, jycho@huwin.com). His doctoral research was in frequency and time domain solver (Freq. and Transient Solver) at KAIST. He and his team are actively focused in improving the frequency and time domain solver in ACVS.

Since 2019, Brian Lee (CMO, brian.lee@huwin.com) has been focused in promoting ACVS to various global PKG, fabless, and system development companies at major conferences such as DesignCon. He plays a role in delivering customized solutions to meet the specific requirements requested from customers.

Huwin is continuously collaborating with customers to make ACVS become the common standardized solution for verifying state-of-the-art channels in the industry.

Huwin also provides a free web-based S-parameter Channel Model simulation environment (snpview.com), which provides fast and accurate analysis and verification of S-parameter models at high-speeds.

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2. ACVS

Contents:

2.1. What's ACVS

ACVS (Advanced Channel Verification System) is an automated analysis and verification solution system for the latest memory and high-speed Serdes channels.

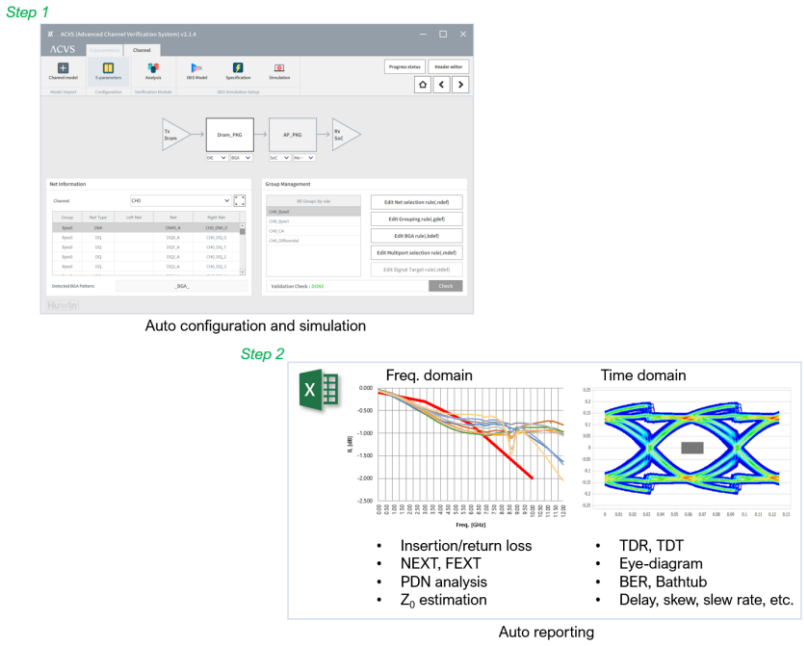


Figure 1. ACVS: Auto. Ch. configuration/simulation and reporting

ACVS is also being developed as a specialized SI/PI simulator for chiplet interface verification through the government-funded project: 'Development of High-Performance AI Chiplet Semiconductor with Heterogeneous integration technology'

2.2. Why ACVS

Recently, the demand for AI-based semiconductors in applications such as ChatGPT and autonomous driving has skyrocketed. Such semiconductors require high speed advanced Ch. Interface designs that can transmit high bandwidth/high speed data, which mandates the need for signal integrity.

To ensure successful high-performance chip-to-chip data transmission, it is essential to identify any signal integrity issues in chiplet-based designs, SiP (System in Package) designs, or in the PKG and PCB (Printed Circuit Board) designs. To obtain full analysis and verification reports efficiently, ACVS (Advanced Chip Verification Solution) has been developed.

The general signal integrity analysis procedure for high-speed digital channels is shown in Figure 2. In the design of high-performance AI semiconductor chiplet packages, which has high speed and high-density interfaces, the accurate signal integrity process is necessary to meet the electrical channel specifications.

In the first step, S-parameters model for the selected analysis nets are extracted by using the EM simulation. S-parameters model represents the electrical characteristics of each net such as frequency domain response and can be used as input for various SI/PI (Signal Integrity/Power Integrity) analyses. The EM simulation can be performed using simulators like Ansys SIwave or HFSS. In the EM simulation, port setup and frequency sweep setup for each analysis net are performed and can easily be automated through ACVS.

In the next step, channel results are retrieved by configuring the Channel System Simulation. In this procedure, the ACVS can be utilized, and can perform Basic and Advanced SI analysis separately.

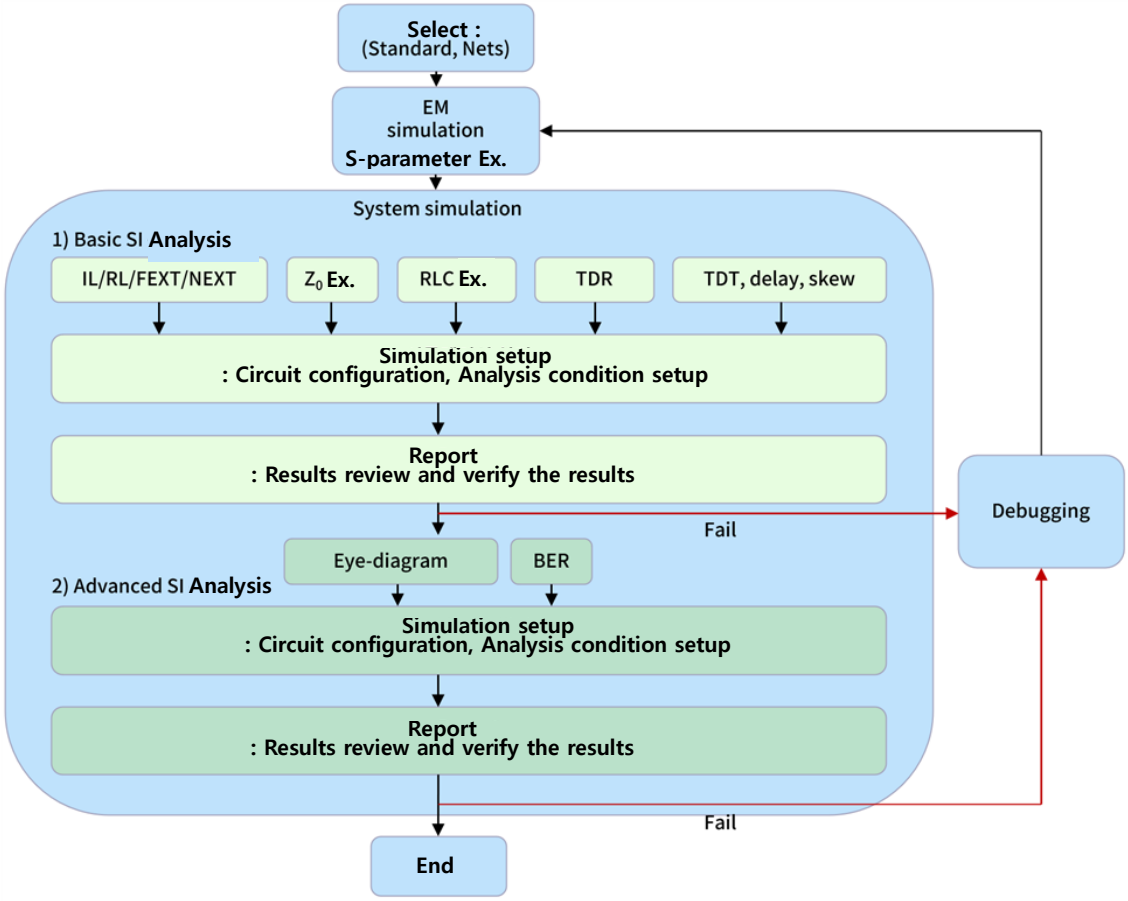


Figure 2. Procedures for high-speed digital channel general Signal Integrity analysis

The ACVS Basic SI Analysis is the procedure for verifying all essential Signal Integrity performance parameters in the high-speed channel system design. This includes Insertion loss/Return loss/FEXT/NEXT, extraction of characteristic impedance, equivalent RLC extraction, TDR (Time-domain reflectometer), TDT (Time-domain transmission), as well as checking delay and skew. Due to the variety of analysis items in this procedure, the traditional method of circuit configuration, simulation setup, and result measurement requires significant effort and time. However, ACVS will automate all these processes, as well as generate result measurements, all within an hour. If the channel's performance is verified in the Basic SI analysis, debugging or Advanced SI analysis can be performed, depending on the results.

The ACVS Advanced SI Analysis includes results such as Eye-diagram and BER. It involves applying the IBIS-AMI model of the chip to the channel system, which constructs an environment that mimics the actual operation of the chip. This allows analyzing the output waveforms in the time domain. The analysis process is complex, especially in terms of simulation settings for each Net (such as Tx/Rx driver and EQ settings) and requires a long simulation time. For instance, in the case of PCIe Gen5, the adaptation for EQ requires an input PRBS of 2,000,000 bits per Net (requires time for ignore bits for EQ).

The procedure for Power Integrity analysis is similar to that of Signal Integrity analysis. Key analysis items include Impedance analysis, which involves the extraction of DC resistance (DC_R) and AC inductance (AC_L), as well as the measurement of |Z11|.

As previously mentioned, the SI/PI (Signal Integrity/Power Integrity) analysis of high-performance AI semiconductor chiplet packages requires consideration in various aspects due to the need for analysis of ultra-high-speed and high-density channels. This necessitates a balanced consideration of simulation accuracy, time, and complexity in the system analysis. In the case of high-density channels, the complexity of simulation increases due to the large number of Nets, which entails intricate circuit configurations, analysis settings, chart outputs, result measurements, and Pass/Fail judgments. Additionally, the ultra-high-speed nature means that the analysis frequency band is high, which can lead to reduced simulation accuracy and increased analysis time. Therefore, as shown in Figure 3, consideration of Simulation Integrity, which addresses issues related to simulation accuracy, time, and complexity, is essential. ACVS is an optimized solution that takes these factors into account.

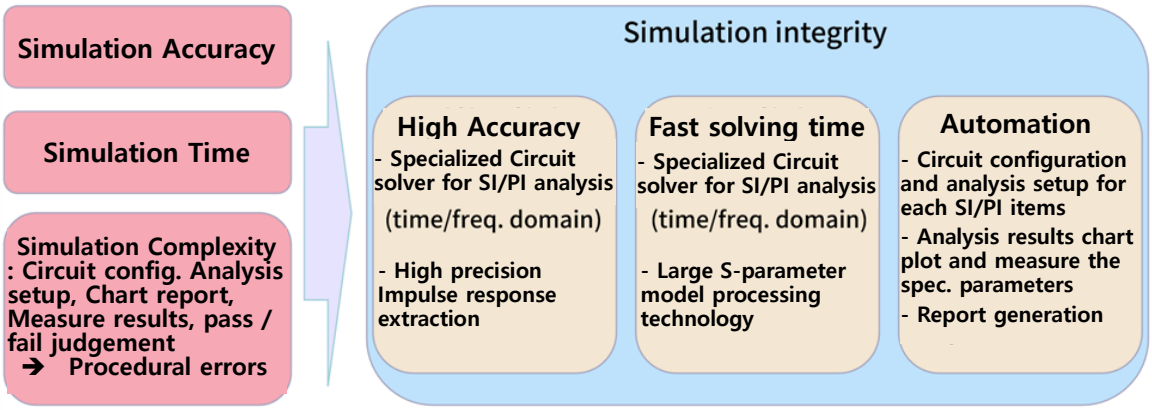


Figure 3. The Importance of Simulation Integrity for Improving Accuracy and Efficiency in SI/PI Analysis

To enhance simulation accuracy, a Circuit Solver specialized for SI/PI (Signal Integrity/Power Integrity) analysis of ultra-high-speed channels is necessary. However, most commercial solutions are developed to cover a wide range of applications (RF, power electronics, analog, digital, etc.), which may limit their accuracy in SI/PI analysis. For example, the Vector fitting technique, initially applied in power electronics, is used to convert S-parameters into equivalent circuits or time responses and is also utilized in the SI/PI field. This technique's accuracy can be affected by S-parameter conditions (frequency range, measurement and extraction environment, etc.). Moreover, the S-parameters for ultra-high-speed, high-density channels often have a wide frequency range and numerous parameter items, leading to significant file size reaching several tens of gigabytes. In such cases, the computational speed significantly deteriorates in the general Circuit Solvers described earlier.

Additionally, conducting various analysis items for high-density channel requires significant effort and time. During this process, frequent procedural errors can occur, leading to deterioration in the reliability of the analysis results. Consequently, some companies are developing their own in-house tools to mitigate the complexity of SI/PI (Signal Integrity/Power Integrity) analysis. However, most of these solutions automate existing Circuit Solvers and thus do not resolve the inherent issues of accuracy and computational time. Table 1. compares the characteristics of general Circuit Simulators and dedicated SI/PI analysis solutions. The trend towards specialized SI/PI analysis solutions is becoming more common, and in South Korea, HUWIN is offering its ACVS (Advanced Channel Verification System) solution. This system provides dedicated SI/PI analysis solutions and technical support to major semiconductor and design house companies (memory/non-memory/AI chips, etc.).

Talbe 1. Comparison of Simulation Integrity Across Different Solutions

Solution Type	Simulation Accuracy	Simulation Time	Simulation Complexity
Previous General Circuit Simulator	Developed as a Solver to all application areas, it lacks computational performance for the specific SI/PI analysis.	It has weaknesses in handling large-size S-parameters and particularly low computational efficiency in Transient and AMI simulations.	Circuit configuration, analysis settings, chart output, and measurements all need to be performed manually by the user, leading to high complexity and a high likelihood of procedural errors.
Specialized SI/PI analysis Solution: ACVS	Using a Solver developed specifically for SI/PI analysis can maximize computational accuracy.	Capable of maximizing computational efficiency in handling large-size S-parameters and IBIS-AMI simulations.	Automates the entire analysis process, resulting in lower complexity and the ability to suppress errors in the analysis procedure.

Huwin's ACVS can be tailored as a customized solution for channel verification. This means it can be utilized as a standardized sign-off verification tool at various stages of design verification, aligning with the design flow and analysis methodologies of the client. It is applicable in interconnection designs such as PKG/PCB or Silicon interposer.

2.2.1. Advanced high speed Channel Technical Issues

Chiplet technology, unlike the monolithic process, features the combination of function-specific Dies manufactured using heterogeneous processes into a single package. Figure 4 is an example of TSMC's 3D packaging CoWoS (Chip on Wafer on Substrate) technology. In this example, the SoC (System on Chip) Die and HBM (High Bandwidth Memory) Die are configured together on a single package. This configuration employs technologies such as RDL (Redistribution Layer), Silicon Bridge, and Interposer.

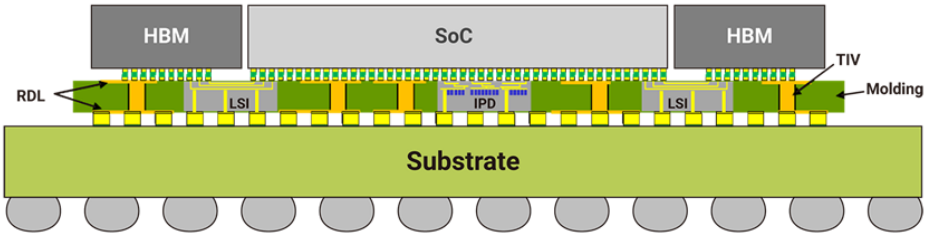


Figure 4. Chiplet Packaging Technology (CoWoS) [1]

Figure 5 represents the configuration of AMD's AI semiconductor model, MI300. This model is composed of a combination of GPU, CPU, and HBM3 (High Bandwidth Memory 3). To meet the high-performance data processing and computation requirements of AI semiconductors, high-performance memory is crucial. In this case, HBM3 with a transmission speed of 6 Gbps is employed. The HBM3 connection utilizes Interposer technology, highlighting the significance of Signal Integrity analysis to ensure performance in ultra-high-speed and high-density interfaces.

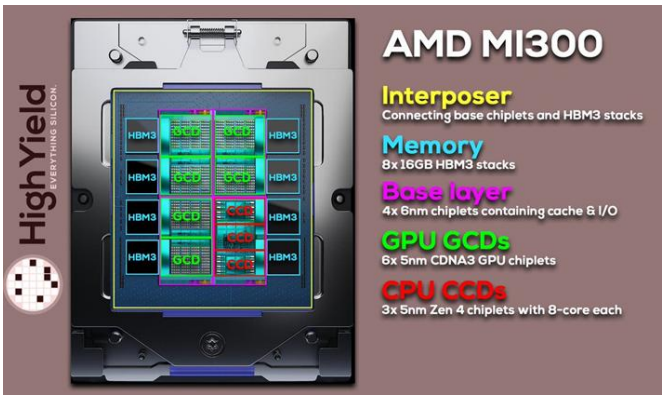
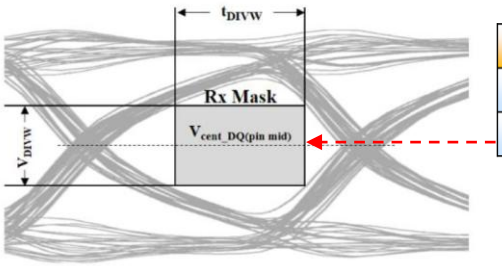


Figure 5. Structure of AMD's new AI chip MI300 [2]

As in the case mentioned earlier, some of the key design specifications used for interfaces between recent high-performance chips include HBM3(E), (LP)DDR5(x), GDDR6, PCIe Gen5,6, UCIe, and each of these technologies has its own significant features as described below.

2.2.1.1. HBM3(E)

HBM3(E) is designed to meet the requirements of high-performance AI chips by offering high-speed bandwidth and low-power operation. It is configured with a DDR 64-bit data bus and can support up to a maximum of 16 channels. The DQ speeds range from 4.8 Gbps to 6.4 Gbps, and for HBM3E, it can go up to 8 Gbps. The DQ Rx Mask voltage is set at 120mV. These specifications contribute to HBM3(E)'s capability to handle the data-intensive demands of AI chips efficiently.



	4.8 Gbps	5.2 Gbps	5.6 Gbps	6 Gbps	6.4 Gbps
V_{DIVW}	120 mV	120 mV	120 mV	120 mV	120 mV
t_{DIVW}	0.3 UI	0.3 UI	0.3 UI	0.3 UI	0.3 UI

- V_{cent} estimation technique applied
- Rectangular mask shape
- CA: DDR operation, 1/2 clock speed of Byte

Figure 6. HBM3, DQ Receiver Eye Mask [3]

HBM3 traces face challenges such as increased resistance in the current path due to smaller size and narrower spacing, as well as signal interference and return path design issues caused by increased coupling. Therefore, in HBM3 analysis, it is essential to verify the entire channel nets, including transient waveform analysis. This comprehensive analysis is crucial for addressing these issues and ensuring the integrity of HBM3 signals. Figure 7 illustrates the challenges associated with HBM3 traces in terms of signal integrity and return path design.

Additionally, the Receiver's buffer, as shown in Figure 8, follows an open model (capacitive load). This can potentially lead to issues during transient simulations, such as solver divergence due to impedance mismatches between Tx, channel models, and Rx, as well as a decrease in analysis speed. These challenges need to be carefully addressed to ensure accurate and efficient simulations of the system.

ACVS has been developed to address the challenges associated with HBM3 analysis, including the use of large-size S-parameters that capture the characteristics of the entire HBM3 net. It can perform transient analysis that takes into account the entire crosstalk without encountering solver divergence issues or

computational speed degradation. This development ensures that ACVS can effectively analyze HBM3 systems, while maintaining accuracy and efficiency, even during complex simulations.

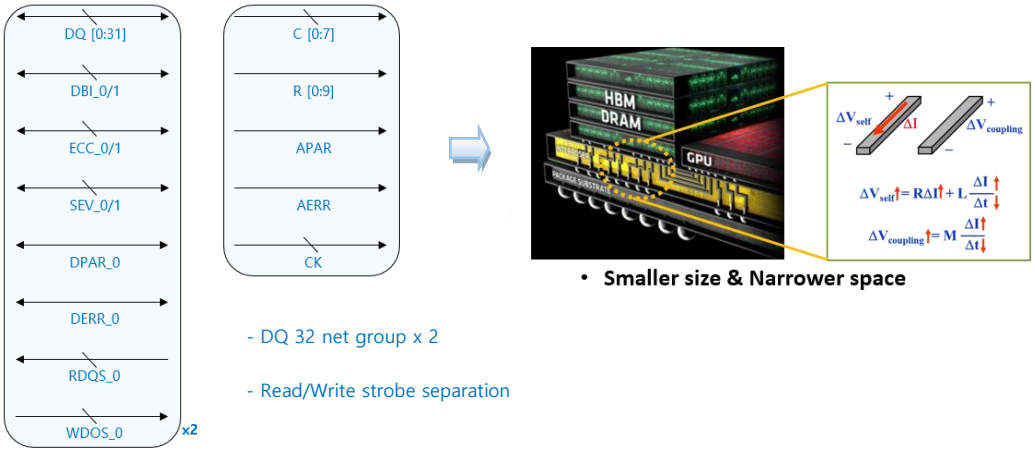


Figure 7. HBM3 standard Net configuration and Tech. issues

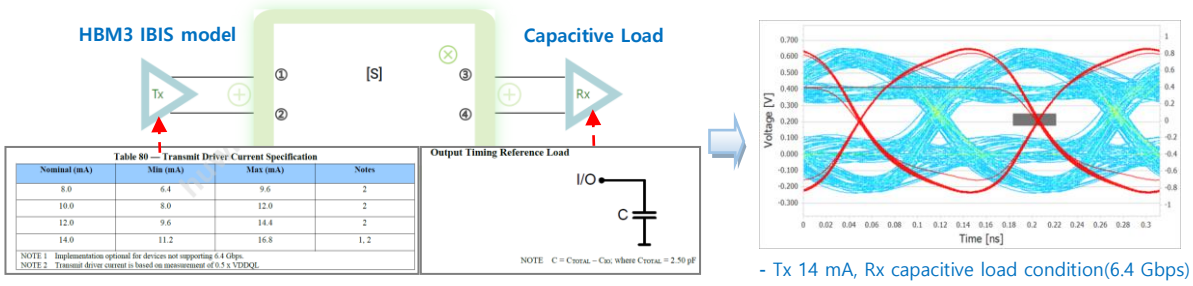


Figure 8. HBM3 analysis example (ACVS)

2.2.1.2. (LP)DDR5(x)

(LP)DDR5(x) has been designed with Tx and Rx models to accommodate the increase in signal speed and data capacity [4,5]. To perform system simulations using these models and reflect chip behavior accurately, specialized simulators tailored to the specific requirements of (LP)DDR5(x) are essential.

ACVS has been designed to simulate channels like DDR5 to mimic the behavior of real chips as shown in Figure 9. It achieves this by enabling analysis incorporating single-ended IBIS-AMI models and reflecting single-ended signal rising/falling edge responses. Furthermore, in analysis using AMI models, it ensures that all crosstalk within the entire net is accounted for. The DC offset resulting from chip Tx-Rx training is automatically calculated for each net, and the alignment of DQ-DGS through forward clocking is maintained, allowing for obtaining Eye results. Figure 10 illustrates the sequential operational steps involved in achieving these simulations.

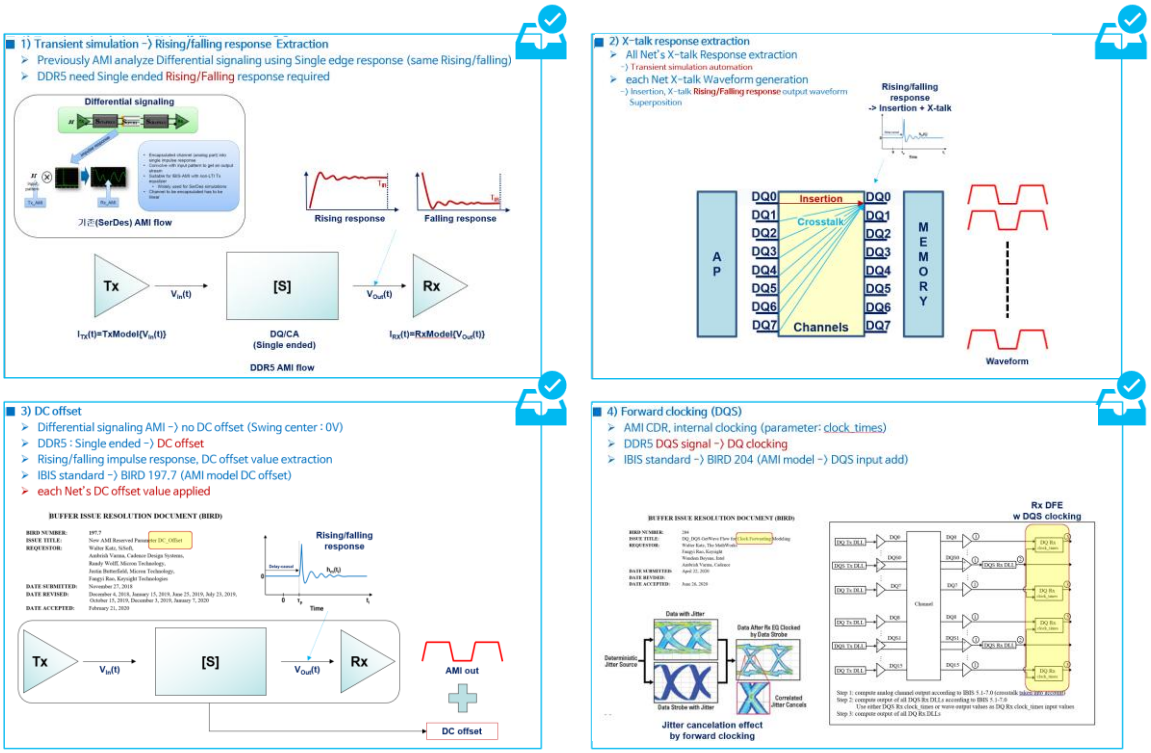


Figure 9. DDR5 analysis (ACVS)

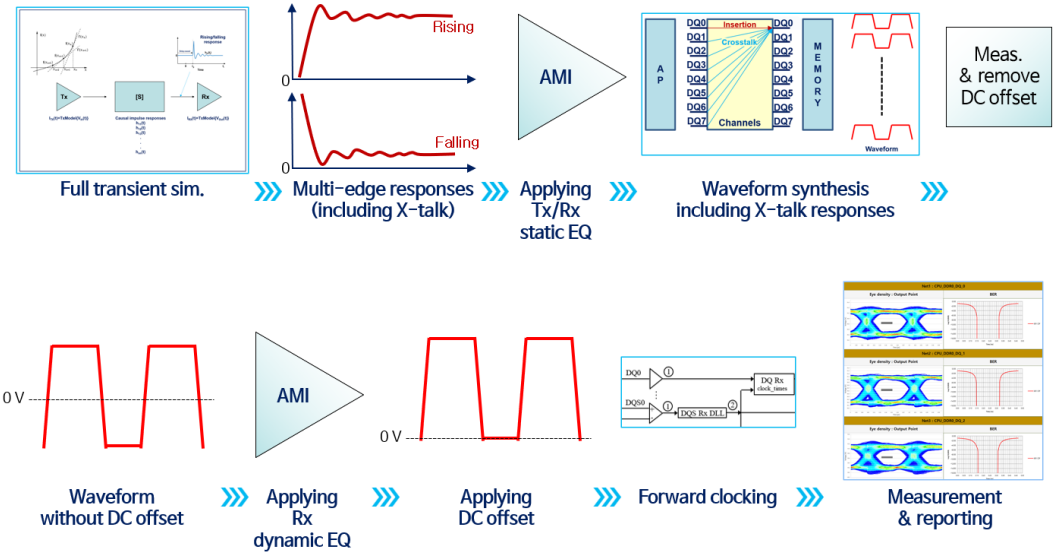


Figure 10. DDR5 analysis (ACVS)

2.2.1.3. GDDR6

GDDR6 is capable of high-speed operation (16 Gbps) and wide bandwidth with low power consumption, meeting the demands of high-performance AI chips. To achieve this, it utilizes components such as WCK (Write Clock) and EDC (Error Detection and Correction) signals, as illustrated in Figure 11. These elements play a crucial role in enabling the desired memory performance and power efficiency for AI chips.

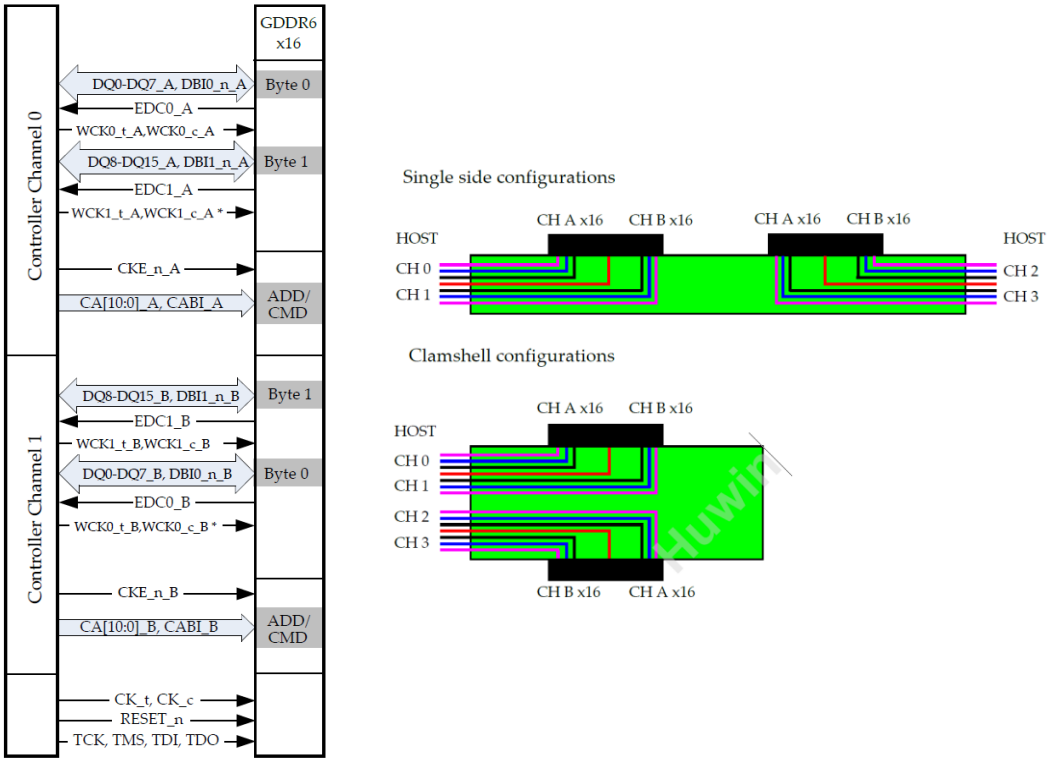


Figure 11. Example System view for x16 mode GDDR6 [6]

In the case of GDDR6, the design involves a very high-density channel due to the presence of numerous nets, especially in packages (PKG) and other components. Therefore, it becomes crucial to perform transient analysis that takes into account crosstalk across all channels between the Controller and Memory in the PKG and PCB designs. Additionally, there is a need for AMI analysis functionality to address Equalization (EQ) for high-speed signals. These capabilities are essential to ensure the integrity and performance of GDDR6 in high-performance AI chip designs.

ACVS facilitates GDDR6 analysis by automatically generating verification reports for SI aspects that may pose problems in the channel. It does this by considering Basic SI results for all channel nets and incorporating crosstalk into AMI EQ simulations, including Eye diagrams and Bit Error Rate (BER) analysis. This automated report generation streamlines the debugging process, enabling a faster and more efficient verification of potential SI issues within the channel.

2.2.1.4. PCIe Gen5,6

PCIe Gen5 specifies Serdes signal transmission at 32 GT/s (giga transfers per second). In 2022, the final specification for PCIe Gen6 was confirmed, featuring 64 GT/s and x16 lanes, allowing for a maximum transmission speed of 256 GB/s. PCIe Gen6 extends bandwidth by applying PAM4 signaling, doubling the bandwidth compared to Gen5. This advancement in PCIe technology offers significantly increased data transfer capabilities for high-performance computing and data-intensive applications.

2.2.1.5. UCIe

UCIe, which stands for Universal Chiplet Interconnect Express, is a specification designed for Multi-Die Advanced Package Modules, as shown in Figure 12. It features a Main band + Side band structure. For the Main band, verification of specifications such as Eye-diagram, VTF (Vertical Throughput Function) loss, and VTF cross-talk is necessary. This specification is crucial for designing Multi-Die Advanced Package Modules, as well as ensuring their performance and integrity.

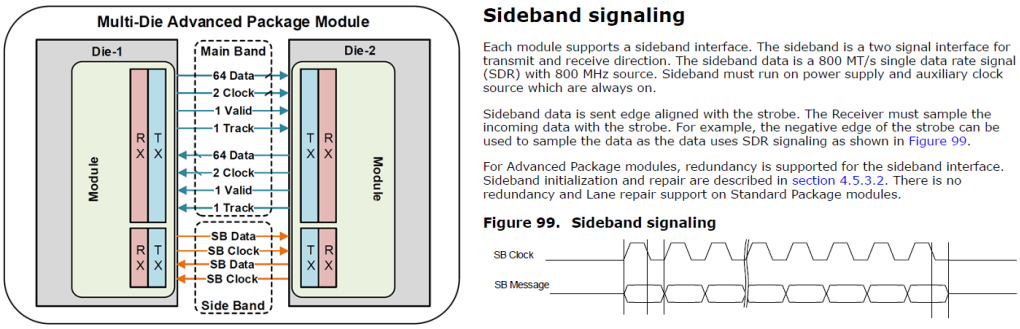


Figure 12. UCIe's PHY signal configuration and sideband signaling (800MT/s) [7]

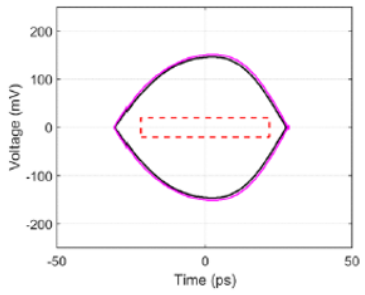


Table 37. Eye requirements

Data Rate (GT/s)	Eye Height (mV)	Eye width (UI)
4, 8, 12, 16[1]	40	0.75
24, 32[2,3]	40	0.65

1. Rectangular mask
2. With equalization enabled
3. Based on minimum Tx swing specification

Figure 13. UCIe Eye Mask specification [7]

For UCIe channel simulation, it's essential to have a Transient analysis module utilizing IBIS-AMI models. Additionally, a VTF analysis module is required to perform the necessary VTF analysis. These modules enable the comprehensive simulation and verification of UCIe channels, ensuring their functionality and performance.

Figure 84. Circuit for VTF calculation

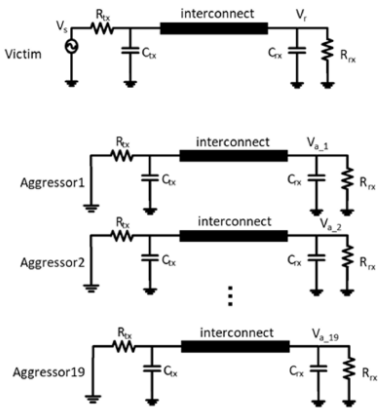


Figure 14. Frequency domain VTF simulation circuit

ACVS is capable of providing AMI analysis for UCIe and verifying Basic SI specifications, including VTF for all nets. This functionality ensures that the necessary analysis and verification reports are available for UCIe channels, enabling a comprehensive assessment of their performance and adherence to specifications.

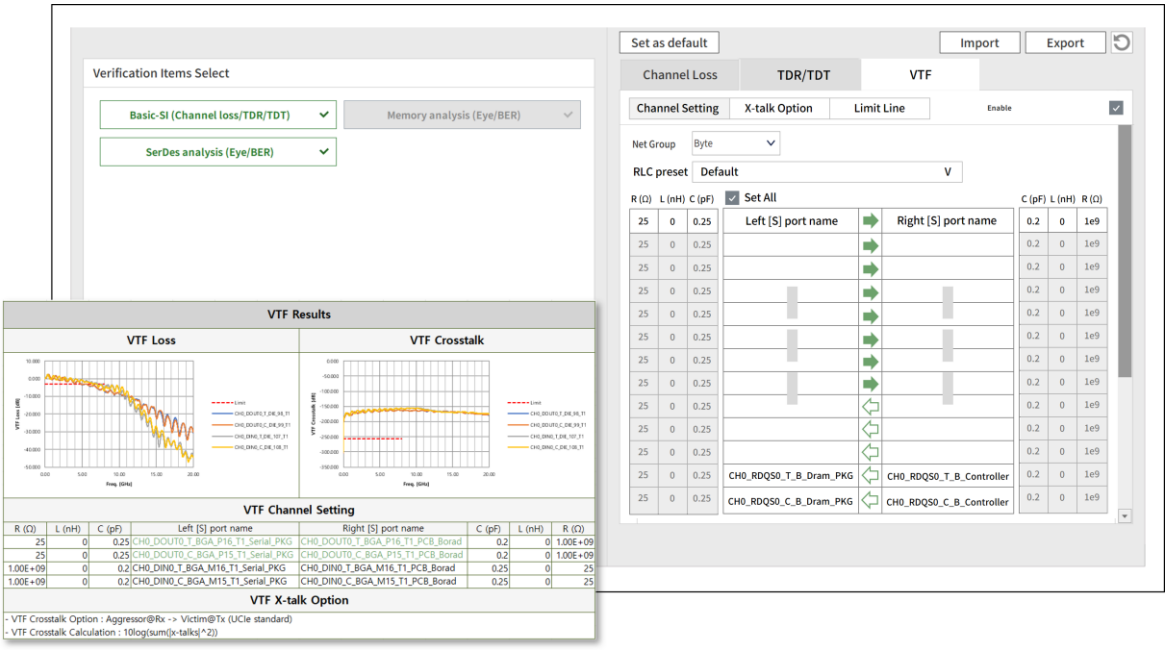


Figure 15. ACVS's UCIe VTF analysis module and report automation feature

Figure 15 shows the UI and analysis result report of the UCIe VTF analysis module implemented in ACVS. It supports automation of circuit configuration, analysis, and report generation for all specifications of UCIe 2.0 VTF. Additionally, an input voltage option has been added, enabling its use for general AC simulations as well.

Figure 16 illustrates the Open Chiplet Platform presented by the UCIe (Universal Chiplet Interconnect Express) consortium. As seen in the diagram, Core, Memory, and other functional block chiplet are combined within a single package. Notably, a new interface specification called UCIe is applied for Die to Die (inter-chiplet) connections. External chip-to-chip connections are established using serial communication standards like PCIe. The transmission speeds for UCIe and PCIe are 16 Gbps each, with PCIe Gen6 utilizing PAM4 modulation and achieving a speed of 64 GT/s. These high-speed interfaces enable efficient data transfer between chiplet and external components.

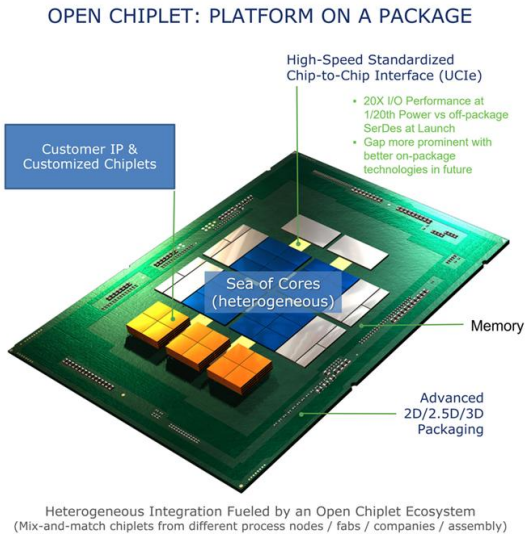


Figure 16. DIE-to-DIE UCIe (Universal Chiplet Interconnect Express) Open Chiplet Platform [8]

Indeed, leveraging chip package structures for the combination of heterogeneous dies offers advantages in cost reduction and yield improvement. However, this approach can introduce complexity to the package structure, requiring sophisticated interconnection designs and high-performance computational blocks for the operation of high-performance AI chips. Consequently, the complexity and time required for Signal/Power integrity analysis can increase as well. In such cases, specialized SI/PI analysis and verification solutions like ACVS become essential to address these challenges and ensure the integrity and performance of the chip package structure.

2.2.2. ACVS Solver (SimNX)

Figure 17. SimNX : Simulation Next X

SimNX, developed by Huwin, is a trademarked solution designed for the next generation of Advanced Channel Signal Integrity (SI) analysis. It is incorporated as an engine within ACVS and offers the following features:

- No File Size or Port Limitations: SimNX can handle channel S-parameter models with file sizes exceeding 40GB and over 1000 ports without any issues.
- Precise [S] to Causal Impulse Response Engine: SimNX utilizes the most precise engine for converting S-parameters to causal impulse responses.
- Accurate TDR/TDT Analysis Engine: It provides highly accurate Time-Domain Reflectometry (TDR) and Time-Domain Transmission (TDT) analysis capabilities.
- Ultra-Fast Full Transient Solver: SimNX includes an ultra-fast full transient solver that accounts for full crosstalk effects.
- Hawk-Eye: This feature allows the generation of Pseudo worst bit patterns based on channel characteristic analysis results.
- AMI Analysis: SimNX can analyze Bus channels (LP/DDR5,6, GDDR6, HBM3, etc.) and Serdes channels (PCIe Gen5,6, etc.) using the AMI (IBIS-AMI) modeling approach, reflecting full crosstalk from all nets.
- Efficient Transient Analysis Options: SimNX offers efficient Transient analysis options, including Fast, Optimal, and Strict modes.
- Versatile Tx/Rx Buffer Models: It supports the combination of various Tx/Rx buffer models, including Ideal, IBIS, and IBIS-AMI models.
- Automated AMI Analysis for All Channel Nets: SimNX can automate AMI analysis for all channel nets, ensuring that all crosstalk effects are considered.

SimNX incorporates the latest Non-iterative Extrapolation method, as shown in Figure 18. This method aims to maintain accuracy in both the low and high-frequency ranges, allowing for precise delay estimation and obtaining transient characteristics of impulse responses, particularly in the peak features. This research and development effort ensures that SimNX provides accurate and reliable results for channel S-parameter model analysis, even in challenging frequency ranges.

	Direct IFFT, 1991	Vector fitting, 1999	Iterative Extrapolation, 2008	Non-iterative Extrapolation, 2018
Accuracy	Low (non-causal)	High (fine fitting)	High (step resolution)	High (LSE)
Causality	X	O	O	O
Low Freq. data	Required	Required	Required	Extrapolation
Propagation delay	Not required	Required	Required	Delay estimation
Efficiency of the method	High (IFFT only)	Mid (iterative fitting)	Low (iterative search)	High (non-iterative)
Commercial	-	Commercial 2	Commercial 1	Huwin

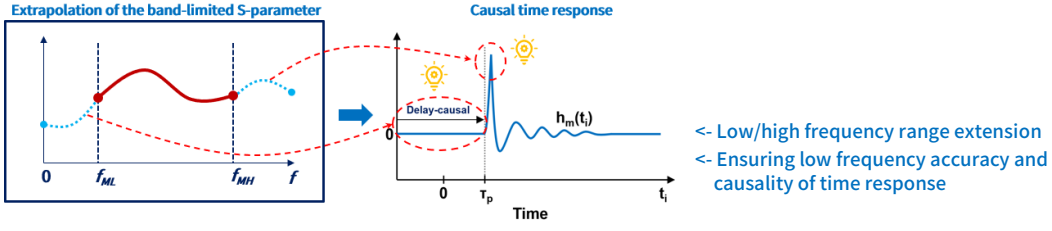


Figure 18. Extrapolation for extracting causal time response

SimNX offers the flexibility to handle all combinations of Tx/Rx buffer models, as shown in Table 2. It allows for analysis using both AMI (IBIS-AMI) models and S-parameters models, as demonstrated in Figure 19. Notably, it includes an industry-first feature that enables the batch analysis of all channel nets, considering cross-talk effects, using AMI modeling. This capability makes SimNX a comprehensive and powerful tool for conducting channel S-parameter model analysis with a wide range of options to suit different scenarios and requirements.

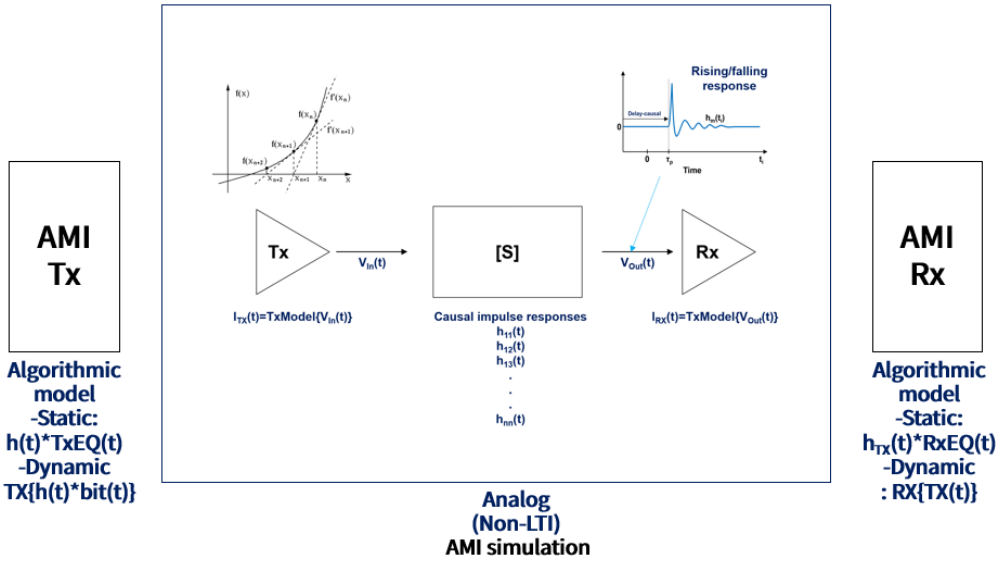


Figure 19. ACVS Hybrid type analysis: Non-LTI(Transient sim.) + LTI (AMI model)

Results of users who have employed ACVS embedded with the SimNX engine are shown in Figure 20. It shows a comparison between ACVS and standard SPICE transient analysis simulations. Both tools yielded equivalent results, but ACVS produced results within a significant less time frame, even when considering the time required for the automatic reporting process into account. Users have reported time savings of more than 20x when using ACVS, making it a highly efficient solution for channel analysis.

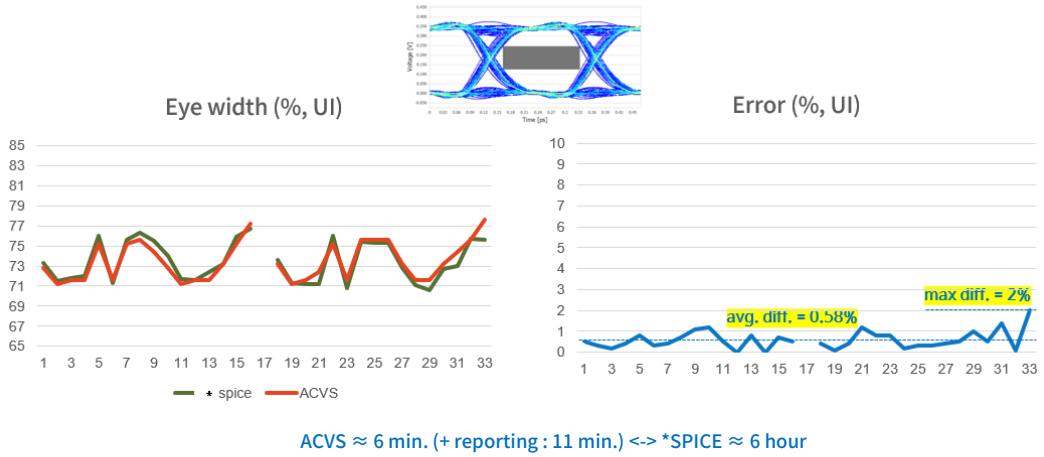
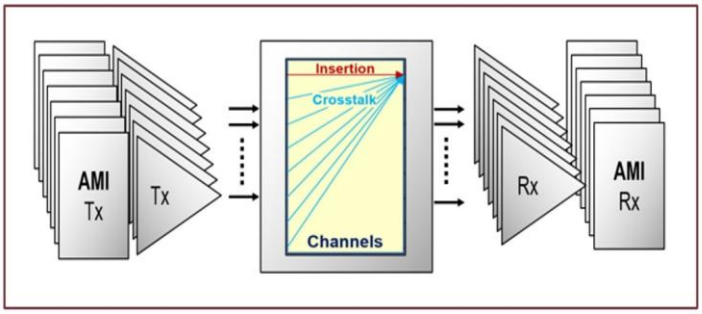
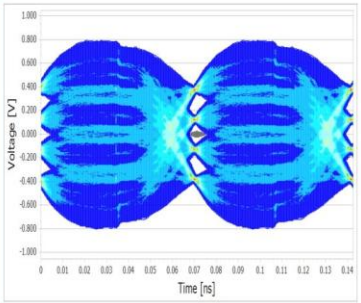


Figure 20. Full transient results comparison (standard spice vs. ACVS)

As shown in Figure 21, ACVS incorporates crosstalk across the entire channel during SerDes AMI analysis, ensuring accuracy while enabling faster analysis with improved computational efficiency compared to competitors.





SerDes AMI Analysis	Golden Standard-1 (circuit simulator)	Golden Standard-2 (circuit simulator)	Huwin ACVS (SI solution)
Single Pair with Cross-talk	Not Supported	**Support**	**Support**
Full Channel Pairs with Cross-talk	Not Supported	Not Supported	**Support**
Report Automation	Not Supported	Not Supported	**Support**

Figure 21. Supports Fully Automated AMI Simulation Including All Crosstalk Effects

2.2.3. ACVS S-tools

ACVS provides tools for both S-parameter generation and correction. These tools are designed to assist in the generation and correction of S-parameter models. This comprehensive set of features makes ACVS a valuable solution for various aspects of channel analysis and verification.

S-Designer:

S-Designer, which is a feature within ACVS, serves as a tool for generating S-parameters. It functions by allowing users to input desired characteristics or specifications for S-parameters, such as Insertion Loss, Return Loss, PSNEXT, and PSFEXT targets. Once these specifications are provided, S-Designer automatically generates S-parameter models that match the specified values. These generated S-parameters adhere to the principles of Causality, Reciprocity, and Passivity and serve as physical models that can replace actual channel models. For the Ch. system simulation, sample S-parameters that meet the performance specifications of each channel can be generated.

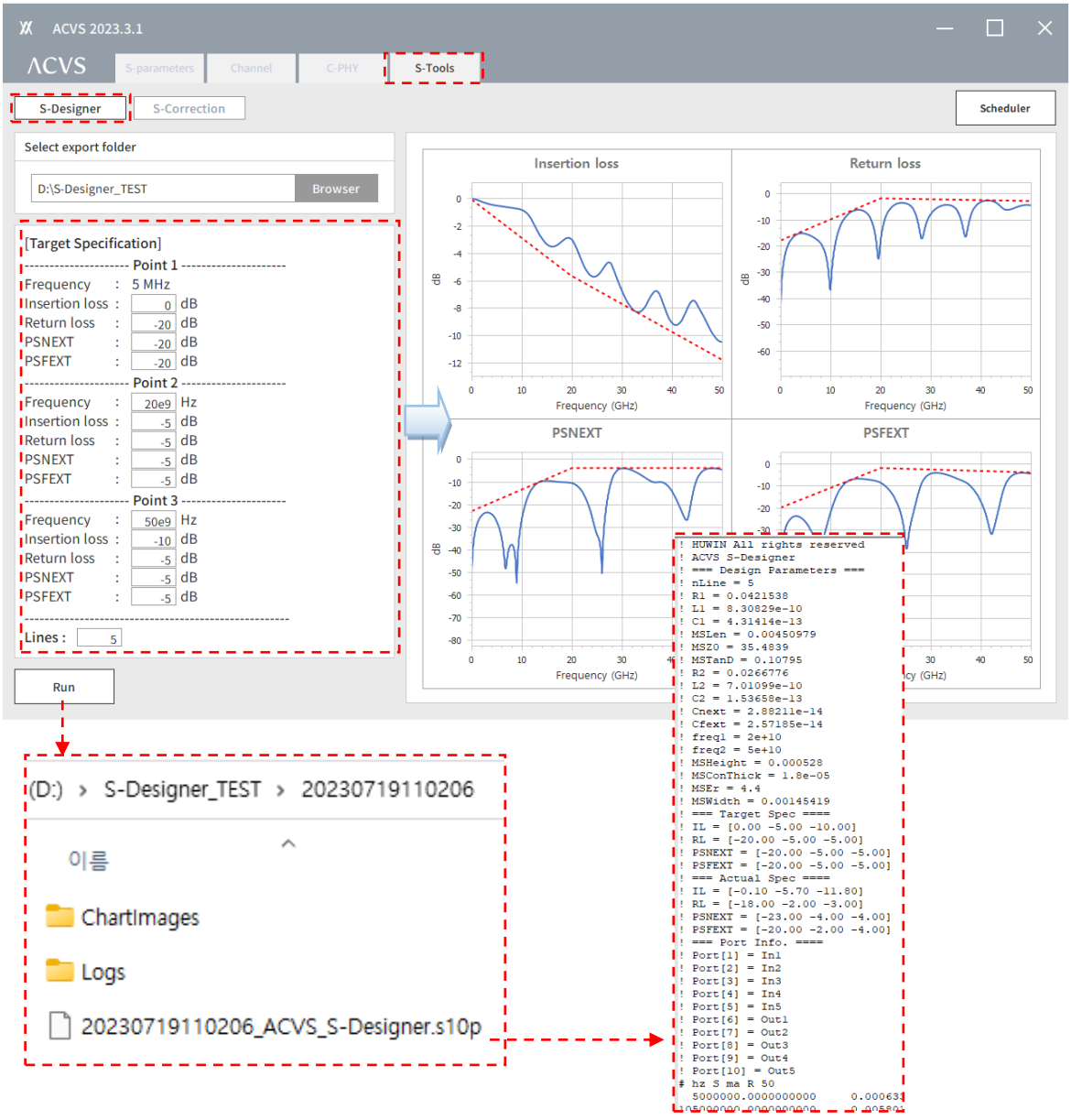


Figure 22. ACVS S-Designer (S-parameter model generation)

S-Correction:

S-Correction, a feature of ACVS, serves as a tool for correcting S-parameters. It works by checking the input S-parameters for errors related to Causality, Reciprocity, and Passivity. When errors are detected, S-Correction applies corrections to the S-parameter data, where it will output the corrected S-parameter files. It offers a chart view that allows users to compare the Causality, Passivity, and Total error before and after correction, facilitating a visual assessment of the improvements made. This feature ensures that the S-parameter data conforms to the essential principles of signal integrity.

Figure 23. ACVS S-Correction (S-parameters model correction)

Correction option:

✓Causality: Enforcing causality

✓Reciprocity: Enforcing reciprocity (S(i,j)=S(j,i))

✓Passivity: Enforcing passivity (with the ensured causality)

Results

✓Causality error: Max error of the causality enforcement (NMSE in dB)

$S_{causal}(i,j)$ vs $S_{original}(i,j)$

✓Passivity (max): Max passivity value

✓Total error: Max error of the total results (NMSE in dB)

$S_{total}(i,j)$ vs $S_{original}(i,j)$

Line-FEM Pro:

Line-FEM Pro is a 2D FEM-based transmission line design tool. Similar to S-Designer, it provides an automatic transmission line design feature based on required S-parameter characteristics (target specs for Insertion Loss, Return Loss, PSNEXT, and PSFEXT). Users can input stackup-related parameters (e.g., metal thickness, dielectric height/permittivity, etc.) and obtain design results, including dimension information, W-element files, S-parameter files, and E/H field data.

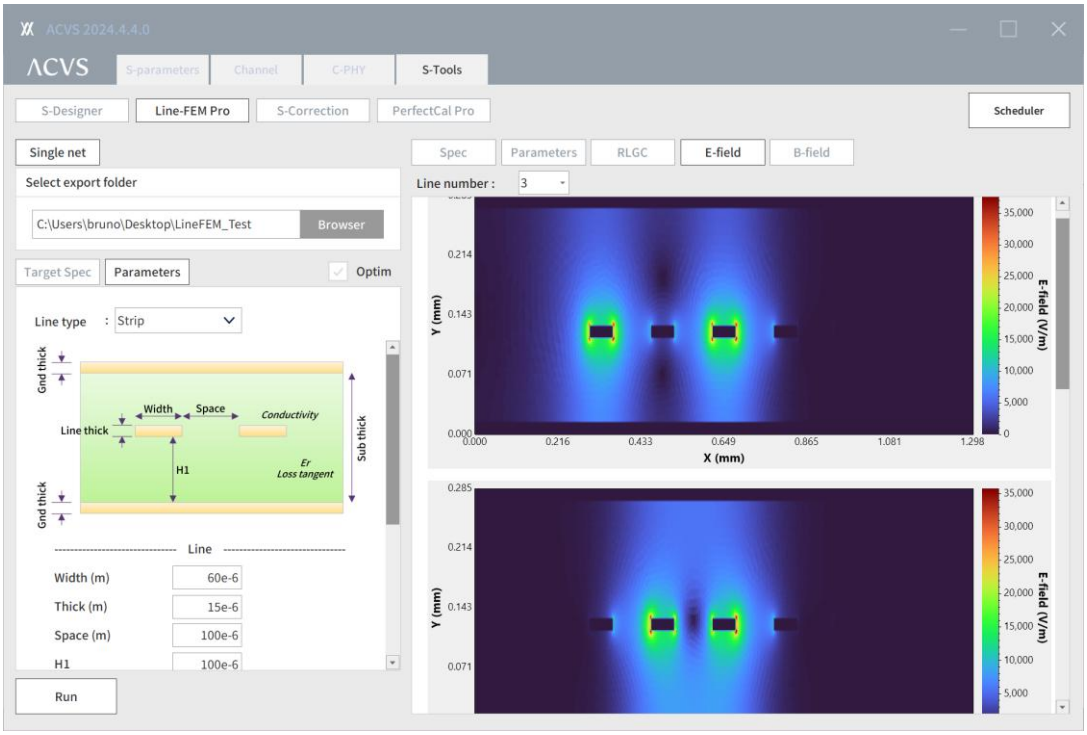


Figure 24. ACVS Line-FEM Pro (high-precision transmission line design tool)

PerfectCal Pro:

PerfectCal Pro is a 2xThru-based de-embedding tool with industry-leading precision. It accurately extracts the S-parameters of 1x fixtures and DUTs using 2/4-port thru fixtures.

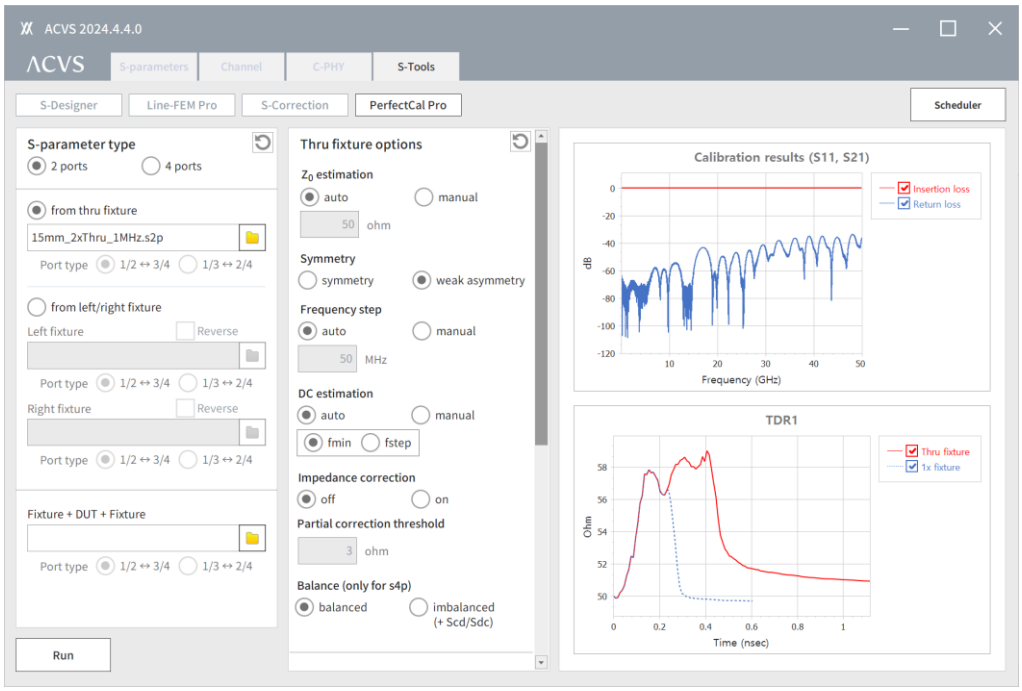
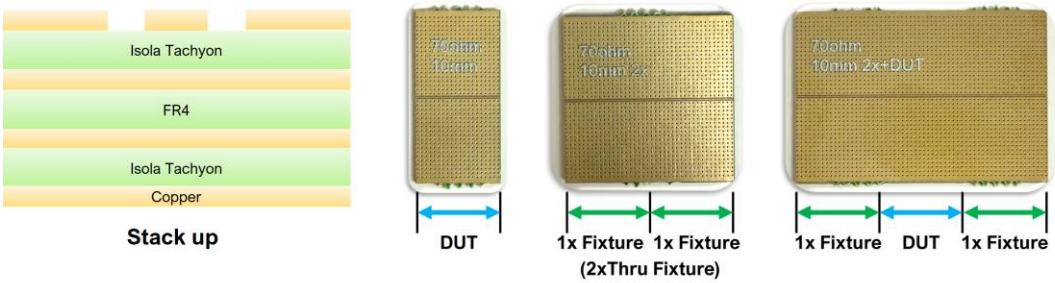
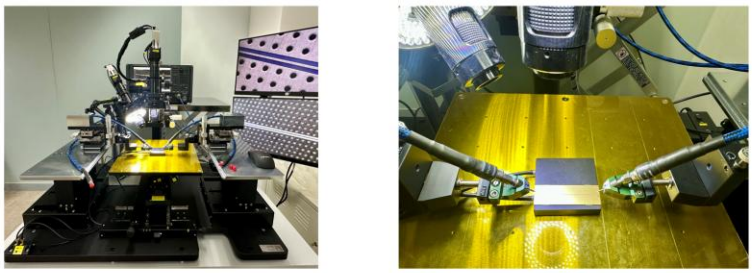


Figure 25. ACVS PerfectCal Pro: Professional grade 2xThru de-embedding tool.

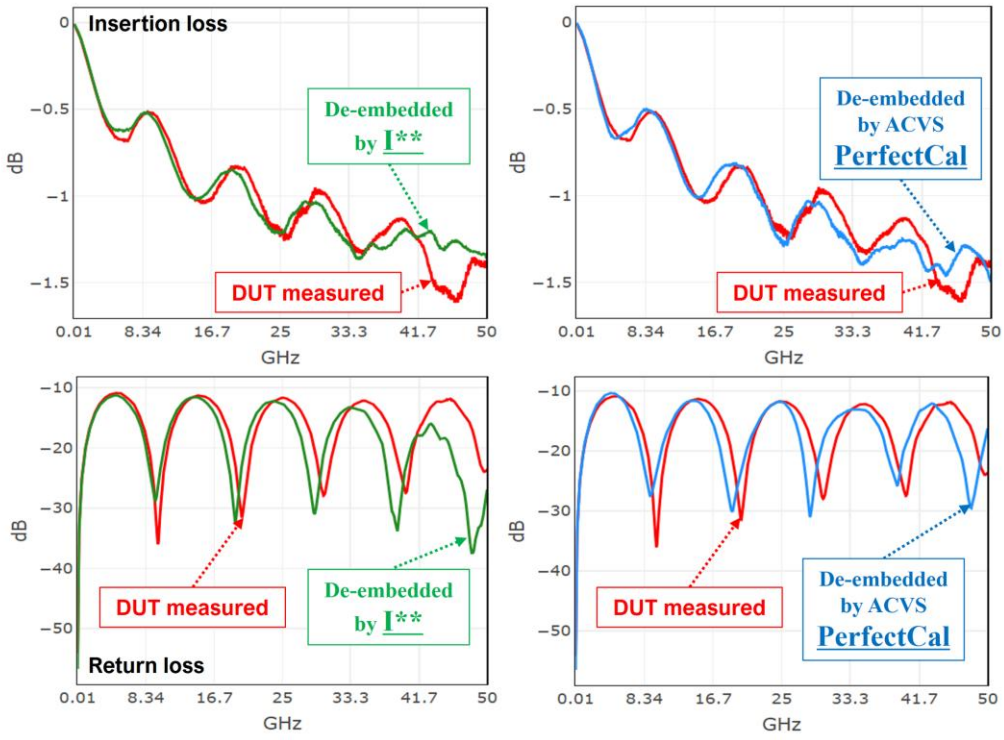
Figure 25 presents a case study validating the de-embedding performance of PerfectCal Pro. A CPWG transmission line structure, including 2xThru, Fixture+DUT, and DUT, was designed. Measurements were conducted using a Keysight PNA N5225B (up to 50 GHz) and a T-plus microprobe. The results of direct probing on the DUT were compared with de-embedding results obtained using PerfectCal Pro and competing tools. The comparison confirmed that PerfectCal Pro's de-embedding results demonstrated a higher similarity to the actual measurement results than those of other tools.



DUT: CPWG 10mm (Z_0: 70 ohm) and 2xThru Fixture



Measurement Setup @ Huwin Lab
(Keysight PNA N5225B, T-plus uProbe)



Direct Probing(DUT measured) vs De-embedded(I vs ACVS PerfectCal)**

Figure 26. ACVS Line-FEM Pro (high-precision transmission line design tool)

2.3. How to use ACVS

ACVS relies on the analysis of a channel's S-parameters, which makes the extraction of S-parameters a crucial step before the analysis can begin. S-parameter extraction is typically carried out using EM model extraction tools such as ANSYS. It's essential to emphasize that obtaining an accurate and suitable model during this extraction process is of utmost importance. Therefore, thorough research into the principles and methods of EM analysis for model extraction is necessary.

2.3.1. Ch. Model extraction

EM analysis basic and model extraction by using EM analysis tool:

A channel, in the context of connecting high-capacity and high-frequency data, refers to the physical structure of the signal path. The channel structure is composed of various design elements such as bumps, pads, vias, traces, balls, and the reference ground that together make up the entire channel. To validate and address the issues that arise during the design of each physical structure and property within the channel for high-capacity/high-frequency data transmission, it is essential to go through a process of extracting (modeling) a model that represents the electrical characteristics of the entire channel structure. This process can be accomplished through Electro-Magnetic Field Analysis (EM analysis).

Through EM analysis, a comprehensive S-parameter (SnP) model is extracted that includes characteristics such as insertion loss, return loss, crosstalk, and impedance, among others, at various frequencies. The extraction of S-parameter models for 3D channel structures is typically performed using the 3D Finite Element Method (FEM) approach with EM simulation tools. One of the prominent simulation tools for this purpose is ANSYS's HFSS (High Frequency Structure Simulator).

The process of 3D FEM-based EM analysis, as shown in Figure 27, involves several steps. It starts with inputting the structural and material properties, defining EM boundary conditions, and configuring ports for high-frequency excitation. Following these initial steps, an automatic adaptive meshing process is used to create a detailed 3D mesh for the given 3D structure. Finally, the 3D FEM analysis solver performs the analysis based on the resulting mesh to generate the desired results.

ACVS provides a functionality module that automates the entire analysis setup and model extraction process for ANSYS EM analysis using ANSYS scripting. This automation streamlines the process, making it more efficient and less prone to manual errors when setting up the analysis and extracting the model. It enhances the usability and productivity of ANSYS EM analysis for users.

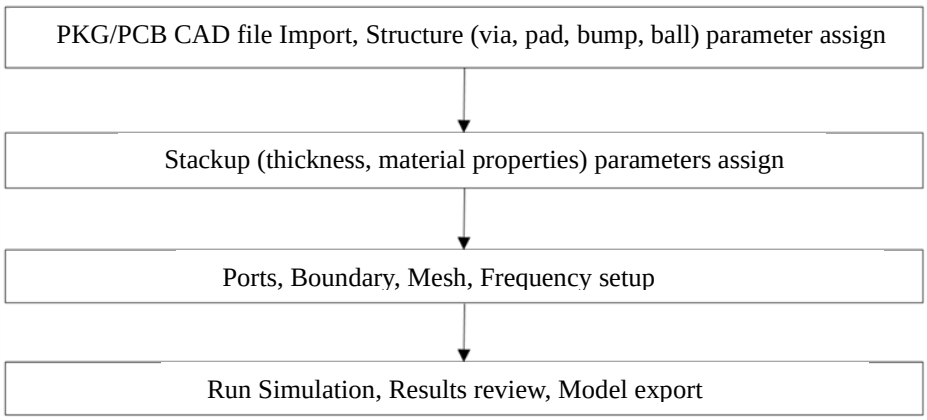


Figure 27. EM Analysis and Model Extraction Procedure

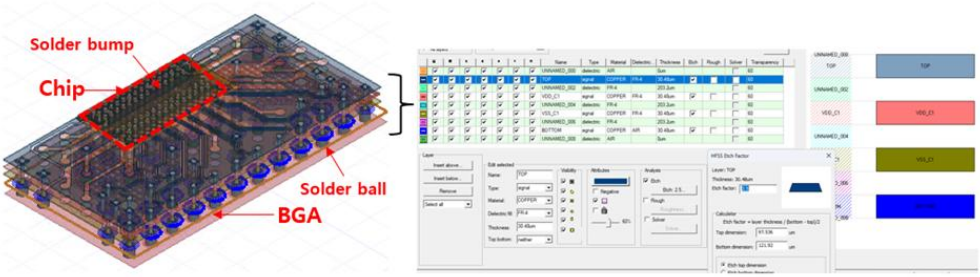


Figure 28. PCB/PKG CAD file Import, Structure and Stack-up parameters assign

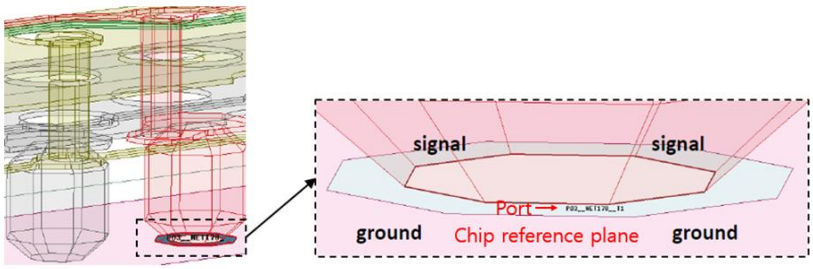


Figure 29. BGA side signal excitation port assign

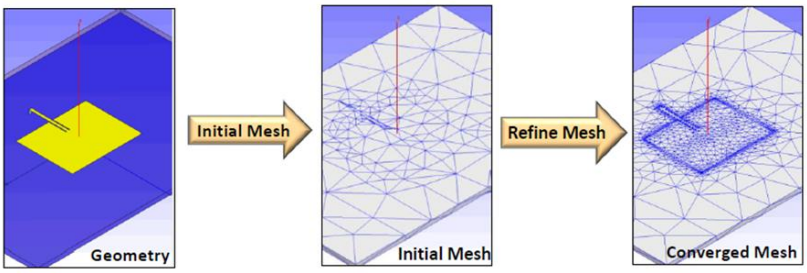


Figure 30. ANSYS HFSS FEM Adaptive Meshing

Figures 28, 29, and 30 illustrate the CAD input, port configuration, and meshing process in the EM analysis, respectively. The Finite Element Method (FEM) solver applies Maxwell's equations to each element of the mesh, performing matrix operations for each element input to calculate the results of the EM field. From the results of the EM field, the signal input/output functions at each port can be calculated. This allows for the verification of parameters such as return loss and insertion loss for each channel net, as shown in Figures 31 and 32.

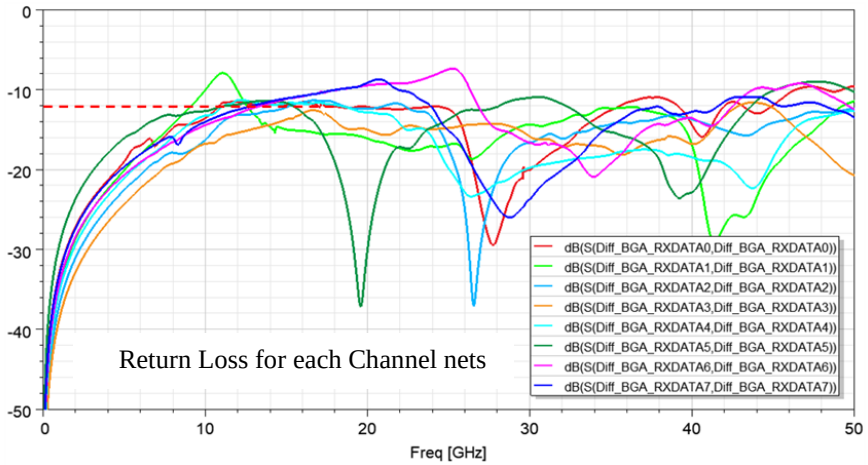


Figure 31. EM analysis results , Return Loss

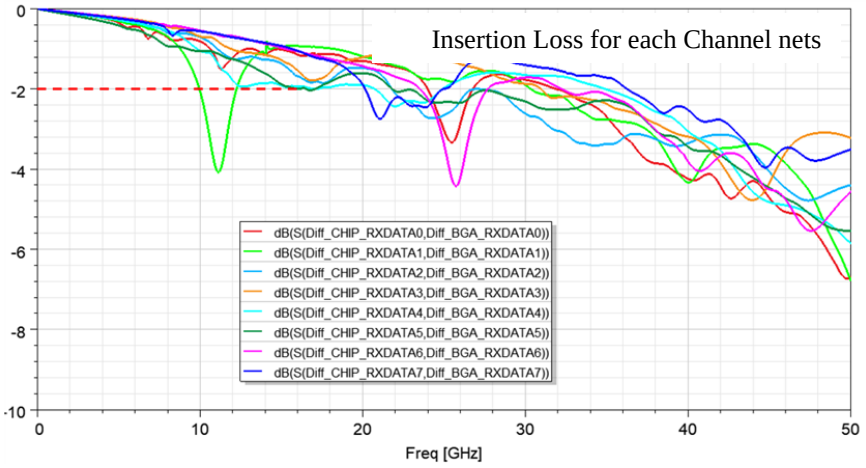


Figure 32. EM analysis results , Insertion Loss

2.3.2. ACVS Analysis example

For high-capacity data transmission, memory and PCIe signals in recent designs have become extremely high-speed (over 10 Gbps) and ultra-wideband (0-100 GHz). Additionally, the number of signal traces for high-capacity signals has increased from hundreds to thousands, leading to higher channel densities in PKG/PCB designs. When these high-frequency signals are transmitted through high-density channels, signal reflections and interference in the channel can lead to problems in meeting high-capacity data transmission specifications. Therefore, as shown in Figure 33, it is essential to perform EM simulations (modeling) and ACVS verification in the early pre-layout design phase to identify and rectify any issues and ensure compliance with the specifications.

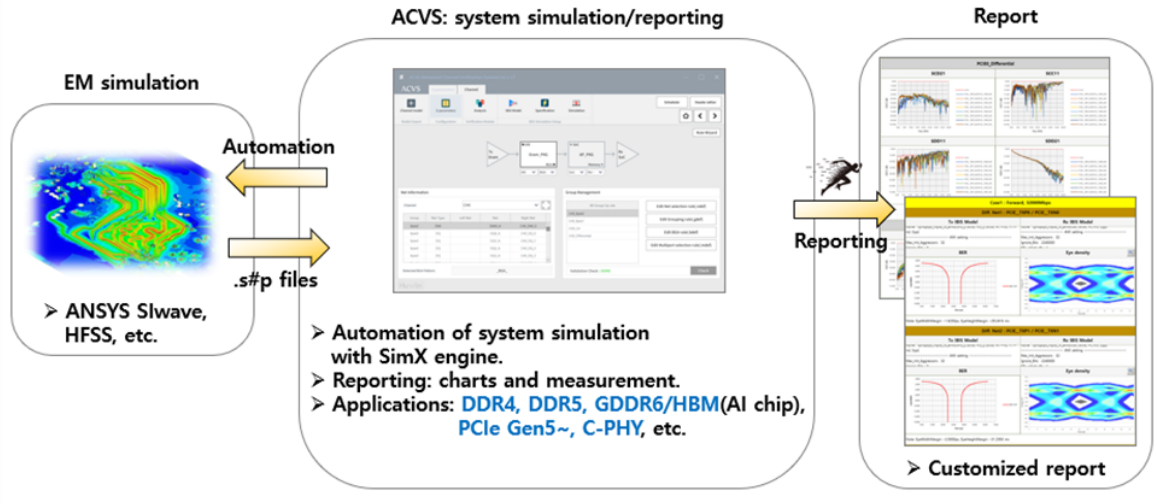


Figure 33. EM Simulation/ Modeling and ACVS verification

The channel validation process in ACVS, as illustrated in Figure 34, involves an iterative procedure where the analysis, layout modifications, and verification steps are repeated until the validation results for the channel meet the required criteria.

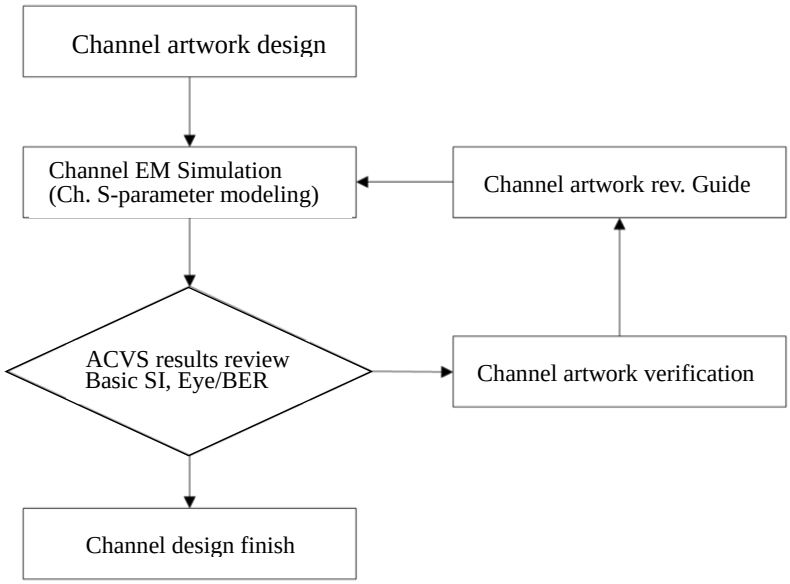
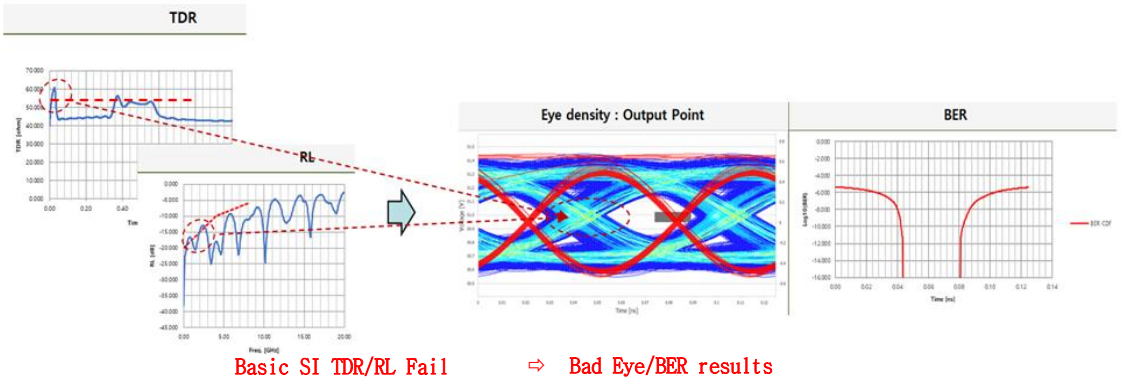


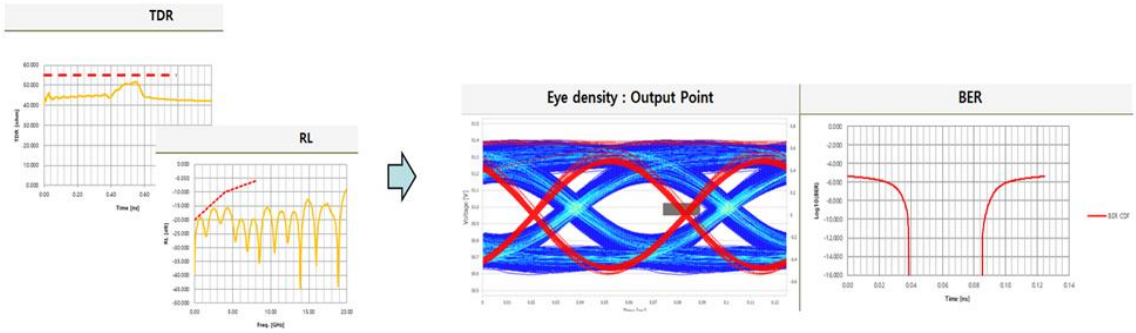
Figure 34. ACVS channel design verification procedure

In high-density memory package design, the effects of signal reflection can be observed and verified through examples like Figure 35. and Figure 36. These examples show the results of before and after modifications, allowing for the examination of Eye diagrams and Bit Error Rate (BER) validation.



Basic SI TDR/RL Fail ⇨ Bad Eye/BER results

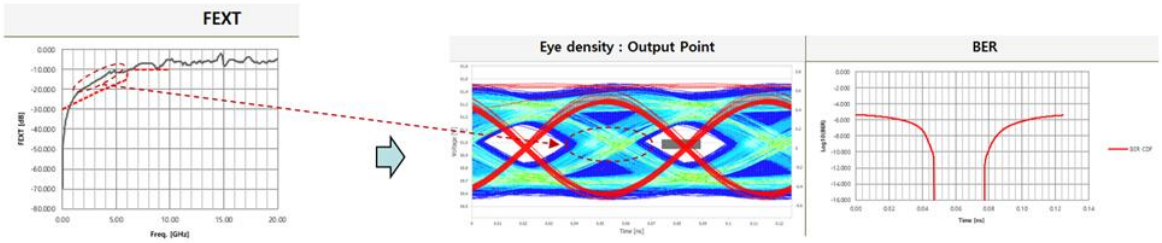
Figure 35. Before/After ACVS TDR/RL => Eye/BER verification



Basic SI TDR/RL Pass ⇨ Good Eye/BER results

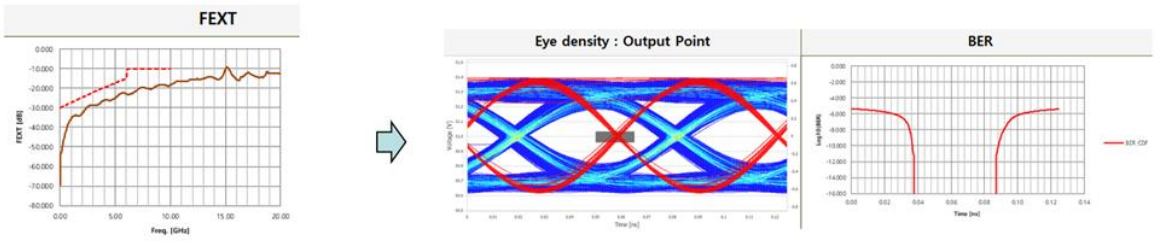
Figure 36. Before/After ACVS TDR/RL => Eye/BER verification

Furthermore, Figure 37. and Figure 38. illustrate the issues related to Crosstalk before and after artwork modifications, along with their corresponding Eye diagrams and Bit Error Rate (BER) results. ACVS channel verification and artwork adjustments demonstrate an improvement in Eye/BER results in the final outcome.



Basic SI crosstalk Fail ⇨ Bad Eye/BER results

Figure 37. Before/After ACVS FEXT => Eye/BER verification



Basic SI crosstalk Pass ⇨ Good Eye/BER results

Figure 38. Before/After ACVS FEXT => Eye/BER verification

2.3.3. ACVS Analysis setup

The process of creating projects, channel configuration, and analysis setup in ACVS has been optimized to handle channel models with many ports and large file size. Additionally, analysis setups can be saved as profile files, allowing for easy reusage of previous analysis setups when replacing the model with a revised version. This feature enables quick analysis of revised models and facilitates result comparison under the same conditions, making it a highly useful and convenient method.

Build project:

You can create a channel analysis project in ACVS by simply dragging and dropping the analysis model from a Windows Explorer folder into the ACVS UI. This user-friendly approach makes it easy to set up and initiate channel analysis projects.

Build -> IBIS analysis -> + channel -> Drag IBIS, SnP files -> Save & Import

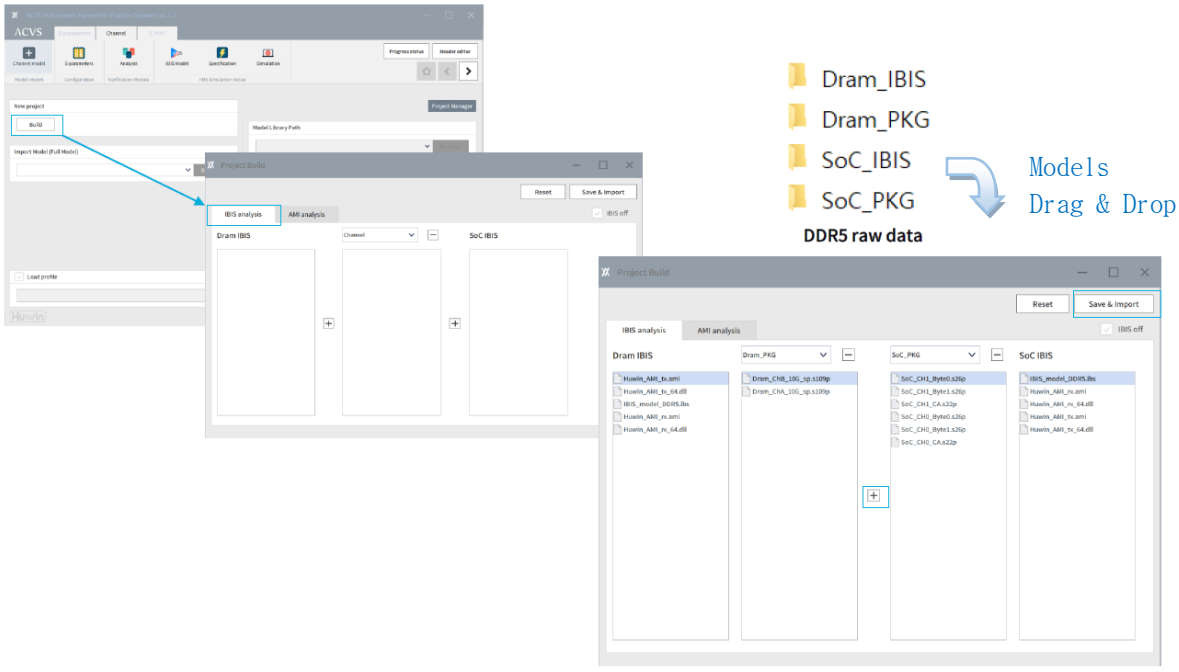


Figure 39. ACVS Build Project, Model Drag & Drop

ACVS rule setup:

ACVS simplifies the process of configuring rules for channel models by offering the Rule Assistant feature, which allows for auto rule setup. This feature, powered by Machine Learning (ML), is designed to automatically recognize and configure rules for most nets, making the rule setup process more convenient and efficient.

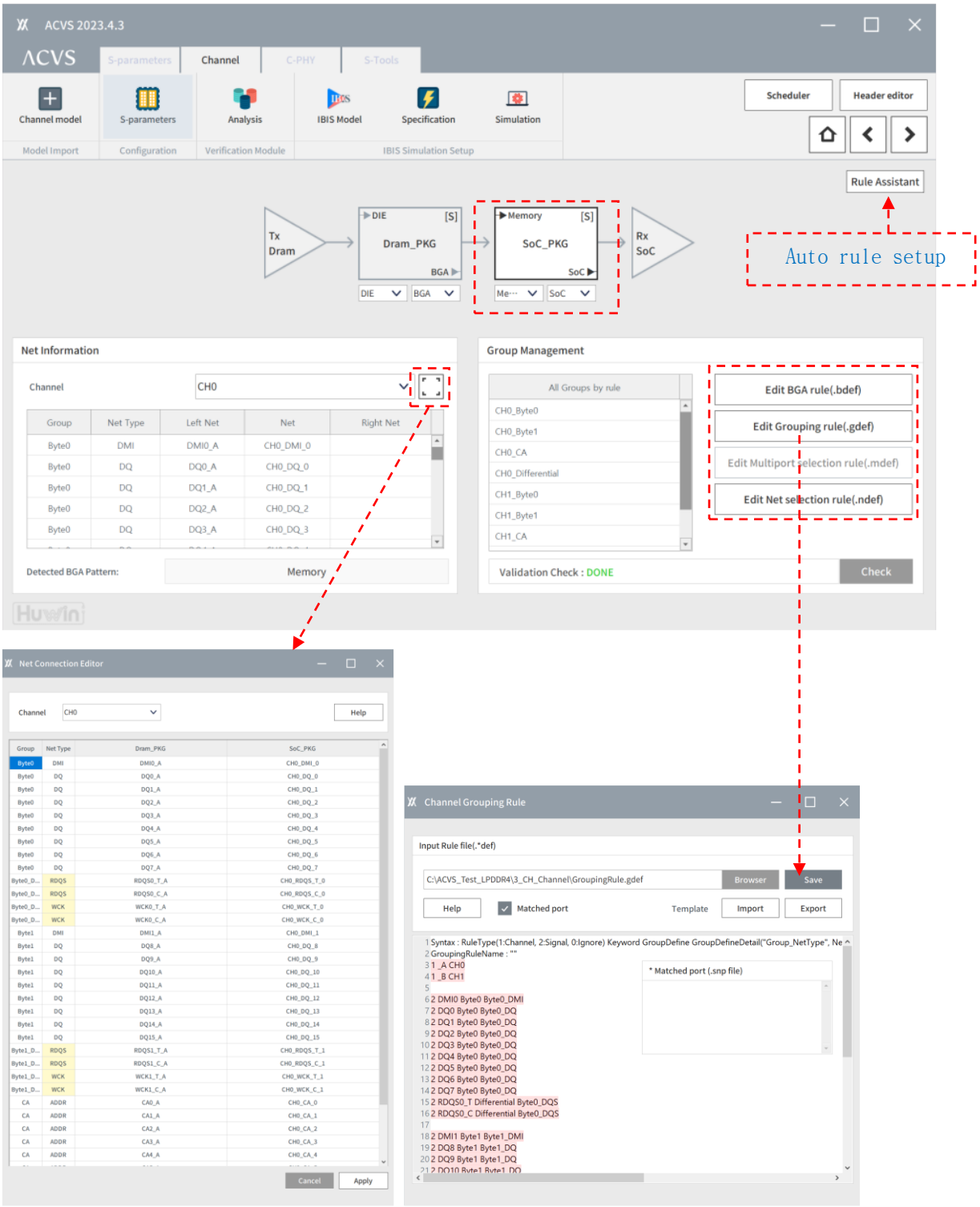


Figure 40. ACVS Ch. Rule setup

Transient Simulation Setup (Port Termination):

In the setup for multi-DIE branch structures as shown in Figure 41, it's possible to configure termination settings using DIE IBIS models for ports other than Tx and Rx.

Additionally, you can set terminations to 50 ohms or ground for ports that are not included in the analysis. This flexibility allows for precise termination control in the channel model.

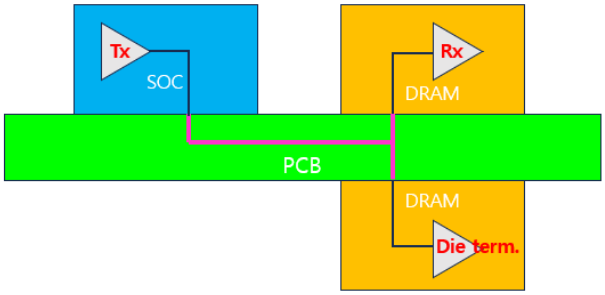


Figure 41. Multi DIE branch structure example (Clamshell configuration)

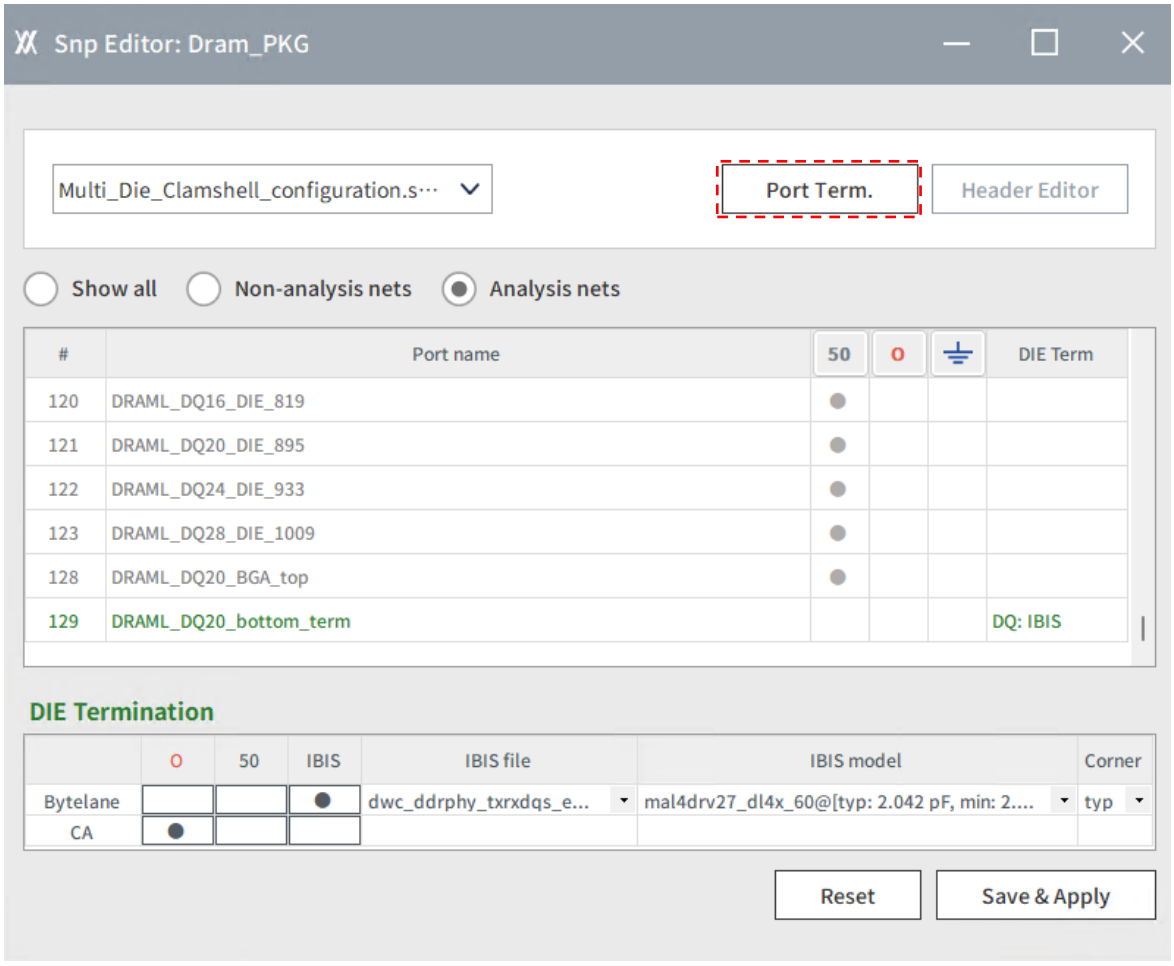


Figure 42. Port Termination for multi DIE configuration

Header Editor:

ACVS provides the SNP Header Editor, which allows you to view and edit header information of very large S-parameter files, such as those exceeding 40GB. In cases where the channel S-parameter model has a very large file size, it becomes impractical to open and edit using a regular text editor. Tools like the Header Editor are invaluable for selectively opening, editing, saving, and verifying frequency information of the model by focusing only on the header. This enhances the usability and manageability of large S-parameter files in the analysis process.

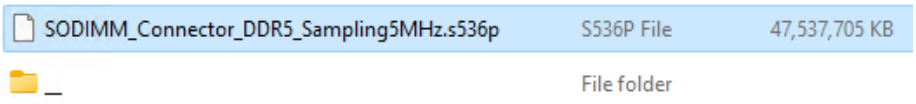


Figure 43. Large size S-parameter example: 536ports, 47GB file size

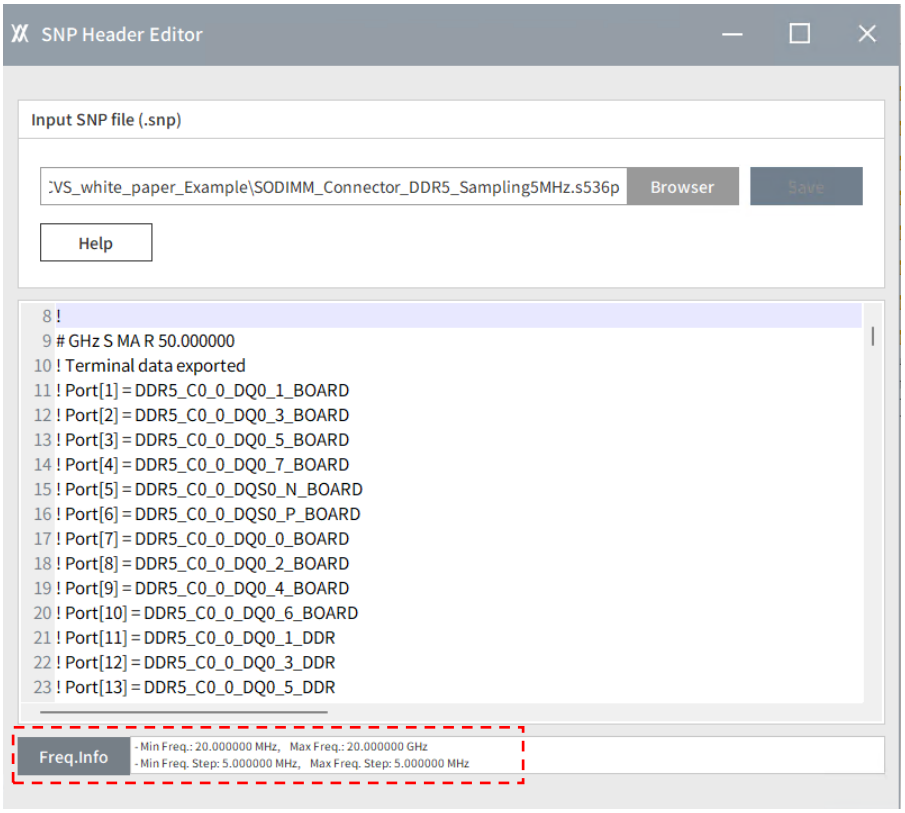


Figure 44. ACVS Header Editor and Freq. Info.

Transient Simulation Setup (IBIS model and Write/Read mode):

In memory channel analysis, when you choose the Write/Read mode, ACVS is configured to automatically select available models for Rx and Tx. Additionally, through model selection for each mode, you can add multiple analysis cases, allowing you to perform analyses for each case separately. This feature provides flexibility in analyzing different scenarios and modes in memory channel analysis.

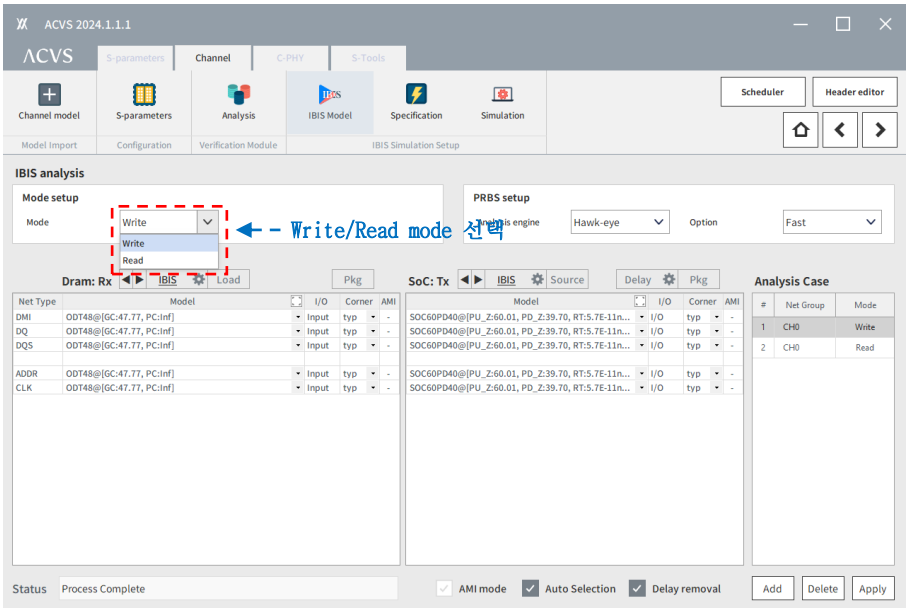


Figure 45. ACVS Transient analysis setup (write/read)

Transient Simulation Setup (Hawk-eye/PRBS):

ACVS's Hawk-eye feature is designed to efficiently predict Eye results for memory signals by generating the optimal bit combinations. It ensures that you can achieve the most accurate and effective Eye results for memory channel analysis. Additionally, if necessary, ACVS allows for PRBS (Pseudorandom Binary Sequence) and manual bit input, providing flexibility in signal generation and analysis.

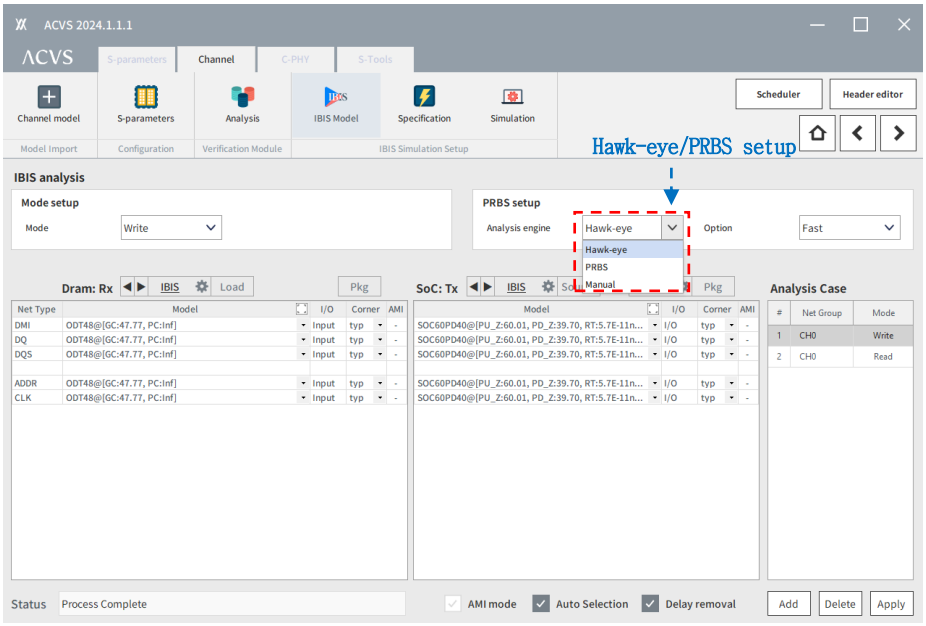


Figure 46. ACVS Hawk-dye / PRBS setup

Transient Simulation Setup (Fast/Optimal/Strict):

ACVS's Hawk-Eye feature offers three options: Fast, Optimal, and Strict. When you select these options, it analyzes the channel with bit combinations that include worst bits for various parameters. These parameters include worst ISI (Inter-Symbol Interference), worst jitter by X-talk, worst over/undershoot by X-talk, and more. This allows you to perform a comprehensive analysis of the channel with fewer bit combinations compared to PRBS, making the process more efficient.

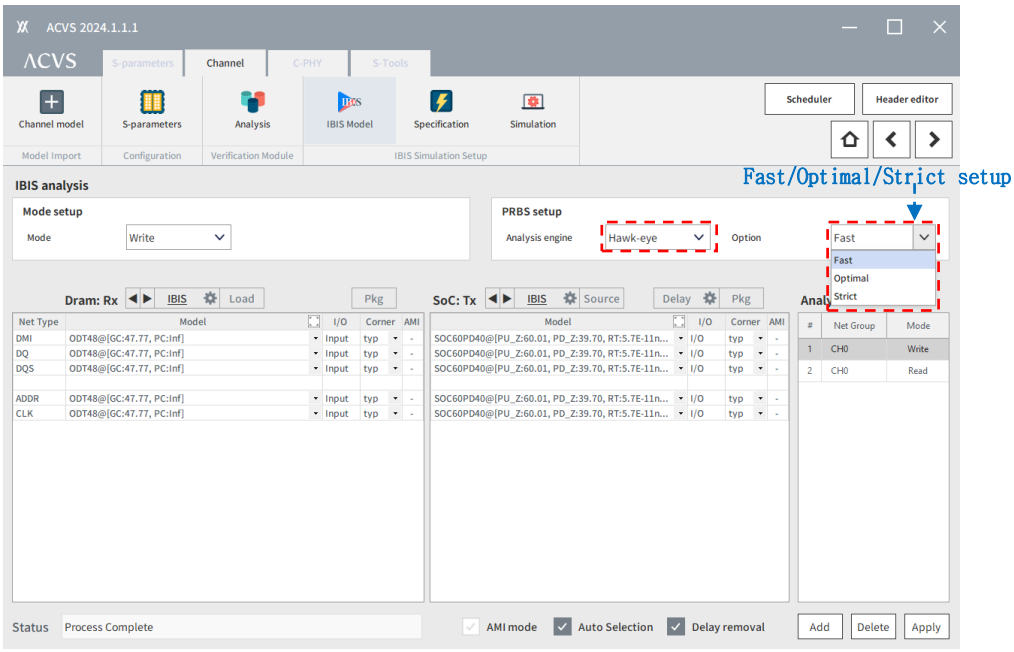


Figure 47. ACVS Transient simulation setup (Fast/Optimal/Strict)

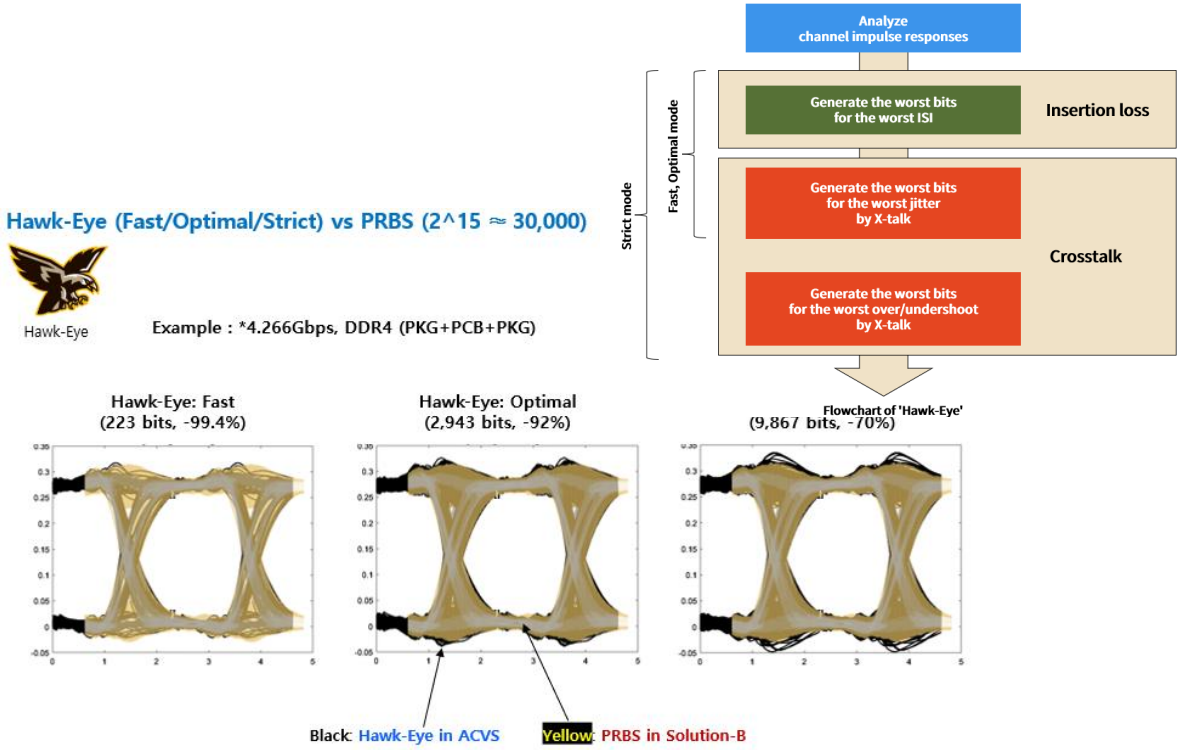


Figure 48. ACVS Hawk-Eye Fast/Optimal/Strict vs. PRBS: bits & results comparison

Transient Simulation Setup (AMI mode / Auto Selection / Delay removal):

In ACVS AMI mode analysis, you can configure the AMI parameters for Serdes or Memory Tx and Rx AMI models to perform the analysis. This allows you to customize the analysis based on the specific AMI parameters relevant to your simulation.

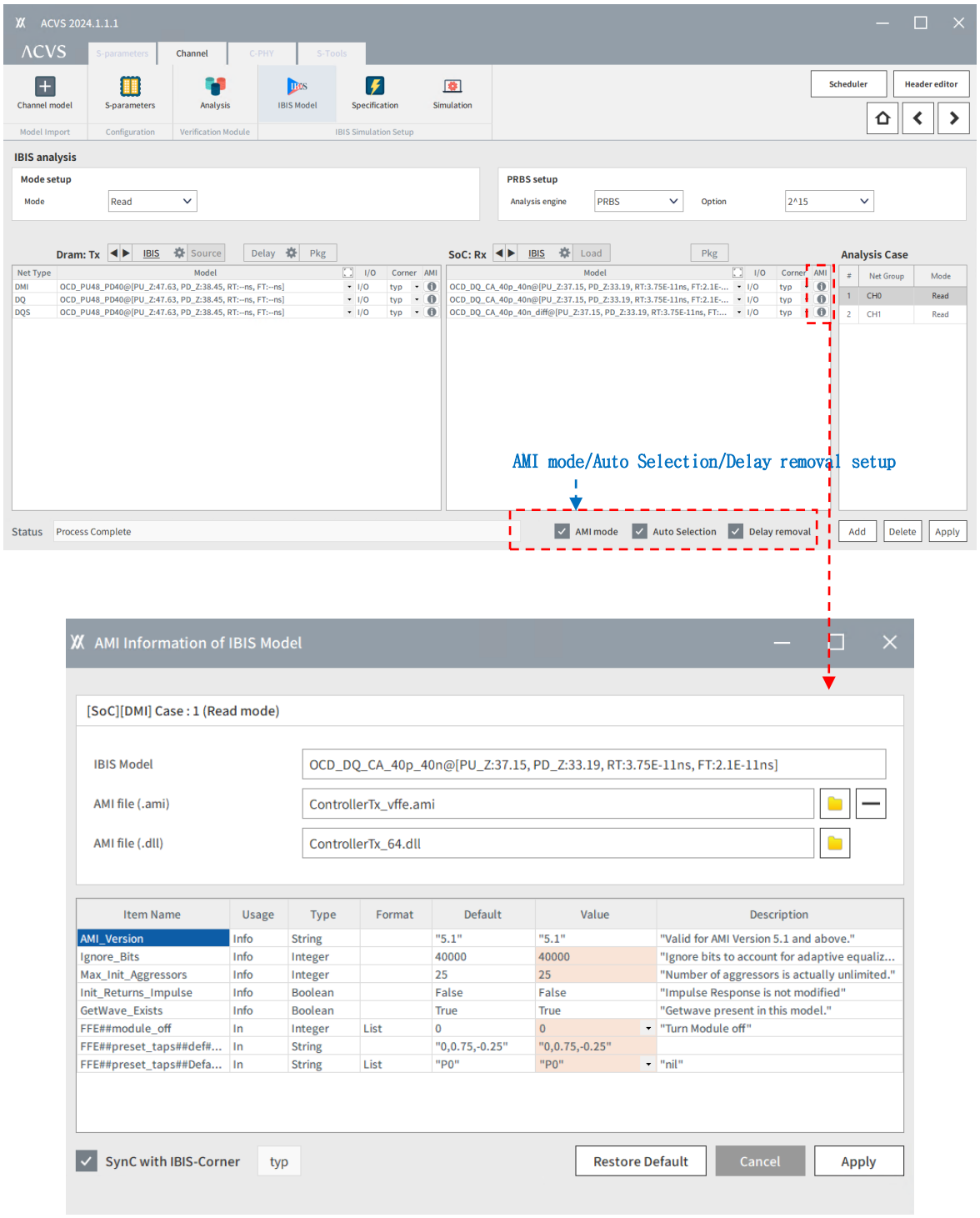


Figure 49. ACVS Transient Simulation setup (AMI mode, Auto Selection, Delay removal)

ACVS's AMI mode analysis allows for various combinations of AMI models, Ideal Source models, and IBIS models for both Tx and Rx models. This flexibility allows you to choose the most appropriate combination for your specific simulation needs.

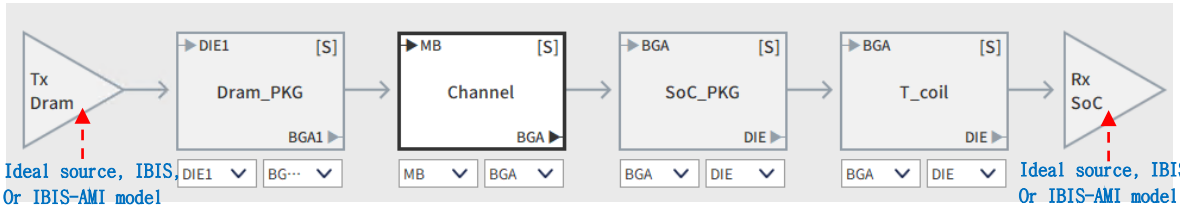


Figure 50. ACVS ch. configuration with Tx, Rx (Ideal source, IBIS, IBIS-AMI) model

Supported Tx, Rx analysis model:

- Ideal Source: In cases where the Tx or Rx models have not been received from the vendor.
  - ➔ Tx: define Driver voltage, Trf, C_comp, Source Impedance (single or differential)
  - ➔ Rx: define Load's C_comp, Load Impedance (single or differential)
  - * The setup to enable custom EQ for Tx or Rx is planned for the ACVS 2024 update.
- IBIS model: The IBIS model received from the vendor (PKG model with linked S-parameters in the same folder is automatically set up. PKG RLC values can be activated, but it is not recommended for channels with signals above 2Gbps.)
- IBIS-AMI model: When IBIS (*.ibs) files, *.ami, *.dll, and PKG S-parameters are present in the Tx and Rx model folders (PKG S-parameters are defined in IBIS, so they are automatically linked).

Talbe 2. Supported ACVS Tx, Rx model combination Case

Tx model case	Rx model case	ACVS analysis support
Ideal Source	Ideal Source	O
Ideal Source	IBIS model	O
Ideal Source	IBIS AMI model	O
IBIS model	Ideal Source	O
IBIS model	IBIS model	O
IBIS model	IBIS AMI model	O
IBIS AMI model	Ideal Source	O
IBIS AMI model	IBIS model	O
IBIS AMI model	IBIS AMI model	O

Auto Selection: The Auto Selection feature automatically selects the Memory IBIS buffer model based on the net type. It recognizes the Net Type keywords such as DQ, DQS, DMI, CLK, CKE, ADDR, etc., and sets the model accordingly.

Delay removal: The Delay Removal feature, as shown in Figure 51, is used to eliminate the delay portion in IBIS rising/falling output waveforms when there is a significant delay. This is done to address potential issues, such as overclocking, that can occur due to triggering of logic input signals.

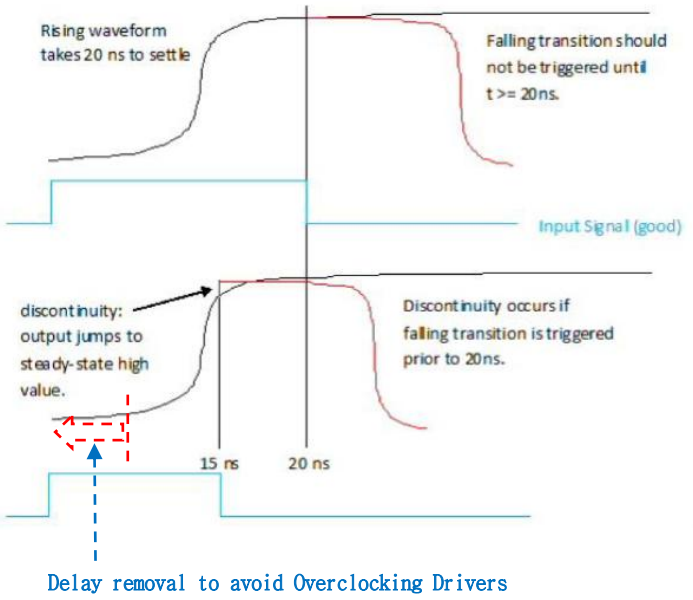


Figure 51. ACVS delay removal

Data Rate Rule setup:

The timing and voltage mask values for different DataRates according to JEDEC specifications can be managed and edited using the saved rule file, as shown in Figure 52. These saved rules can be selected and applied to the analysis, functioning like a library of settings for different scenarios.

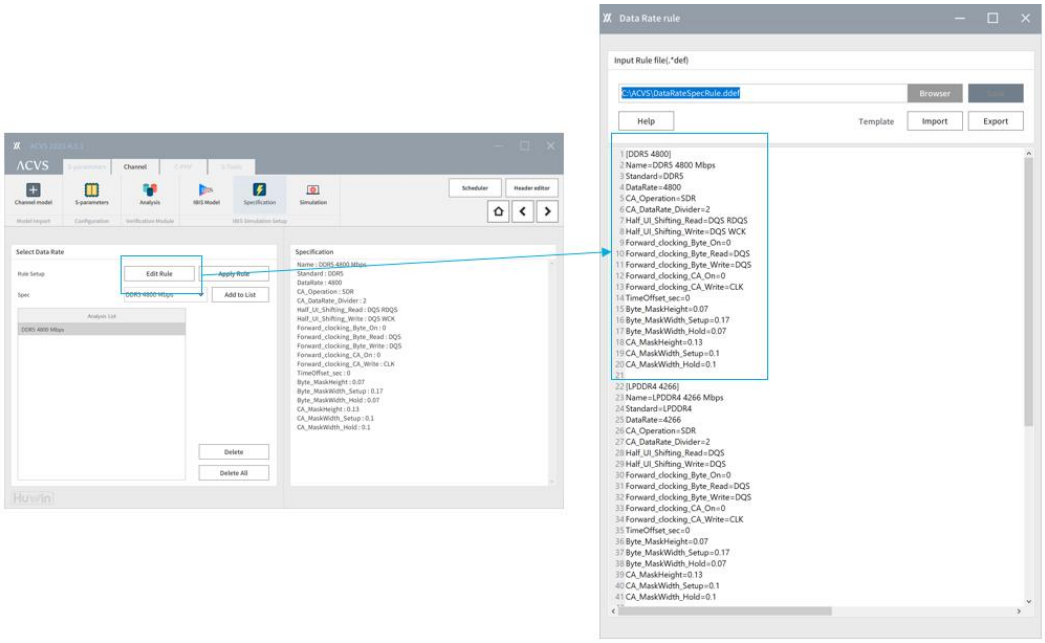
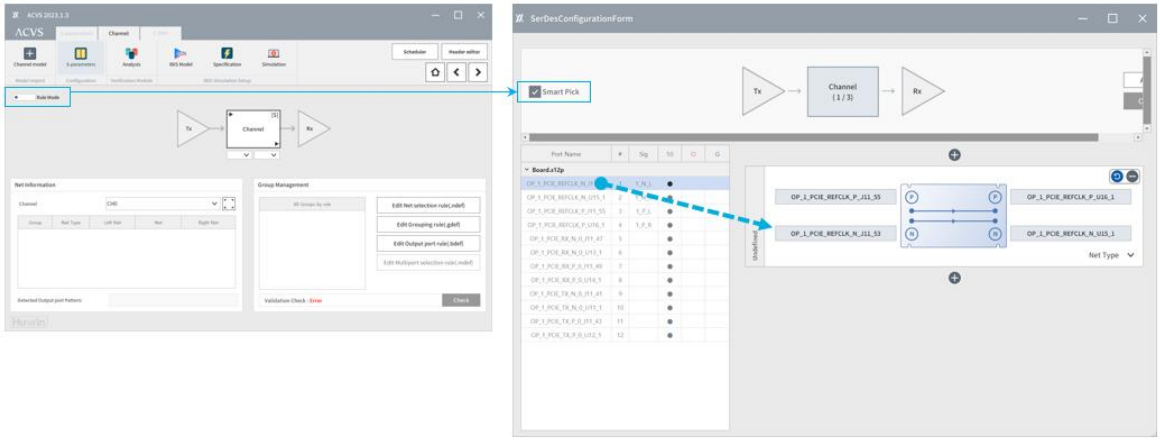


Figure 52. ACVS Ch. Spec. setup : Data rate, SDR/DDR/QDR, timing/voltage Mask

Smart Pick, Serdes Ch. Configuration:

In ACVS, during SerDes channel analysis, you can search for ports with specific keywords using the search bar. With the Smart Pick feature, dragging and dropping a specific port automatically identifies all constituent ports of the differential pair, creating the differential pair channel automatically. Additionally, the signal direction of the SerDes channel can be configured after channel setup by clicking the arrow indicating the direction.



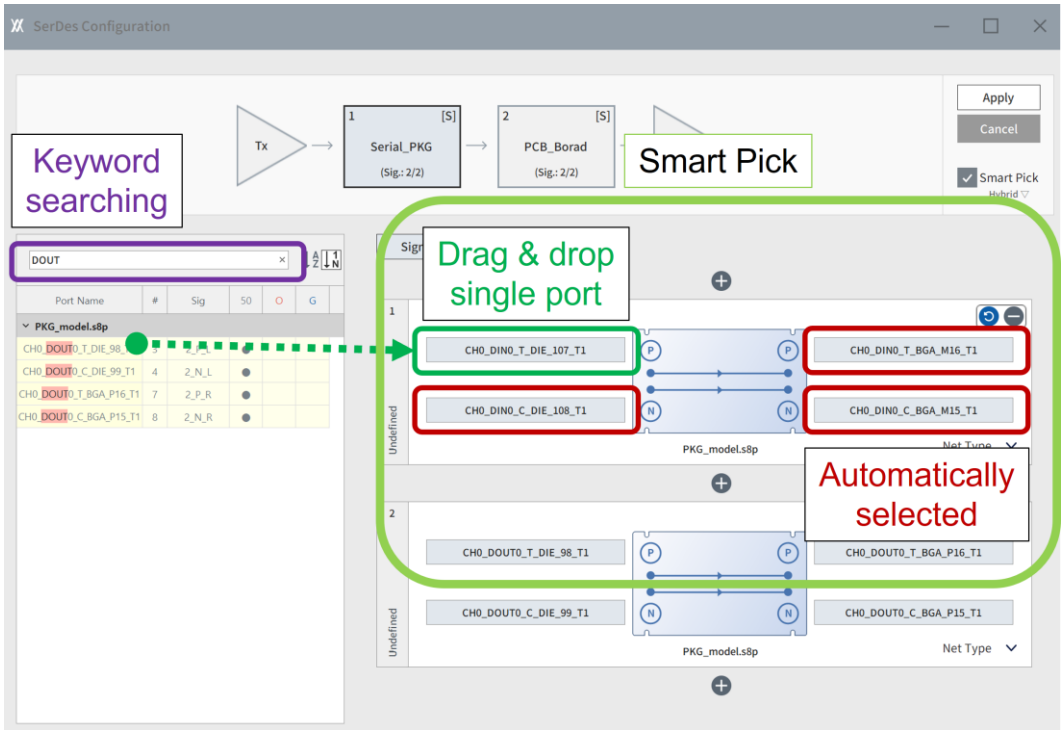


Figure 53. ACVS UI mode ‘Smart pick’ Ch. configuration

Analysis Run and Scheduler:

After setting up the analysis in ACVS, when you click the Run button (>) as shown in Figure 54, the analysis job is added to the ACVS Scheduler. Each analysis job is performed sequentially, and you can change the execution order of the uploaded jobs. Figure 55 represents the Progress Status and Log window.

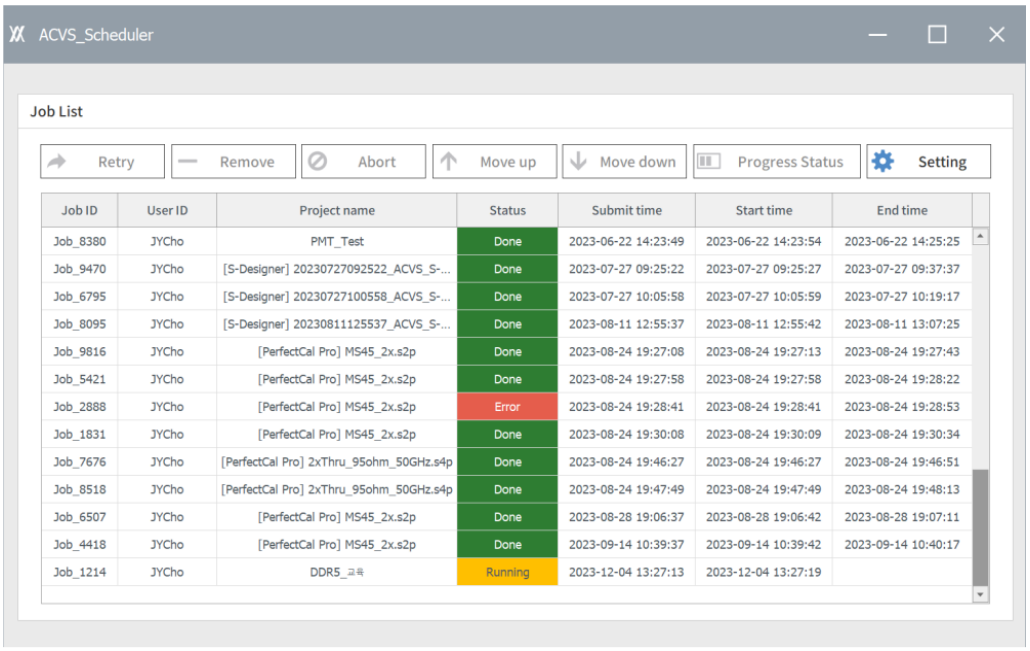


Figure 54. ACVS Scheduler

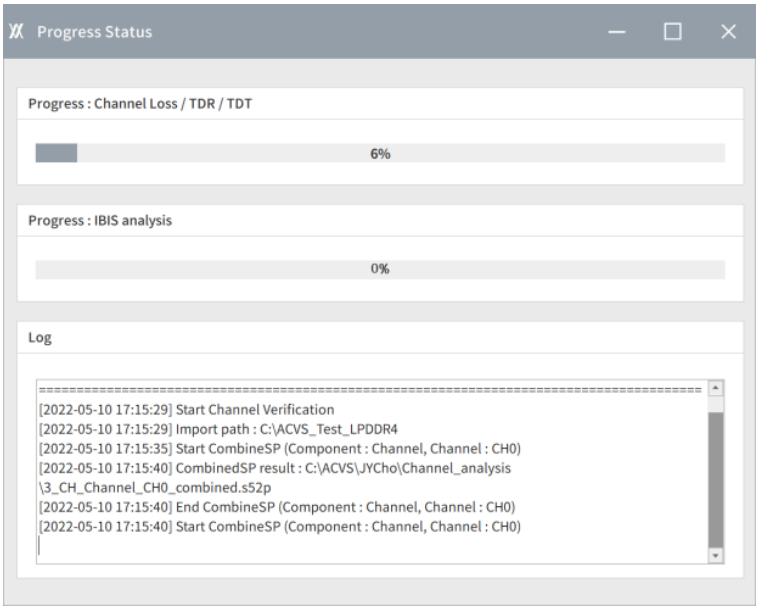


Figure 55. ACVS Analysis progress Status

2.3.4. ACVS Ch. Verification Report

2.3.4.1. Full Ch. Basic SI report and Output

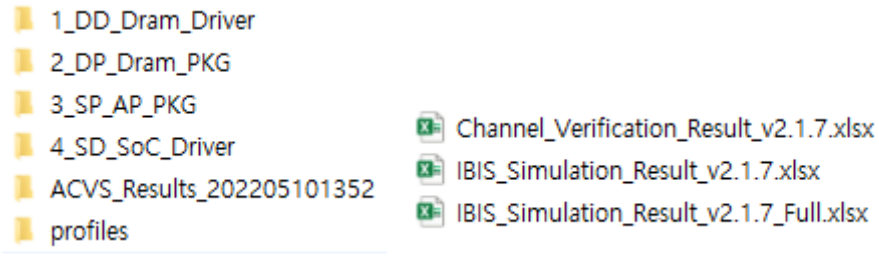


Figure 56. ACVS Results

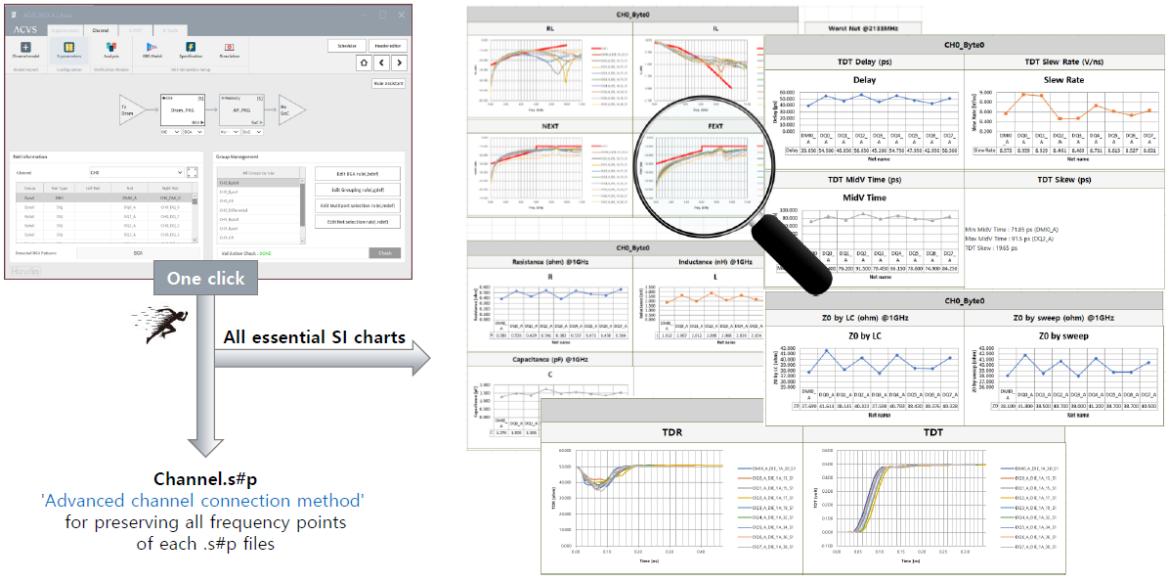


Figure 57. ACVS Basic SI results and output

ACVS generates automatic reports in Excel format for all SI-related charts and result items with easy setup for the channel S-parameter model. The automatically generated Basic SI result report includes charts for the following results of all channel nets.

- Insertion Loss
- Return Loss
- X-talk (PSNEXT, PSFEXT: Power Sum near-end cross-talk, Power Sim far-end cross-talk)
- Group delay
- RLC extraction
- Z0 estimation

- TDR
- TDT
- Skew

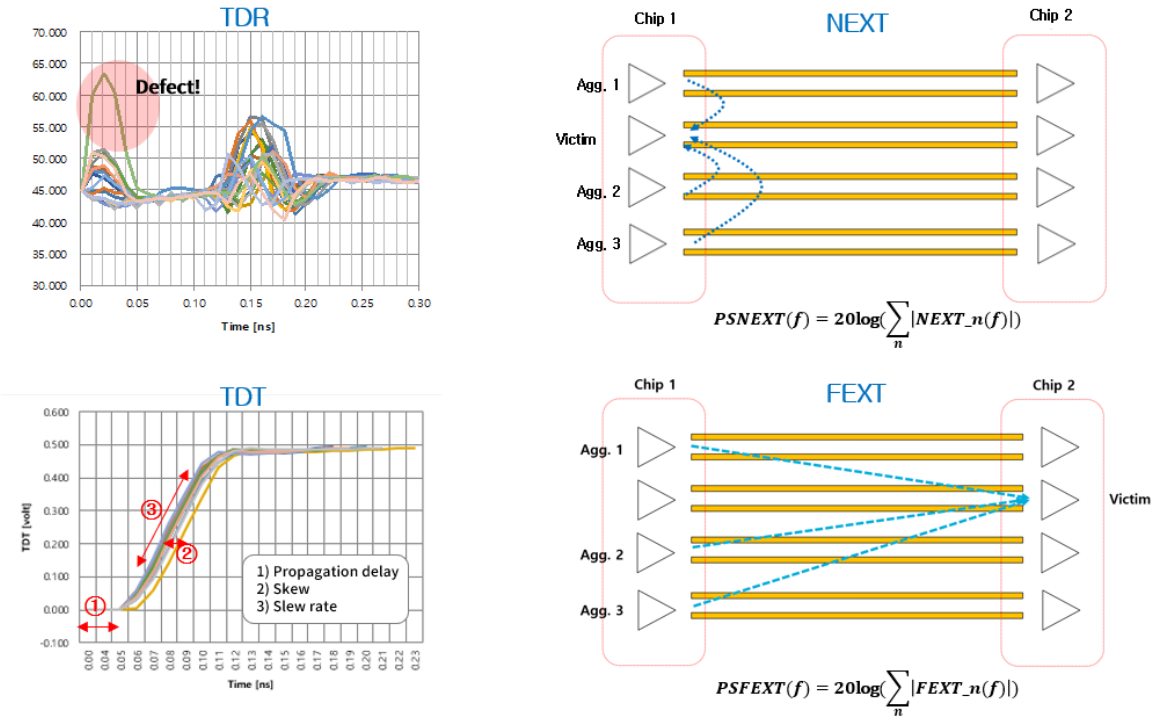


Figure 58. ACVS TDT/TDT results chart and NEXT, FEXT definition

The ACVS Basic SI Report is useful for pre-verification before full transient analysis, and it can be utilized in the following ways:

- PKG all nets model RLC/Z0 pass/fail verification and management
- PKG/PCB all nets model TDR/TDT pass/fail verification
- PKG/PCB model cascading and S-parameter model export applied to Transient signal analysis.
- PKG/PCB all nets model IL/RL/NEXT/FEXT pass/fail verification
- Silicon Interposer all nets model IL/RL/NEXT/FEXT/TDR/TDT pass/fail verification
- Connector model IL/RL/NEXT/FEXT/TDR/TDT pass/fail verification
- Generating SI verification (sign-off) reports for the designed channel model, which can be documented, stored in a database, and shared with relevant stakeholders.

2.3.4.2. Full Ch. Eye report

ACVS automatically generates Memory-IBIS (Eye) analysis reports for each channel net. These reports come in two versions: one with charts captured as images and the other with raw data linked, allowing you to view the full version with a Chart viewer, as shown in Figure 59.

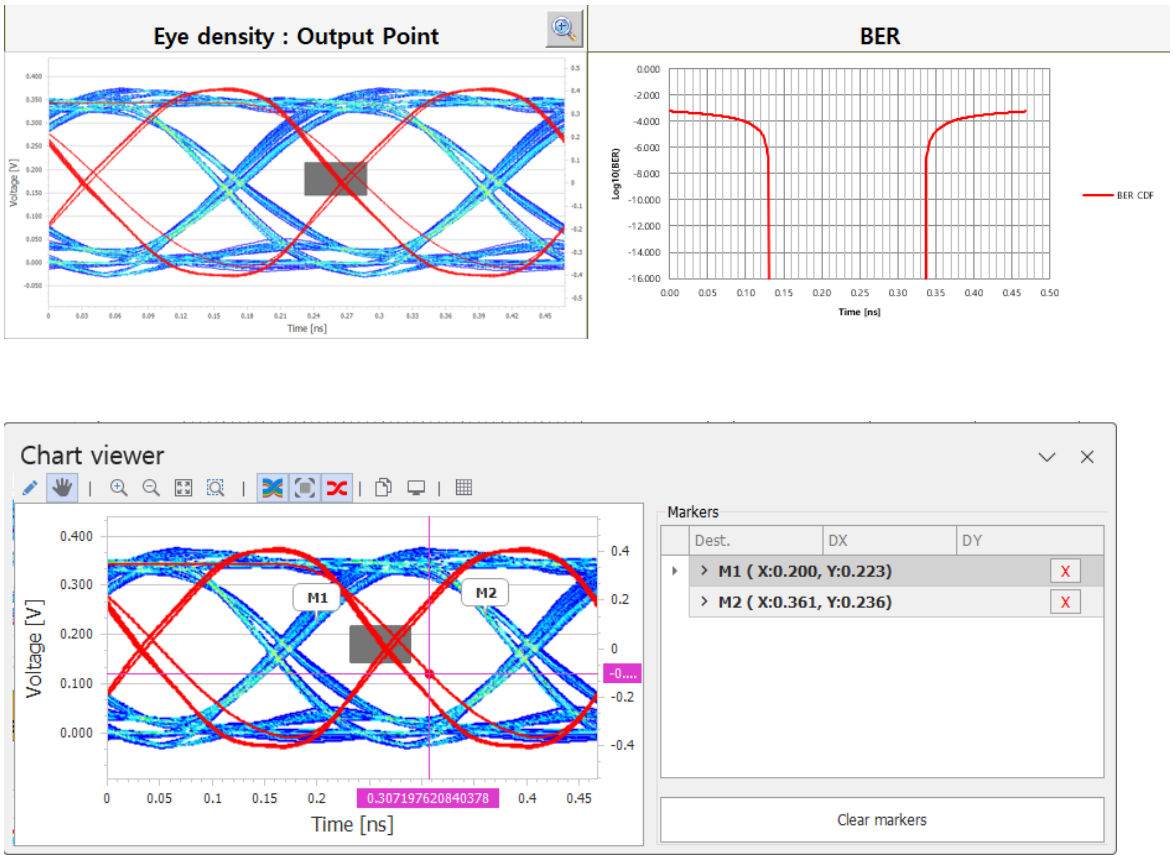


Figure 59. ACVS Eye diagram/BER Chart and Chart viewer

Eye measurements values are automatically compiled into tables for each net, as shown in Figure 60.

Measured Result							
Signal	Eye Width (ps)	Eye Width (UI)	Eye Width margin (ps)	Eye Width margin (UI)	Eye Height (mV)	Eye Height margin (mV)	Eye Vref. (mV)
DRAML_DM_DBI0	175.340	74.800%	119.081	50.800%	193.748	123.748	180.116
DRAML_DQ0	**169.714**	**72.400%**	**113.455**	**48.400%**	**196.250**	**126.250**	**180.116**
DRAML_DQ1	175.340	74.800%	119.081	50.800%	261.019	191.019	180.116
DRAML_DQ2	173.465	74.000%	117.206	50.000%	239.990	169.990	180.116
DRAML_DQ3	172.527	73.600%	116.268	49.600%	253.931	183.931	180.116
DRAML_DQ4	166.901	71.200%	110.642	47.200%	157.030	87.030	180.116
DRAML_DQ5	172.527	73.600%	116.268	49.600%	225.344	155.344	180.116
DRAML_DQ6	172.527	73.600%	116.268	49.600%	187.472	117.472	180.116
DRAML_DQ7	168.776	72.000%	112.518	48.000%	178.808	108.808	180.116

Figure 60. ACVS Measured Eye results

ACVS provides Eye results for cases where PAM4 modulation is applied, as shown in Figure 61.

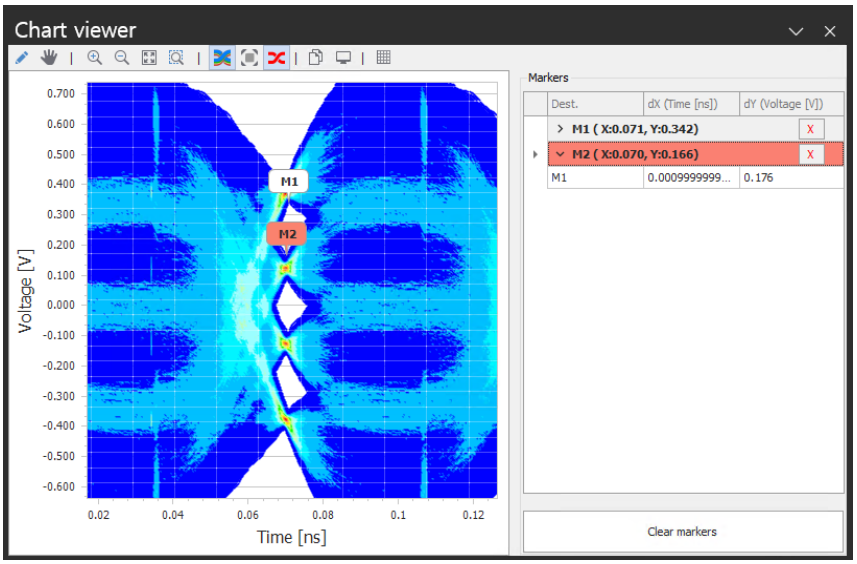


Figure 61. ACVS PAM4(Modulation Levels =4) signal wave form view

2.3.4.3. ChartNX

ChartNX is a standalone chart tool within ACVS that allows users to directly create, measure, and edit charts based on ACVS analysis results. It inherits the strengths of chart tools integrated into traditional circuit simulators while addressing their limitations, offering a more specialized and advanced charting solution for the Signal/Power Integrity. Chart projects configured by users can be saved, managed, and shared, enhancing efficiency in collaboration across departments and organizations.

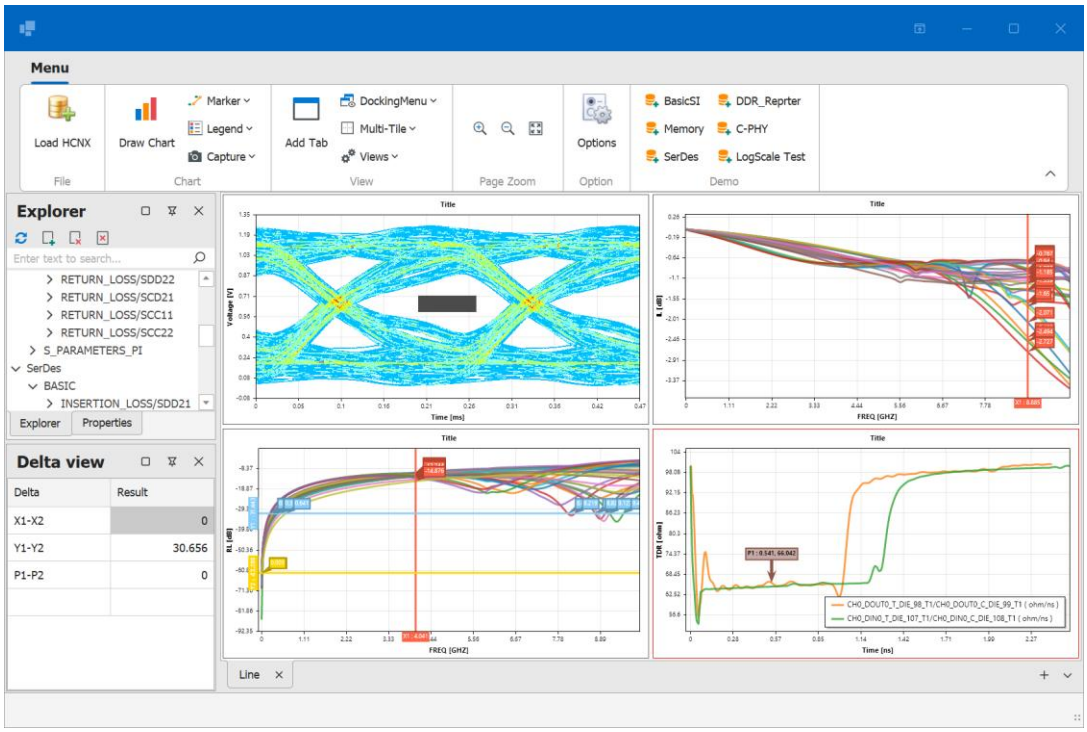


Figure 62. ChartNX: The Advanced and Innovative Standalone Charting Tool

2.4. * snpview.com

www.snpview.com is a web-based, free S-parameter view and simulation platform that incorporates some of Huwin ACVS's solver capabilities. It works seamlessly on Google Chrome and Microsoft Edge browsers, but it does not support Internet Explorer.

You can access the website www.snpview.com to load S-parameters without port limitations. However, unlike ACVS, which generates automatic reports for the entire net, snpview.com allows you to select and plot individual nets, perform simulations, and share the results on a per-net basis.

Snpview.com has been optimized to utilize ACVS's SimNX engine in a cloud computing environment. It provides Basic SI and Time Domain simulation results on a net-by-net basis, allowing users to access accurate TDR/TDT/Eye simulation results free of charge. However, due to limitations in the web UI, it does not currently support simulations using users' actual IBIS and IBIS-AMI models. Instead, it offers a feature called ChannelView, which allows users to explore the EQ capabilities of IBIS-AMI models.

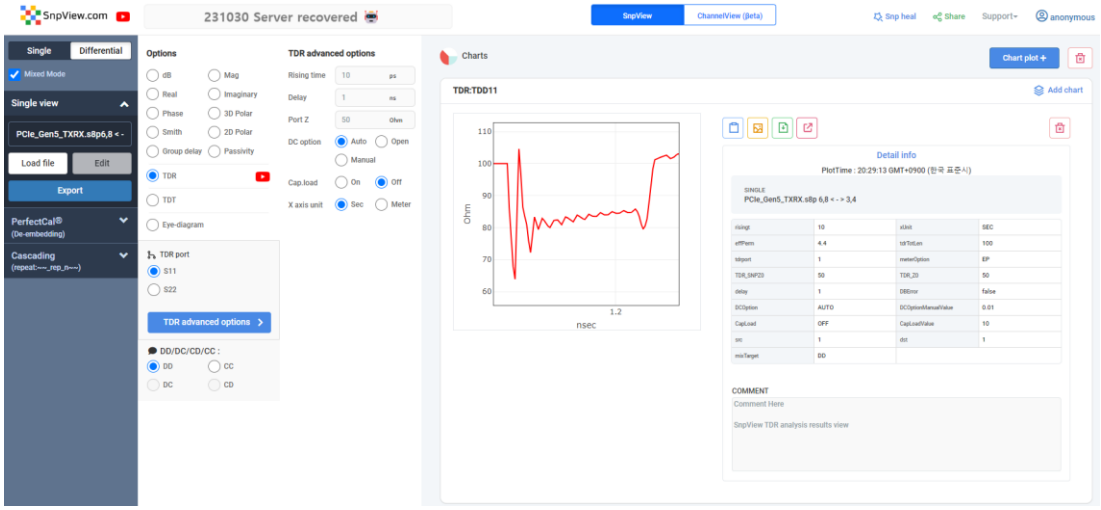


Figure 63. Snpview.com/ SnpView : differential TDR plot example

Additionally, Snpview.com provides an Snp heal feature for S-Parameters, allowing users to enforce causality and passivity in the S-Parameter data.

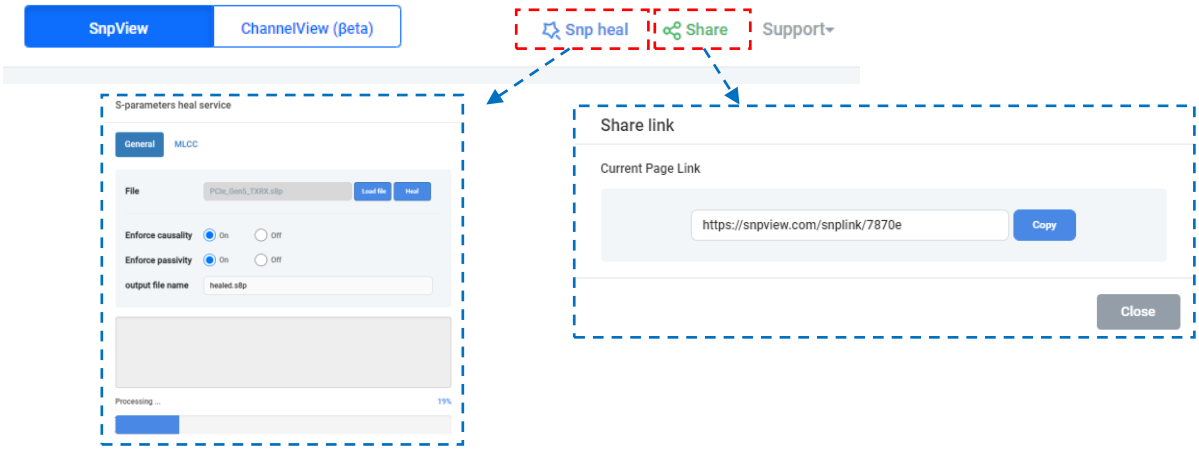


Figure 64. Snpview.com : Snp heal , results/comment view Share

The Share Link feature allows users to share the currently plotted results, comments, and S-Parameters links with other engineers. It enables engineers to share and collaborate on Snpview results and explore additional results by following shared links (Please note that using the Share feature requires logging in with Google Chrome).

Additionally, SnpView has recently introduced the ChannelView feature, which allows users to perform channel simulations for free on the web. This service is currently in beta release, providing users with the capability to simulate channels conveniently through the web interface.

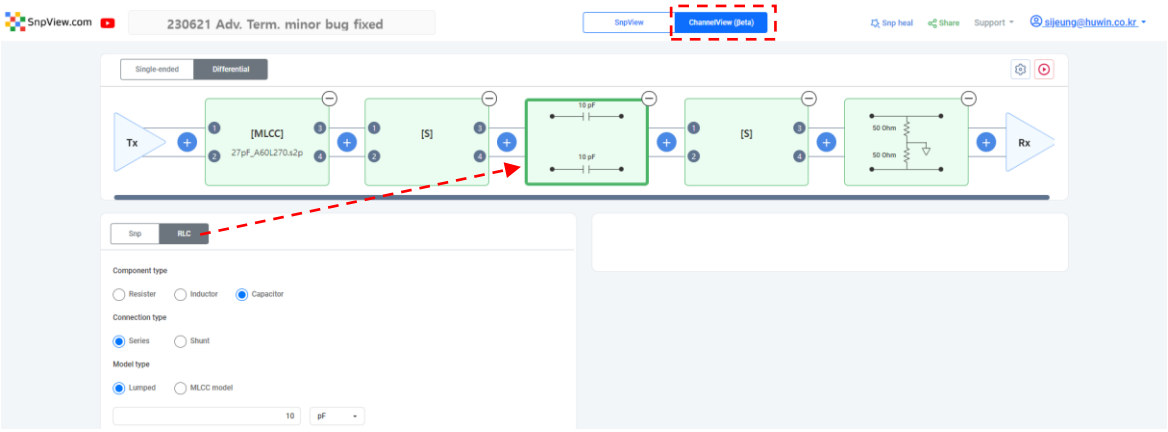


Figure 65. SnpView.com / ChannelView : Ch. Setup (Tx/Snp/RLC/Rx)

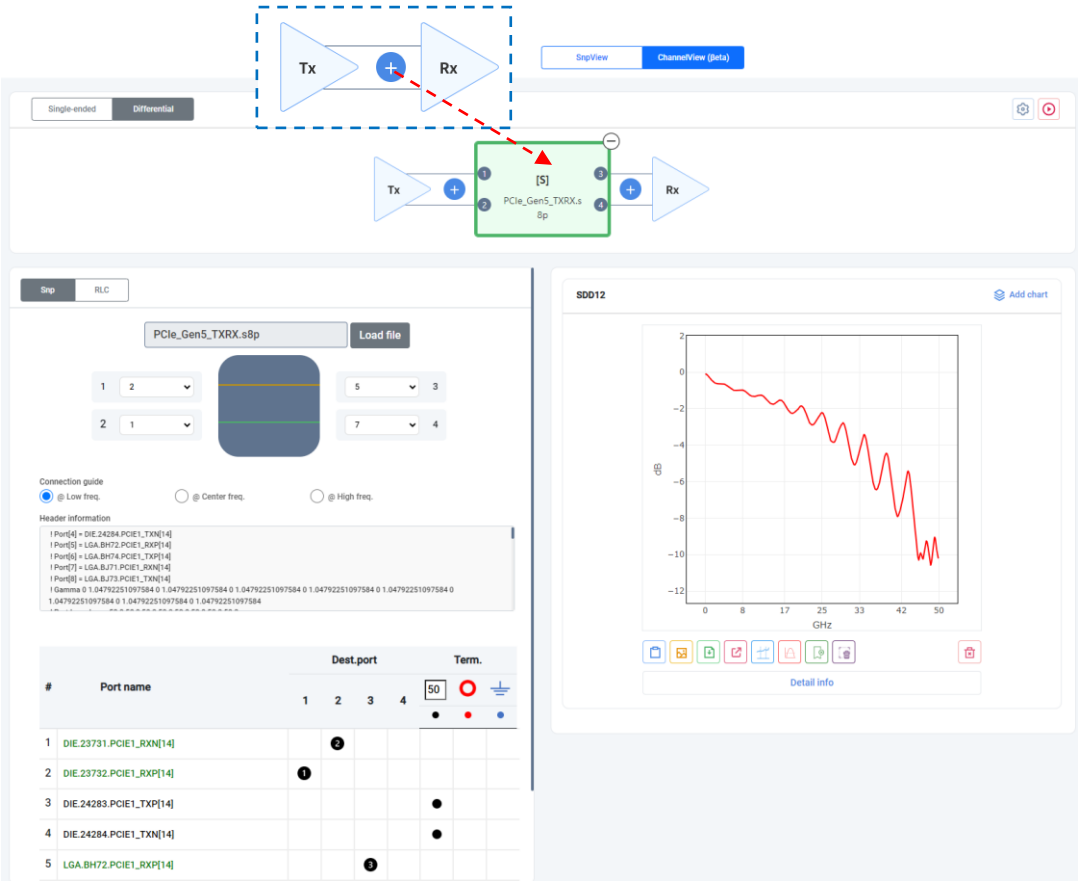


Figure 66. Snpview. com / ChannelView : Ch. S-parameter(Snp) setup

ChannelView allows users to connect components such as direct/parallel RLC or MLCC S-parameters to a channel and view the corresponding Basic/TDR/TDT/Eye analysis results. This feature provides flexibility in simulating and analyzing channel behavior with different components.

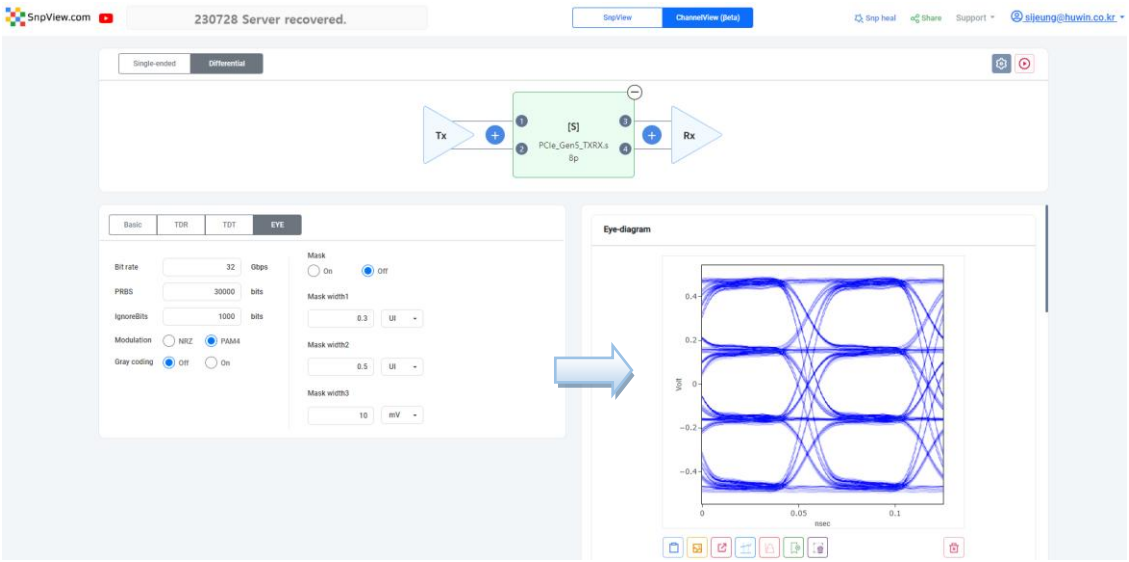


Figure 67. SnpView.com / ChannelView : Ch. Results plot

Additionally, in ChannelView, you can apply Driver, Jitter, and EQ conditions to the Tx and Rx models to observe the Eye results. This allows you to analyze how different driver, jitter, and equalization settings impact the performance of your channel.

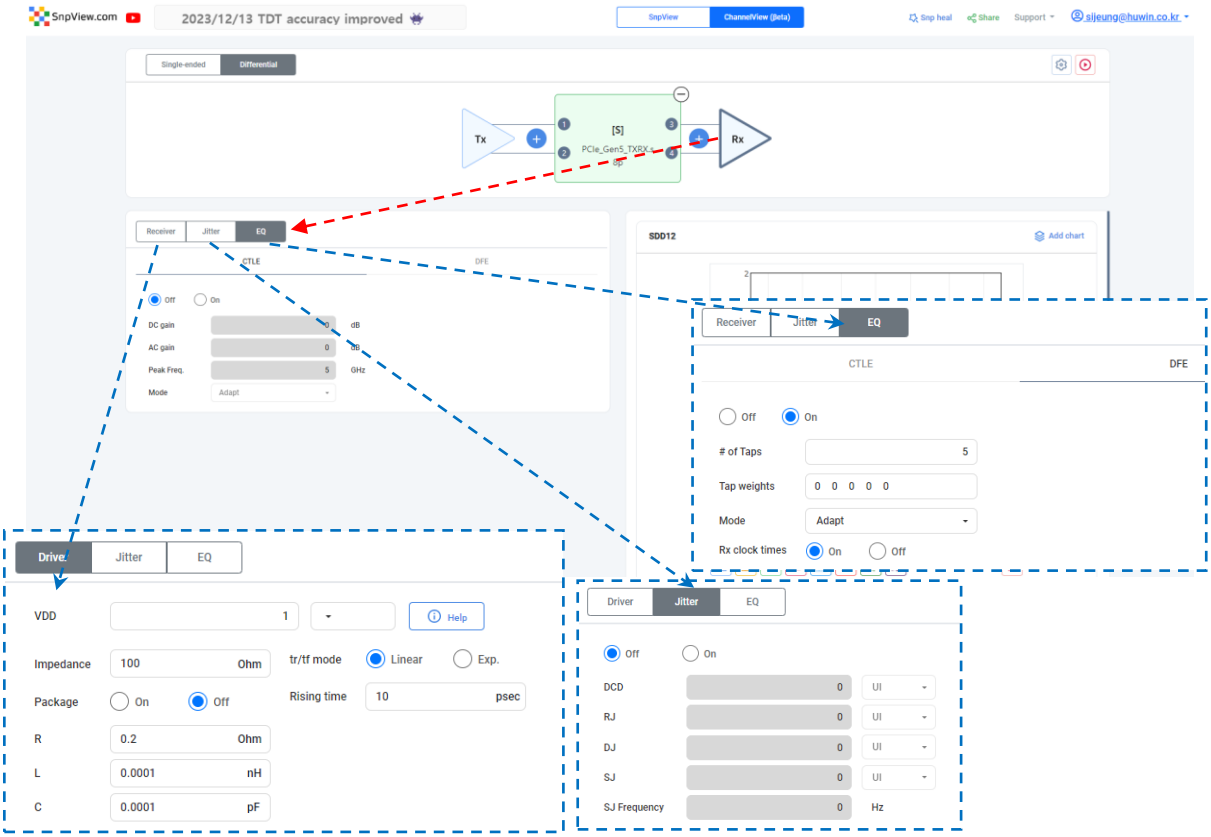


Figure 68. SnpView.com / ChannelView : Tx/Rx Driver/Jitter/EQ setup

SnpView.com also offers a lite version of PerfectCal. This version provides key features of PerfectCal Pro from ACVS, allowing users to check highly accurate results for free. (For more precise de-embedding, we recommend using ACVS PerfectCal Pro.)

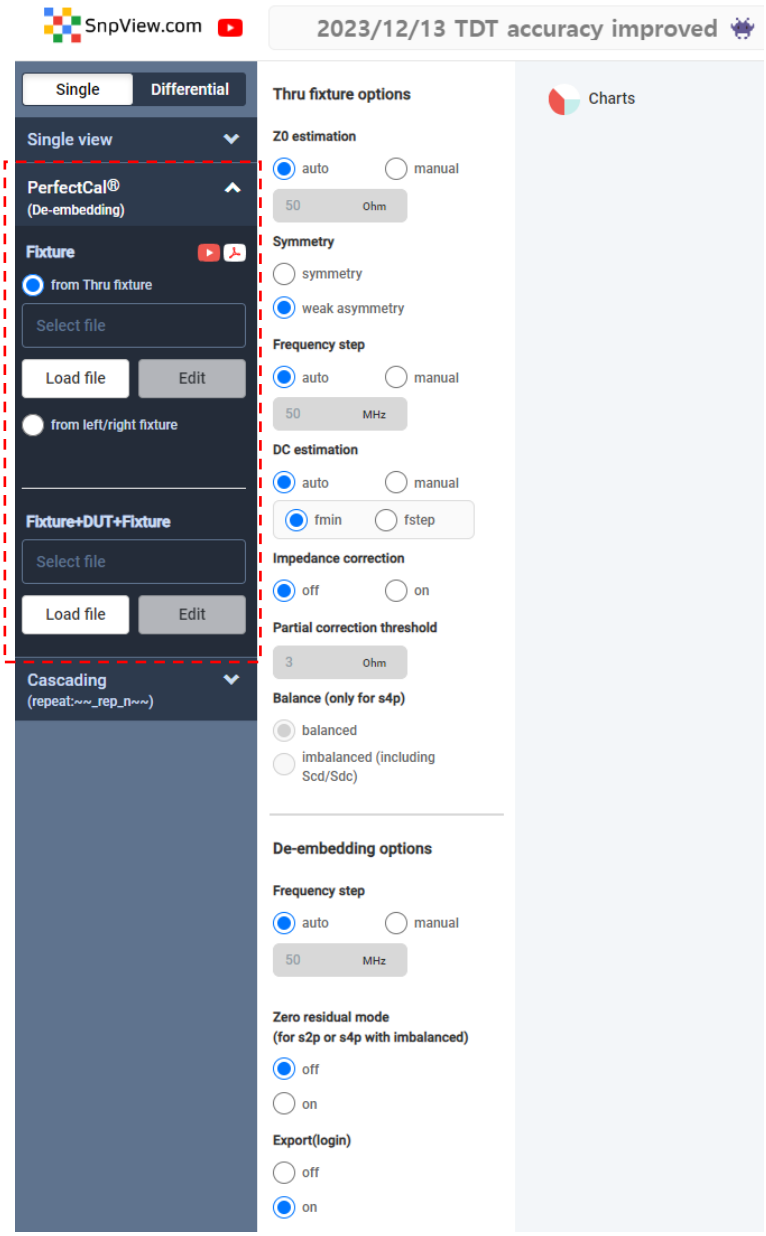


Figure 69. SnpView.com : PerfectCal® -> free Deembedding

2.5. Summary

In the high-performance semiconductor industry, precise EM simulation and advanced system analysis, along with an automated SI verification solution like ACVS (Automated Channel Validation System), are essential for PKG/PCB design processes involving ultra-high-density and high-speed signal channels. ACVS is a specialized SI solution that takes simulation integrity into account. It automates EM simulations to extract ch. S-parameter models and generates automated reports through both Basic SI and Advanced SI analysis for the advanced channel systems. The conducted analyses can accurately verify compliance (Pass/Fail) that meets the requirements of the latest high-speed data transmission standards, all within a short time span. This significantly improves efficiency during multiple design revision cycles, enabling successful operation even at first fab-out versions, and increases its competitiveness within the market of high-performance chip designs.

2.6. Reference

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[5] JESD79-5, JEDEC Standard, DDR5 SDRAM

[6] JESD250C, JEDEC Standard, Graphics Double Data Rate (GDDR6) SGRAM Standard

[7] UCIe_1p0_with_legal_disclaimer_July_26th_2022.pdf, Universal Chiplet Interconnect Express (UCIe)

[8] https://www.uciexpress.org/