Tips & Solution Seminar :

# SerDes/DDR Memory Tips & Solutions

## "Gen5,6급 SerDes 와 Memory Ch. 검증 및 최적화 시뮬레이션, 측정 기법"

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## Contents :

5 Generation

ANSYS Electronics 이용한 3D EM 모델링 / 분석

Huwin ACVS 이용한 Channel 검증

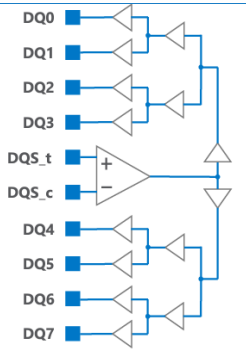
# SerDes/DDR Memory Tips & Solutions

## 5Generation : ~50GHz ->

Expected to implement equalization

- PCIe Gen6, USB4, 100G per-lane Ethernet and OIF/CEI
- DDR5, GDDR6, C-PHY

SimX

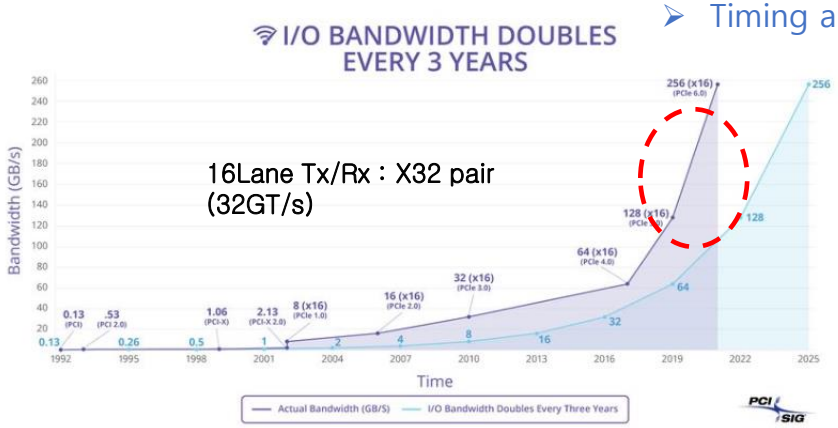



New simulation techniques required

- Statistical analysis to predict behavior over millions of bits
- IBIS-AMI can be used to model the equalization

Forwarded clock problem

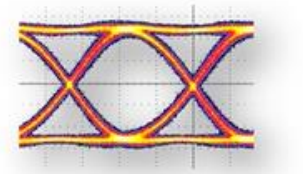
- Timing and voltage margins are specified at an extremely low BER(1E-16)




| 버전 | 날짜 | | 인코딩 | 데이터 전송률 | 대역폭 | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 발표 | 적용 | | | 1레인 (×1) | 2레인 (×2) | 4레인 (×4) | 8레인 (×8) | 16레인 (×16) |
| 1.0~1.1 | 2003년 | 2004년 | 8b/10b | 2.5 GT/s | 250 MB/s | 500 MB/s | 1 GB/s | 2 GB/s | 4 GB/s |
| 2.0~2.1 | 2007년 1월 | 2007년 8월 | 8b/10b | 5 GT/s | 500 MB/s | 1 GB/s | 2 GB/s | 4 GB/s | 8 GB/s |
| 3.0~3.1 | 2010년 11월 | 2012년 1월 | 128b/130b | 8 GT/s | 984.6 MB/s | 1.97 GB/s | 3.94 GB/s | 7.88 GB/s | 15.75 GB/s |
| 4.0 | 2017년 6월 | 2018년 | 128b/130b | 16 GT/s | 1.969 GB/s | 3.94 GB/s | 7.88 GB/s | 15.75 GB/s | 31.51 GB/s |
| 5.0 | 2019년 5월 | 2020년 | 128b/130b | 32 GT/s | 3.938 GB/s | 7.88 GB/s | 15.75 GB/s | 31.51 GB/s | 63 GB/s |
| 6.0 | 2021년 예정 | 미정 | 128b/130b | 64 GT/s | 8 GB/s | 16 GB/s | 32 GB/s | 64 GB/s | 128 GB/s |

64Gbps (16ps UI), S-para.로 정확한 BER ?

HawkEye







PCIE GEN5 Channel Topology

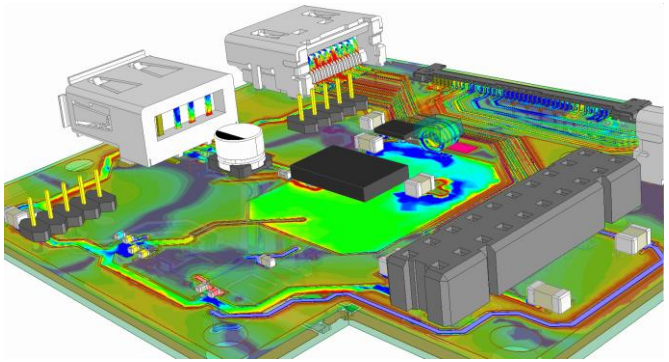
* 그림출처 : Y. L. (Nvidia), Y. H. (Amphenol), "PCIe Gen. 5 CEM Connector and Add-In Card PCB Design Optimizations"', DesignCon 2019

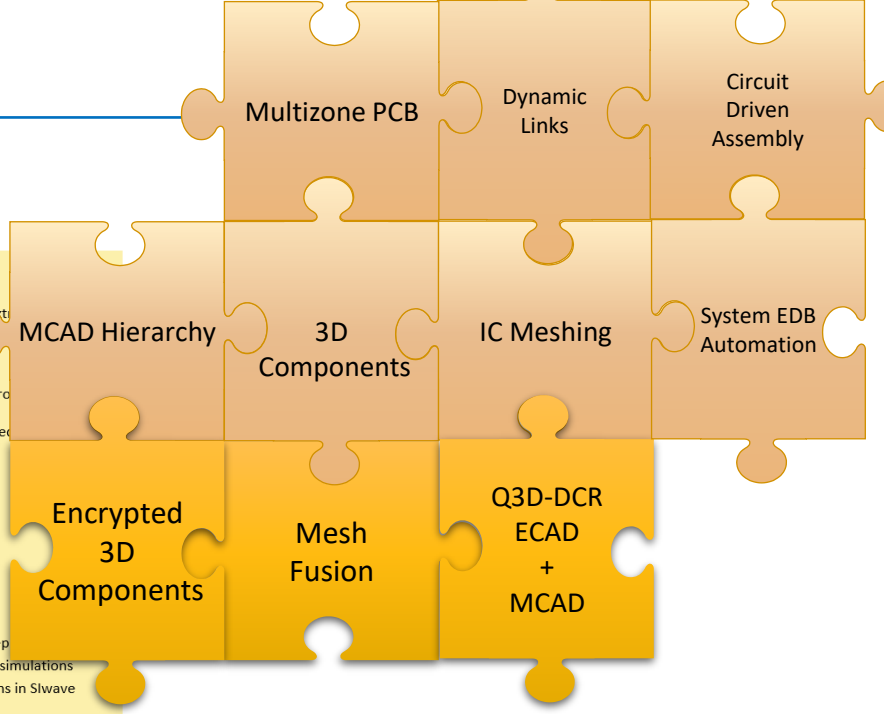
# SerDes/DDR Memory Tips & Solutions

## 3D EM Modeling :

### Ansys HFSS HPC: Two+ Decades of Innovations

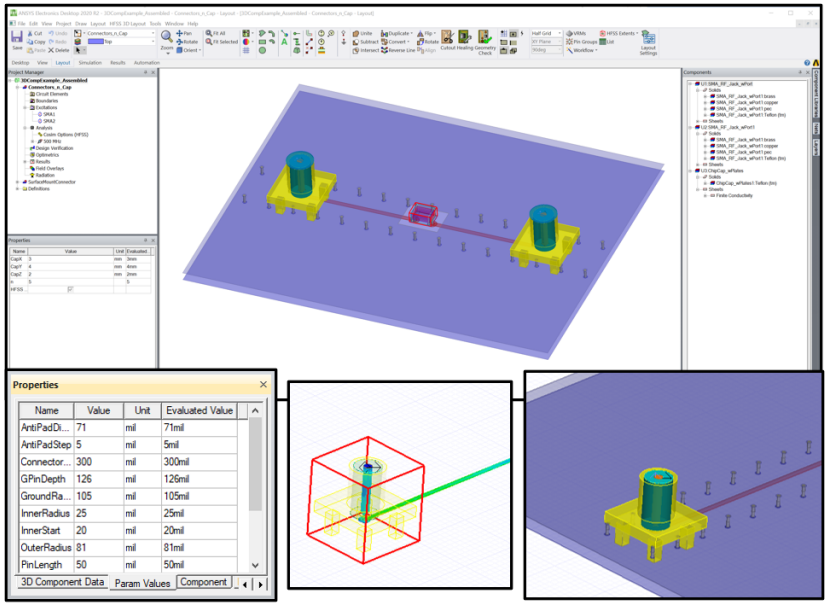
- **1990 HFSS v1.0**
  - Automatic adaptive meshing
  - Gold standard accuracy and reliability
- 1999 HFSS v7
  - Matrix multi-processing
- 2005 HFSS v10
  - Spectral Decomposition Method (SDM), for parallel frequency points
  - Distributed Solve Option (DSO), for parallel design points
- 2007 HFSS v11
  - Iterative matrix solver
- 2008 HFSS v12:
  - Domain Decomposition (DDM)
  - Mixed Order Elements
- 2010 HFSS v12.1
  - HFSS-IE solver (3D MoM) with fast ACA solver
  - DDM with Mixed Order Elements
- 2011 HFSS v13
  - Finite Element – Boundary Integral (FEBI)
  - Multi-core TAU Mesher, field recovery, and fields post-processing
  - HFSS Time Domain Solver, DGTD
- 2012 HFSS v14
  - Finite Antenna Array DDM
  - Hybrid FEM-MoM solver
  - HFSS-IE Physical Optics (PO) asymptotic solver
- 2013 HFSS 15.0
  - Improved matrix multiprocessing, up to 2X faster matrix solves
  - Improved parallel frequency sweeps with MPI interconnect
- 2014 HFSS R15.0.3
  - Distributed Matrix solver
  - Hierarchical HPC, Parameter w DDM
  - Geometry-aware Phi mesh, fast meshing for layered media
  - GPU support for HFSS transient
- 2015 HFSS R16
  - Rescale & Nimbix Cloud deployment
  - HFSS Time Domain Solver, FETD
  - Auto-HPC setup
  - HFSS-IE MLFMM Fast Solver
- 2016 HFSS R17
  - Introduction of Savant SBR+ Sc
  - GPU for frequency domain sol
- 2017 HFSS R18
  - Broadband adaptive meshing
  - S-parameter only solve, 90% faste
  - Multi-level HPC, Parameters-Fre
- 2018 HFSS R19
  - Improved GPU for FD, up to 50% impro matrix acceleration
  - HFSS SBR+ GPU support, up to 5x spee antenna placement studies
- 2019 HFSS 2019R2
  - Microsoft Azure Cloud Deployment
  - Fast HFSS Solve auto-setup option
- 2019 HFSS 2019R3
  - Multi-cell 3D Component Array DDM
- **2020 HFSS 2020R1**
  - Improved distributed frequency sweep
  - Improved GPU performance for SI/PI simulations
  - Improved distribution for HFSS Regions in SIwave





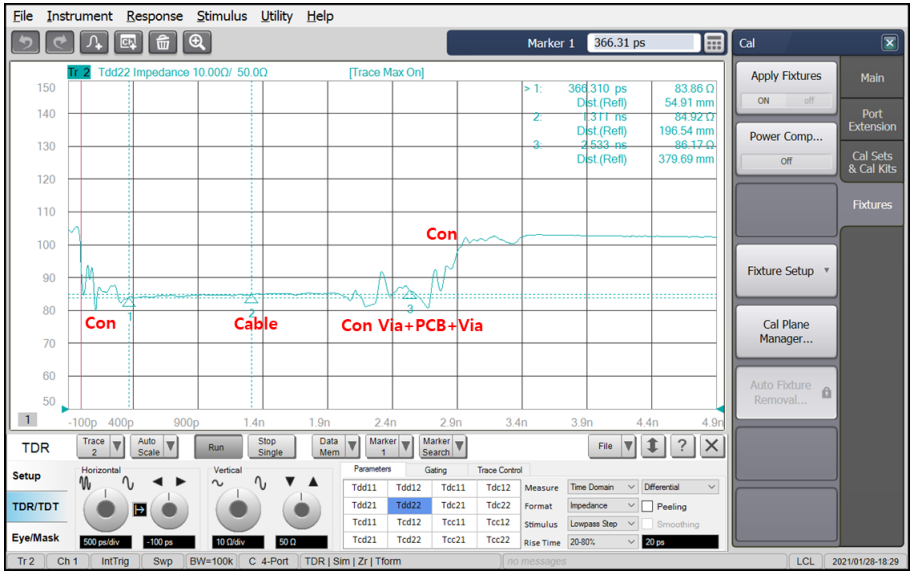

### HFSS 3D Components in Layout

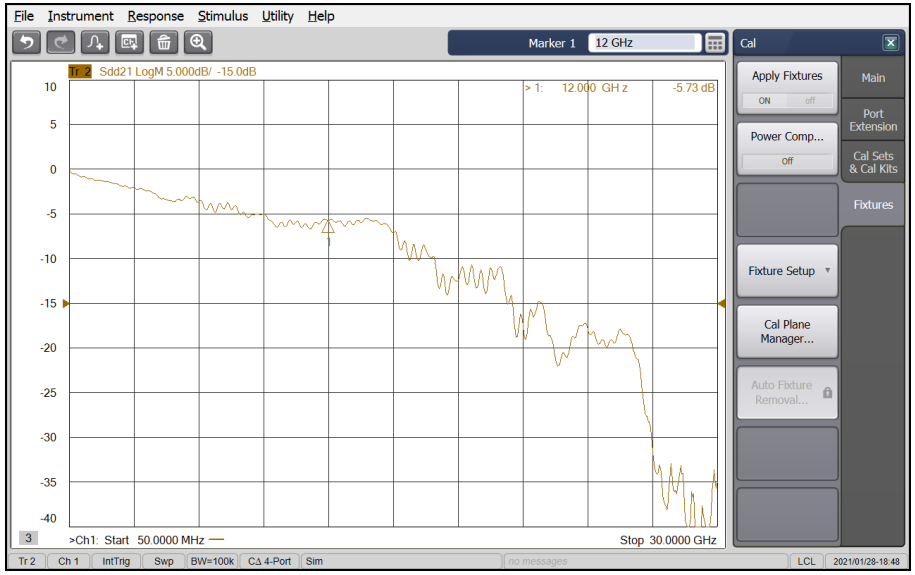
- Direct import
- Parametric support
- Parameterizable
- 3D mesh operation support
- Scripting support
- UI improvements
  - Tree view
  - Menu integration
  - Definition manager
- *Note: encrypted component support available in 2021R1*

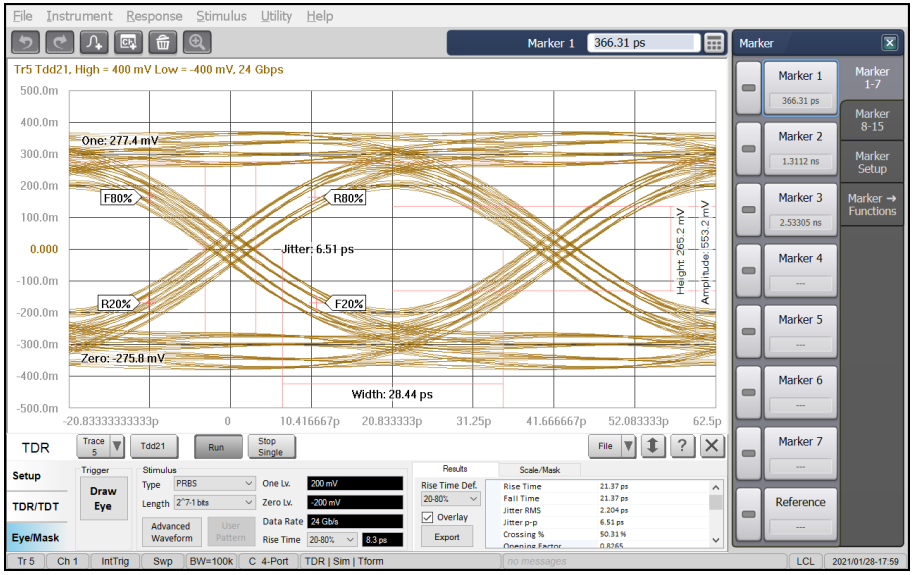


# SerDes/DDR Memory Tips & Solutions

## 측정 & Characterization :



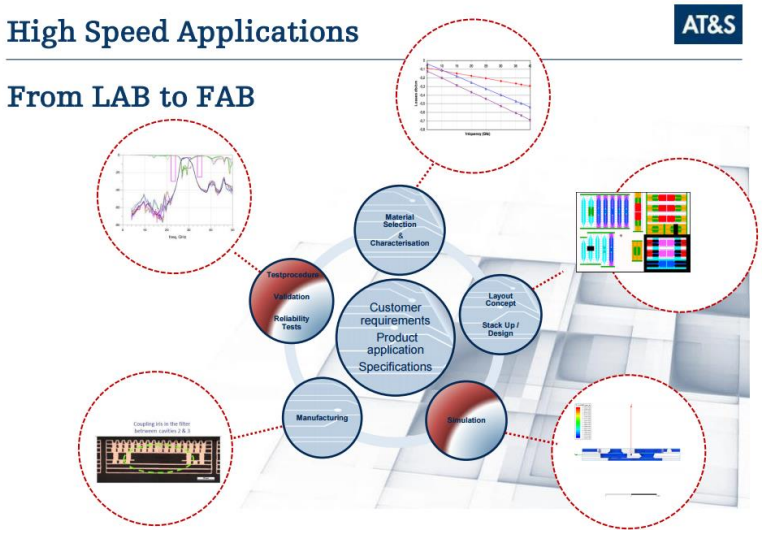



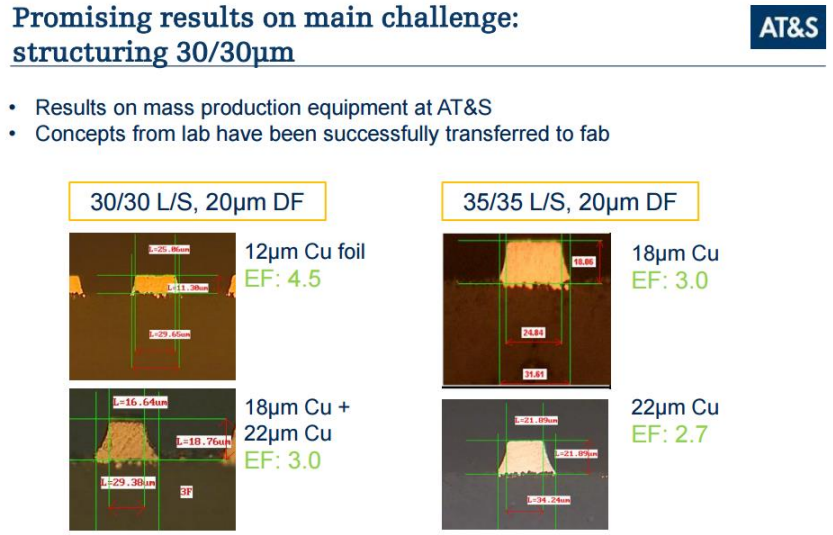
## 측정 & Characterization :

❖ 측정과 해석 결과 차이

- ➢ PCB 원자재의 물성과 실제 제작된 PCB의 유전율의 차이가 존재함
  - ✓ 그 차이가 크지 않지만 TDR 결과 비교시 약간의 delay 차이가 나타남
  - ✓ 접합 PCB의 경우 손실 값의 보상이 필요함

- ➢ 제작된 PCB 형상이 해석과 차이가 존재함
  - ✓ PCB 형상의 에칭 및 표면 거칠기 형상을 trace 부분별로 정확히 반영하기는 어렵고 평균적인 수치를 적용하여 해석 필요(적용 가능하나 효율성이 매우 떨어지고 평균값을 적용해도 오차가 크지 않음)
  - ✓ PCB trace 밀도 또는 곡률 등의 형상에 따라 제조상의 오차가 발생함



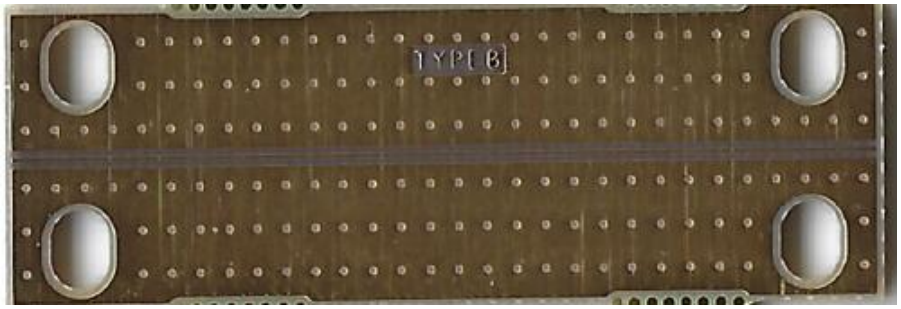
# SerDes/DDR Memory Tips & Solutions

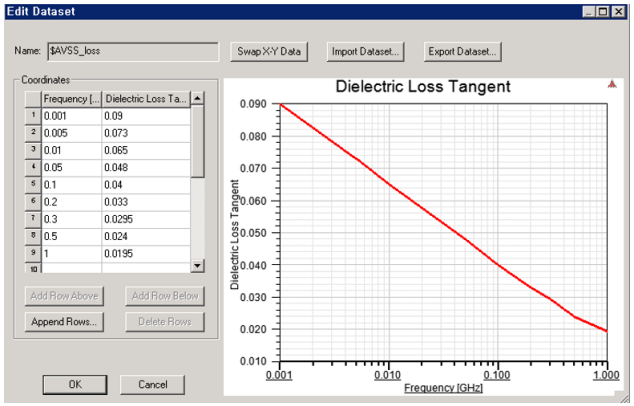
## PCB Materials & Technology :

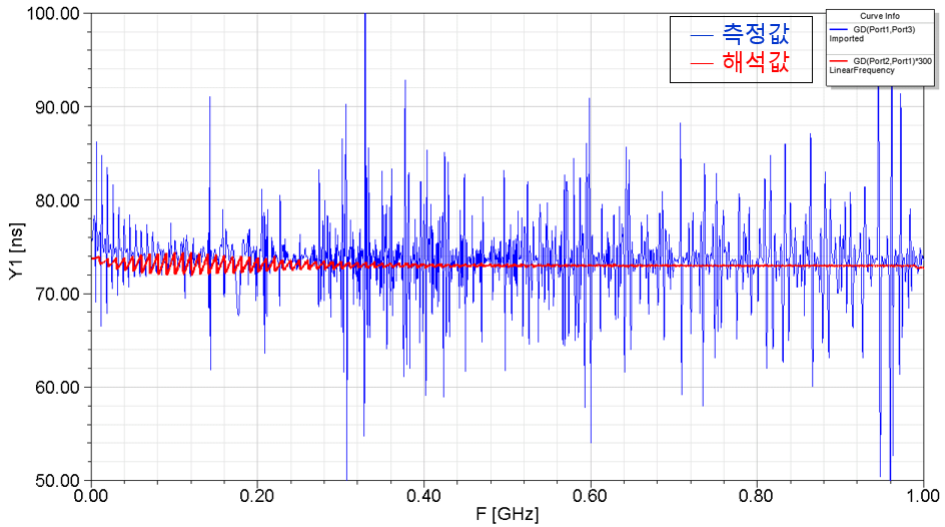
| | | | | | | Frequency | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Supplier | Type | Dk @ 10Ghz | Df @ 10 GHz | Copper Treatment Rz | 5 GHz FR 4 | < 20 GHz Advanced FR4 | < 30 GHz Low Dk Material | 30GHz - 80 GHz Very Low Dk material |
| Materials | Panasonic | R1755M, R1650 | 4,5 | 0,015 | 5-7µm | ☑ | | | |
| | Panasonic | Megtron 2, 4 | 4 | 0,015 | 5-7µm | | ☑ | | |
| | Panasonic | Megtron 6 | 3,5 | 0,004 | 2µm | | | ☑ | |
| | Rogers | RO43XX | 3,6 | 0,0037 | 7-9 µm | | | ☑ | |
| | Rogers | RO 3003 | 3 | 0,0013 | 5-10µm | | | | ☑ |
| | Panasonic | LCP | 3 | 0,001 | 2µm | | | | ☑ |
| | Du Pont | Pyralux TK | 2,5 | 0,002 | 4µm | | | | ☑ |
| | Isola | Astra 3.0 Dk | 3 | 0,0017 | 2µm | | | | ☑ |
| Technology | Connection | PTH´s | | | | ☑ | ☑ | ☑ | ☑ |
| | | Laser Vias | | | | ☑ | ☑ | ☑ | ☑ |
| | | Filled Vias | | | | ☑ | ☑ | ☑ | ☑ |
| | | Deep Drilling | | | | ☑ | ☑ | ☑ | ☑ |
| | Stack up | Homogeneous | | | | ☑ | ☑ | ☑ | ☒ |
| | | Hybrid | | | | not required | not required | ☑ | ☑ |
| | | Asymmetric Hybrid | | | | not required | not required | not required | ☑ |
| | Structuring Process Line / Space Tolerance | Panel Plating | | | | 75µm +/- 20% | 75µm +/- 20% | 75µm +/- 20% | 75µm +/- 20% |
| | | Semi Pattern | | | | 90µm +/- 10 % | 90µm +/- 10 % | 90µm +/- 10 % | 90µm +/- 10 % |
| | | Semi Additiv | | | | 30µm +/- 7 µm | 30µm +/- 7 µm | 30µm +/- 7 µm | 30µm +/- 7 µm |

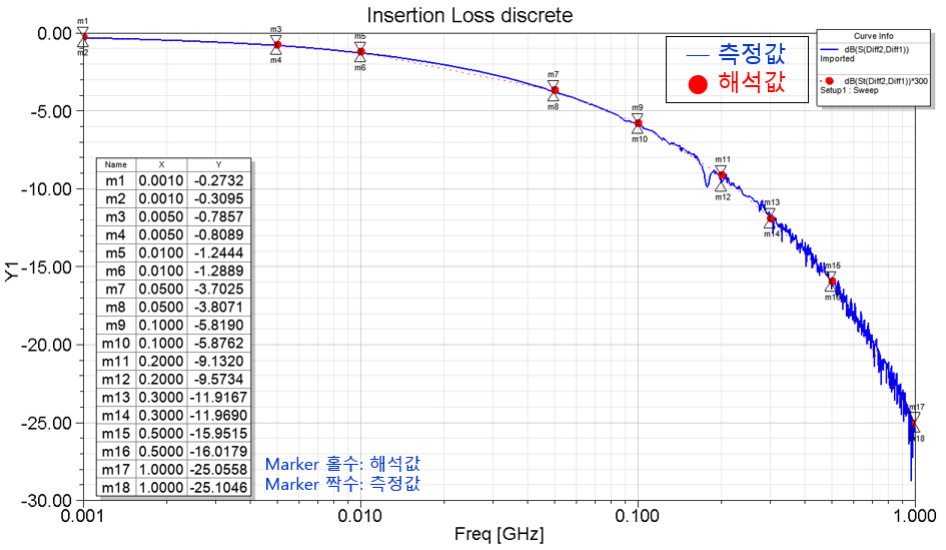
## PCB 측정과 해석 정합성 : PCB 물성 분석

- HFSS 해석에서 사용하는 PCB relative permittivity는 time delay, dielectric loss tangent는 insertion loss를 이용하여 구할 수 있음
- PCB 측정과 해석 결과를 비교하여 유전율과 손실값을 보상함



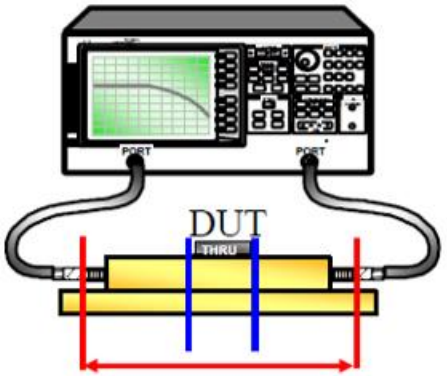



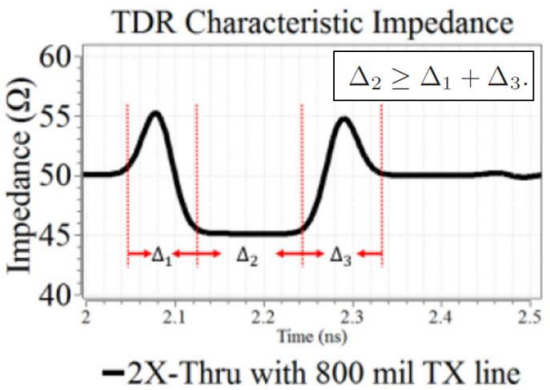




| Name | X | Y |
|---|---|---|
| m1 | 0.0010 | -0.2732 |
| m2 | 0.0010 | -0.3095 |
| m3 | 0.0050 | -0.7857 |
| m4 | 0.0050 | -0.8089 |
| m5 | 0.0100 | -1.2444 |
| m6 | 0.0100 | -1.2889 |
| m7 | 0.0500 | -3.7025 |
| m8 | 0.0500 | -3.8071 |
| m9 | 0.1000 | -5.8190 |
| m10 | 0.1000 | -5.8762 |
| m11 | 0.2000 | -9.1320 |
| m12 | 0.2000 | -9.5734 |
| m13 | 0.3000 | -11.9167 |
| m14 | 0.3000 | -11.9690 |
| m15 | 0.5000 | -15.9515 |
| m16 | 0.5000 | -16.0179 |
| m17 | 1.0000 | -25.0558 |
| m18 | 1.0000 | -25.1046 |

## PCB 측정과 해석 정합성 : De-embedding 필요성 및 원리

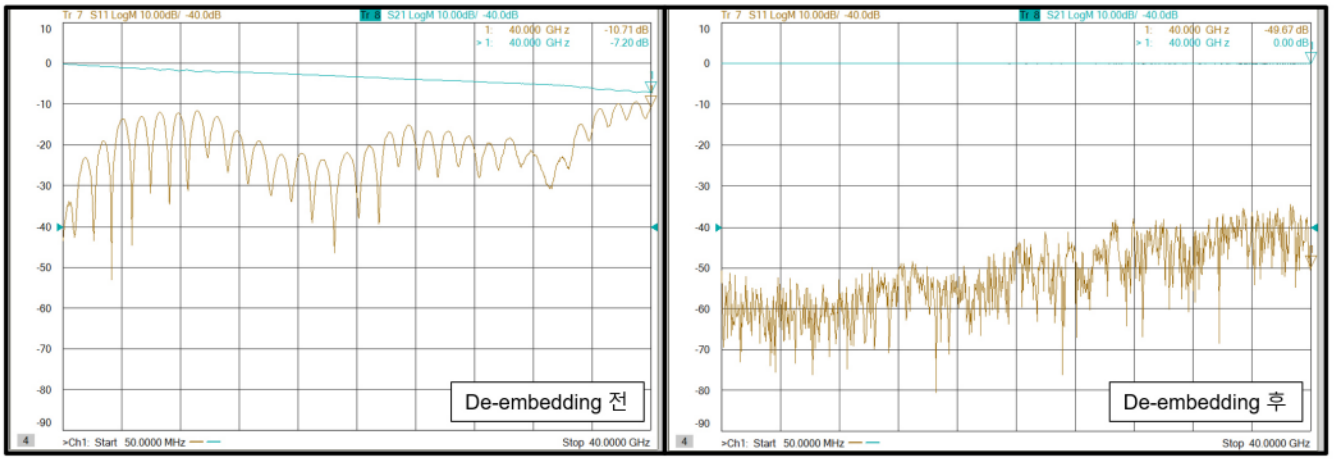
- ❖ DUT를 측정장비와 연결하기 위해 존재하는 PCB 등의 fixture가 필요함
- ❖ DUT가 너무 작은 경우에 측정 probe사이에 coupling이 발생하기 때문에 이격이 필요함
- ❖ Fixture + DUT + fixture 구조에서 양쪽 fixture 특성을 제거하여 DUT 특성을 구함
- ❖ Fixture 두개를 연결한 2X thru를 측정하여 Fixture의 역함수를 구함



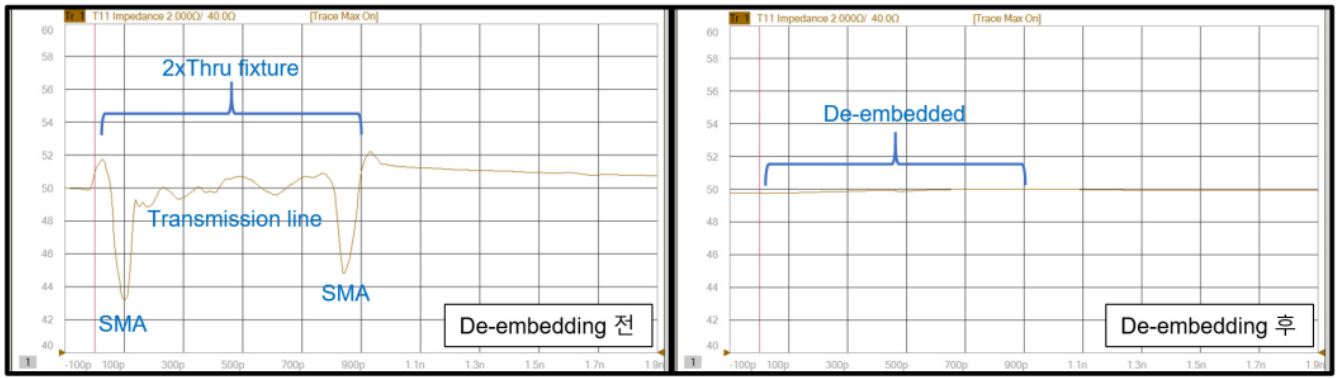



## PCB 측정과 해석 정합성 : 측정 및 성능 분석 사례

❖ 2X thru 측정 결과



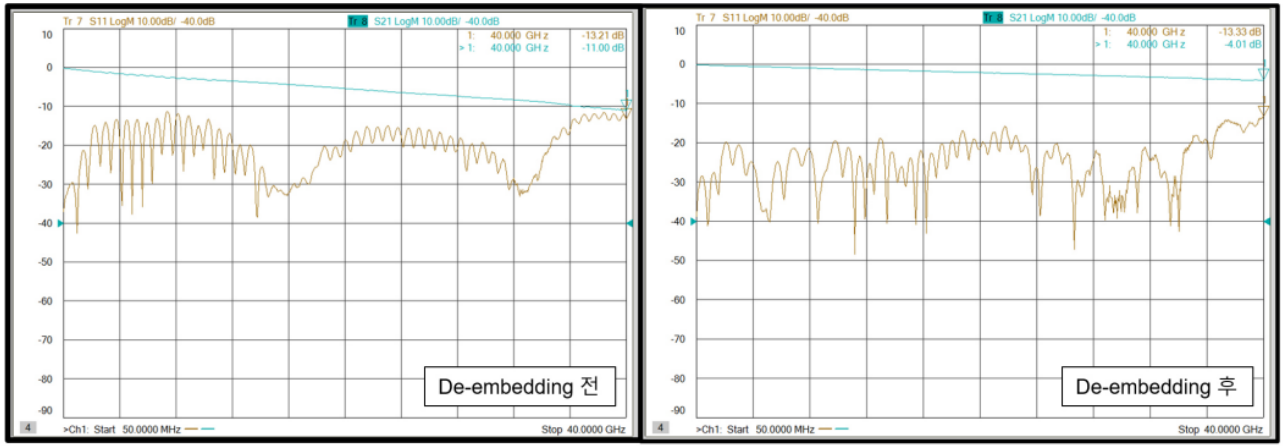

2xThru fixture de-embedding 전후 IL/RL



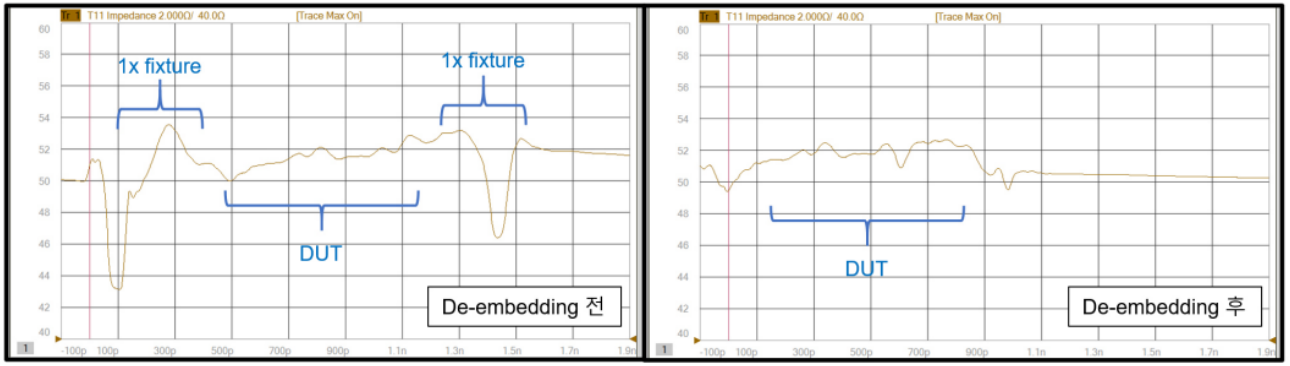

2xThru fixture de-embedding 전후 TDR 결과

## PCB 측정과 해석 정합성 : 측정 및 성능 분석 사례

❖ DUT 측정 결과




Fixture+DUT de-embedding 전후 IL/RL




Fixture+DUT de-embedding 전후 TDR

# ANSYS Electronics
# 3D EM Modeling

**Memory/SerDes 채널 분석/모델링**

HuWin

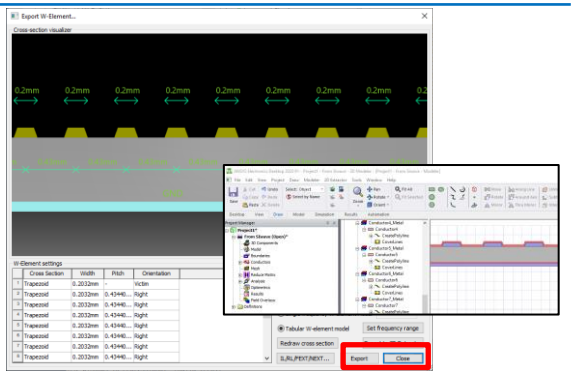
## 3D 해석 필요성

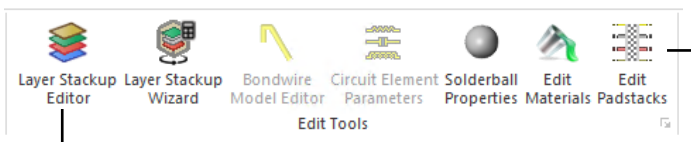
- 최근 고속 신호 전송 채널은 그 크기가 점점 작아지고 있기 때문에 직접 측정이 불가능하고 제조 후 수정이 불가능하여 해석을 이용한 설계의 필요성이 높아짐
- 작아지고 복잡해진 채널은 via, socket, connector 등의 다양한 불연속 인터페이스의 임피던스 매칭과 상호 간섭의 영향을 고려하여 설계되어야 함
- 기존의 각 채널 구성의 S-parameter의 연결로 전체 채널 분석이 불가능하고 3D 해석을 통한 상호 영향성 분석도 필요함
- 모든 채널을 3D 해석을 이용하여 분석하는 것이 가장 정확하지만, 시간 절약을 위해 3D 해석이 필요한 부분을 판단하여 적절히 활용하는 방안이 필요함
- 일반적인 PCB trace는 SIwave가 효과적이고 Package와 같은 PCB의 top에서 bottom으로 연결되는 구조는 HFSS 3D layout, connector 등의 3D 개체를 포함한 부분은 HFSS를 활용하는 것이 효과적인 해석 방법

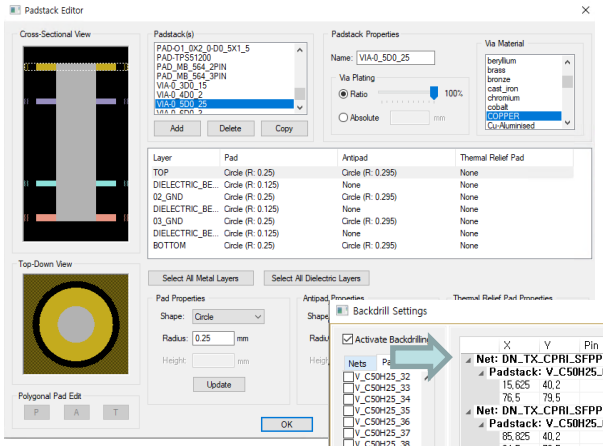
## Stack up 및 via 속성 확인

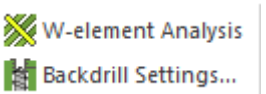
❖ Stack up은 PCB 사양 중 가장 중요한 항목으로 확인 필수
- ➢ HFSS 3D 해석에 필요 없는 layer는 제거하는 방법도 있음

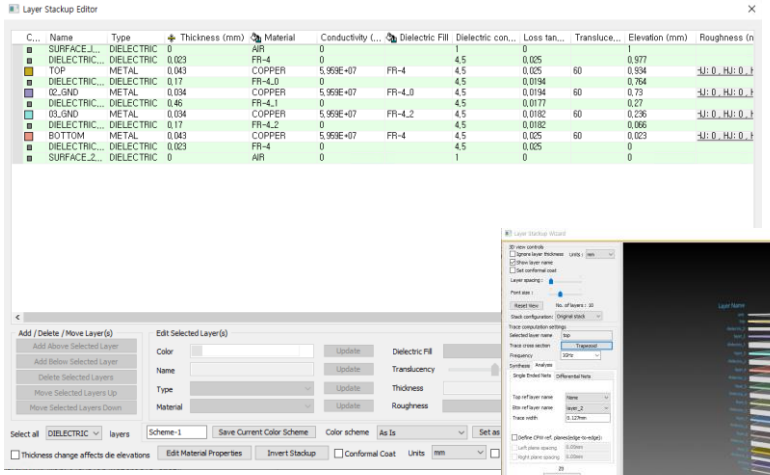
❖ Via 정보는 via 선택 후 Edit Padstacks 클릭하여 확인
- ➢ layout data에 정확히 입력되지 않은 경우가 있기 때문에 확인 필수)

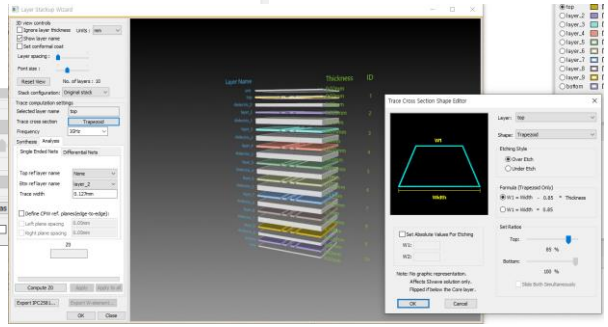


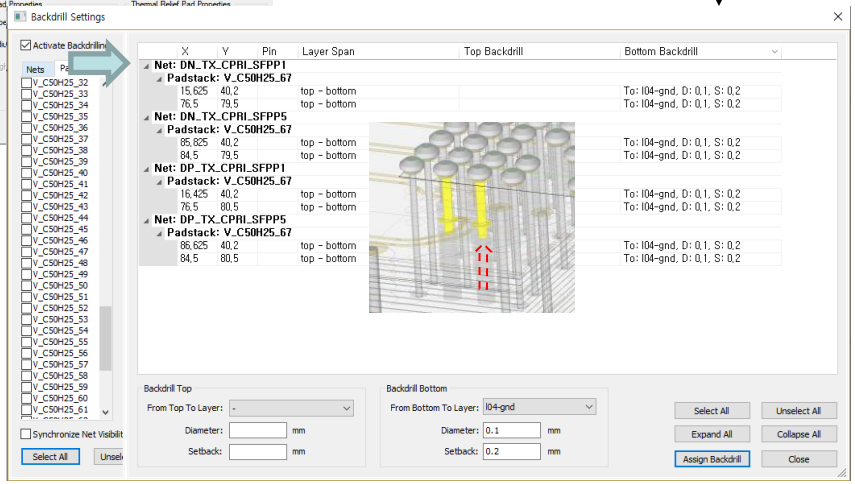




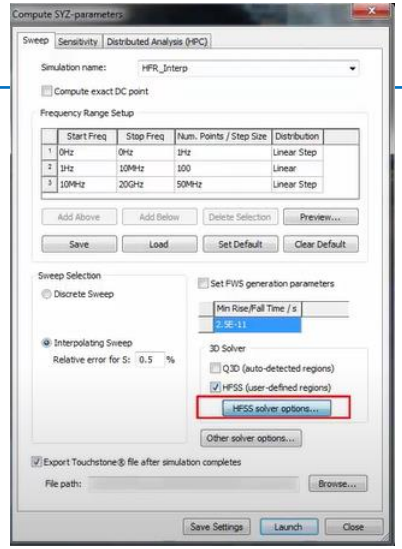

Layer Stackup Wizard

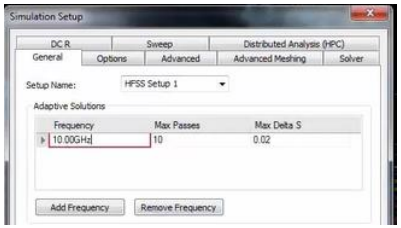
## SIwave와 HFSS 3D layout 연동 해석 : SIwave region 설정

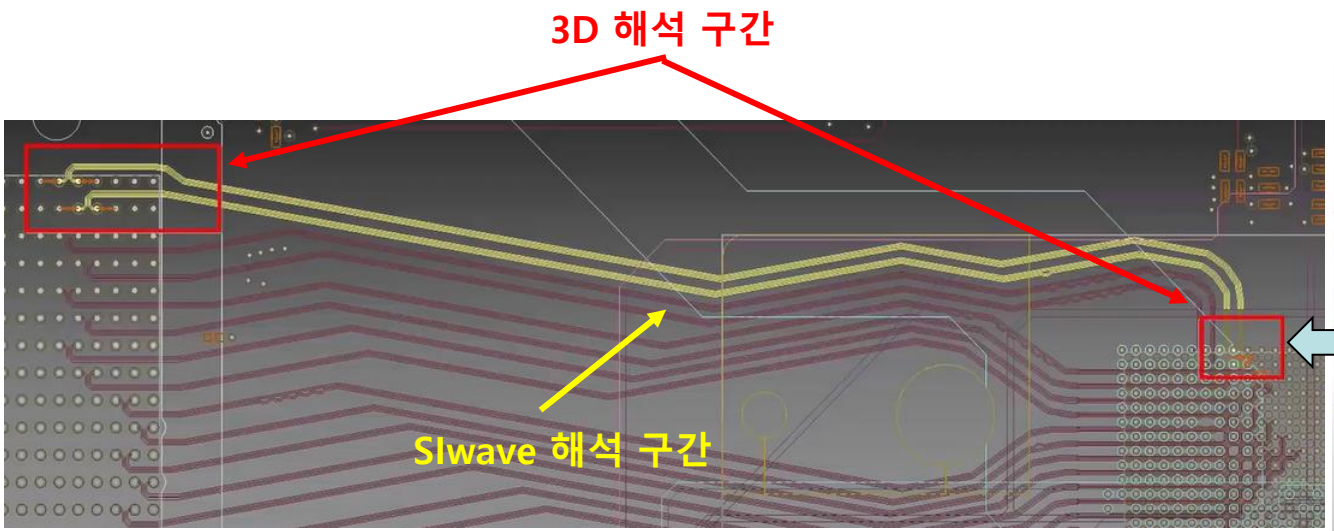
- SIwave는 지정된 region 구간을 HFSS 3D layout로 해석하는 기능을 제공
  - 3D 해석할 구간을 region으로 설정

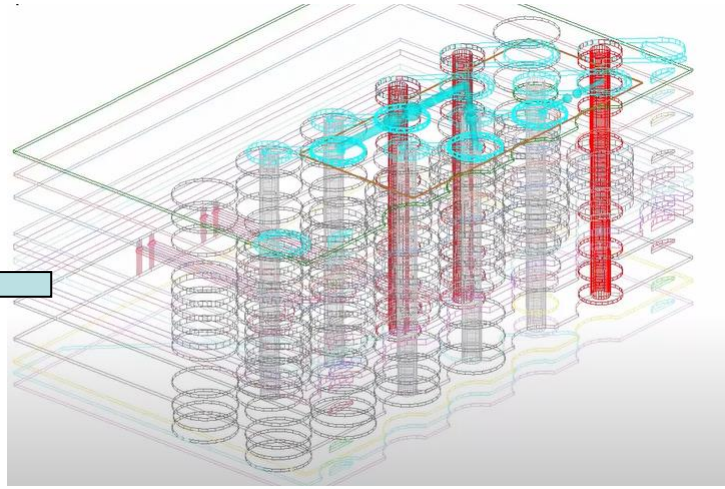
- Region 설정 시 주의 사항
  - Region은 SIwave port를 포함한 구간만 설정 가능
  - 구간 경계면은 HFSS 3D layout port 설정이 가능하도록 경계면에 수직한 reference plane을 포함해야 함

- Region 설정된 구간은 SIwave 결과 폴더의 HF#로 저장됨



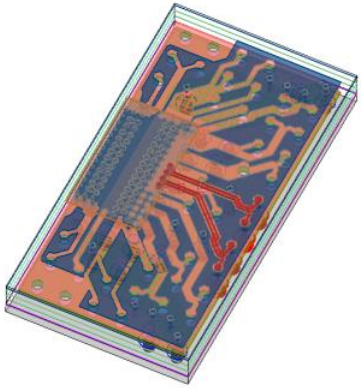



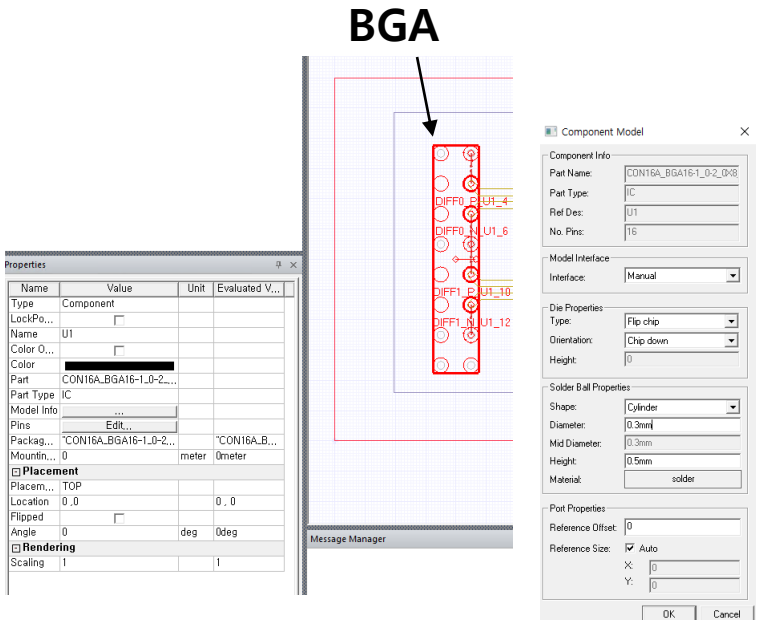



## HFSS 3D layout를 이용한 PCB 해석

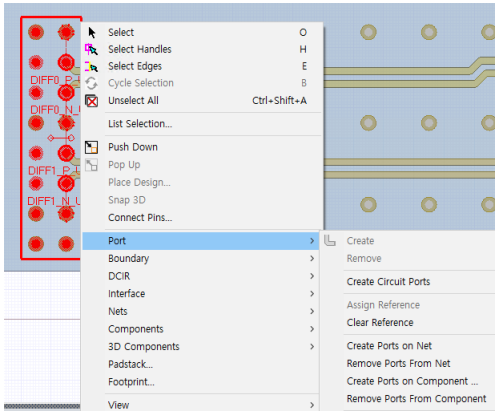
- PCB와 같은 적층 구조 해석은 layer마다 2D triangular mesh를 생성하는 phi meshing 기술이 유용함
- 해석은 HFSS solver을 사용하기 때문에 HFSS와 거의 같은 결과를 나타냄
- Package 와 같이 top에서 bottom으로 연결되는 형태의 해석은 SIwave region 사용이 불가능하기 때문에 3D layout를 추천
- BGA와 die의 solder ball 모델을 지원하고 port 설정도 분석 net만 선택하면 자동으로 생성이 가능하기 때문에 모델링 시간도 절약됨





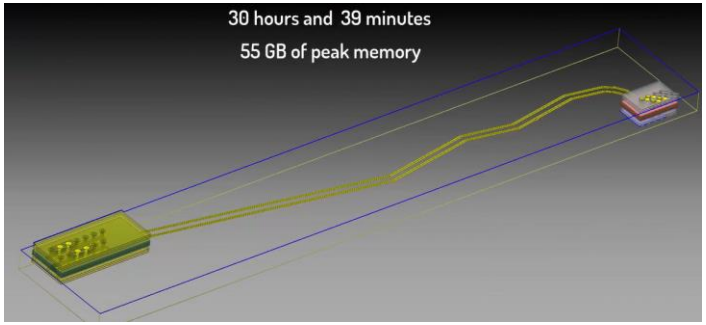






## SIwave 해석 결과 비교: 소요 시간 / 메모리

- Via 부분 해석 결과 차이 있음
- Trace 부분 해석 결과 유사함
- 소요 시간 / 메모리는 큰 차이가 있음
  - SIwave: 10h 39m / 67GB
  - SIwave(Region): 12h 25m / 65GB(88GB)
  - HFSS: 30h 39m / 55GB




SIwave only "Without Regions"

Simulation profile for SIwave_interp

| Module | Real Time | CPU Time | Memory | Size |
|---|---|---|---|---|
| Command | Real Time | Cpu Time | Memory | |
| geomproc | 00:02:15 | 00:02:14 | 1235M | 408982 triangle |
| solve_setup | 00:14:39 | 00:16:40 | 4047M | 1 project |

Finished at 02/23/2018 18:40:47

SIwave 2018.1.0 Feb 22 2018 at 23:48:39 beginning
C:\Program Files\AnsysEM\AnsysEM19.1\Win64\siwave_solver.exe
on at 02/23/2018 18:40:50

| Command | Time | Cpu Time | Memory | Number of Elements |
|---|---|---|---|---|
| geomproc | 00:00:33 | 00:00:33 | 1174M | 425204 triangle |
| xsec_solve | 00:00:59 | 00:21:30 | 7303M | 5163 xsections |
| via_extract | 00:00:38 | 00:19:57 | 7303M | 9380 blocks |
| bsm_adapt | 00:02:41 | 00:02:42 | 7303M | 1861484 triangles |
| Interpolating sweep converged after 205 solutions | | | | |
| DCS_36p | 10:02:29 | 329:03:26 | 67045M | 11974596 matrix |
| SIwave | 00:14:39 | 02:15:44 | 67045M | 11974596 matrix |

Finished on at 02/24/2018 05:02:53

SIwave + HFSS Regions "With Regions"

Simulation profile for HFR_Interp

| Module | Real Time | CPU Time | Memory | Size |
|---|---|---|---|---|
| Command | Real Time | Cpu Time | Memory | |
| HFSS Region 0 | 00:19:12 | 05:54:03 | 86.44GB | 131438 tetrahedra |
| HFSS Region 1 | 00:37:58 | 07:46:15 | 87.98GB | 170648 tetrahedra |
| geomproc | 00:02:30 | 00:02:30 | 1234M | 408984 triangle |
| solve_setup | 00:36:14 | 00:17:18 | 405JM | 1 project |

Finished at 02/22/2018 19:33:34

SIwave 2018.1.0 Feb 19 2018 at 23:50:45 beginning
C:\Program Files\AnsysEM\AnsysEM19.1\Win64\siwave_solver.exe
at 02/22/2018 19:33:37

| Command | Real Time | Cpu Time | Memory | Number of Elements |
|---|---|---|---|---|
| geomproc | 00:00:34 | 00:00:33 | 1174M | 425210 triangle |
| xsec_solve | 00:00:34 | 00:19:20 | 7144M | 5164 xsections |
| via_extract | 00:00:35 | 00:18:21 | 7144M | 9381 blocks |
| bsm_adapt | 00:02:51 | 00:02:51 | 7144M | 1861368 triangles |
| Interpolating sweep converged after 271 solutions | | | | |
| DCS_36p | 10:19:52 | 333:49:40 | 65348M | 11974100 matrix |
| SIwave | 00:14:45 | 02:12:08 | 65348M | 11974100 matrix |

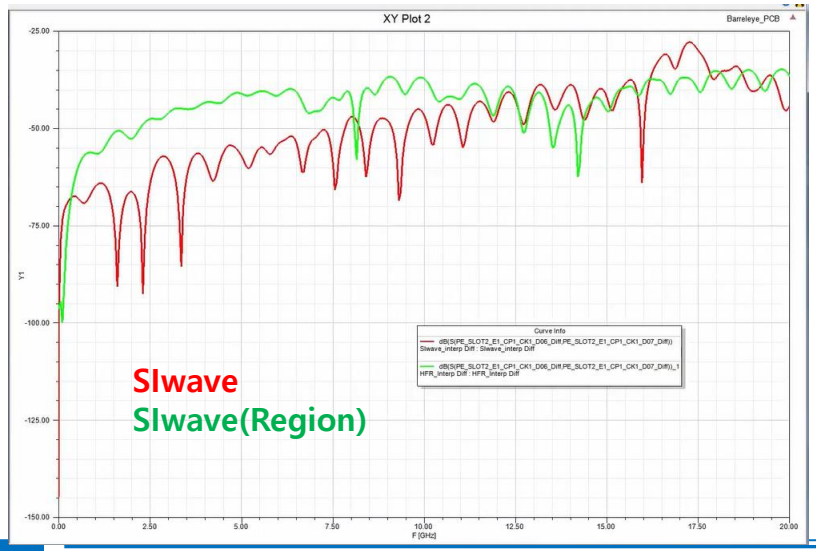
Finished at 02/23/2018 06:22:51

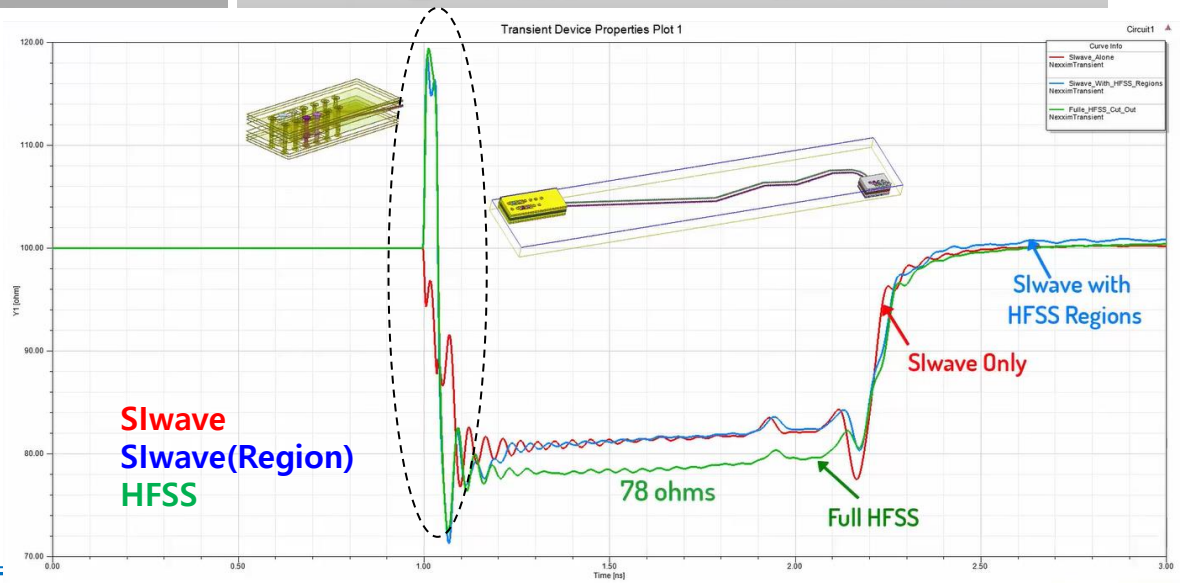
| | | | |
|---|---|---|---|
| Start Date | Feb 23th | Start Time | 18:23:53 |
| End Date | Feb 24th | Finished Time | 05:02:53 |

05:02:53 - 18:23:53 = 10 hours 39 minutes

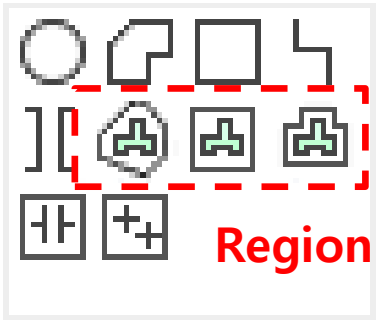
| | | | |
|---|---|---|---|
| Start Date | Feb 22nd | Start Time | 17:57:39 |
| End Date | Feb 23rd | Finished Time | 06:22:51 |

06:22:51 - 17:57:39 = 12 hours 25 minutes

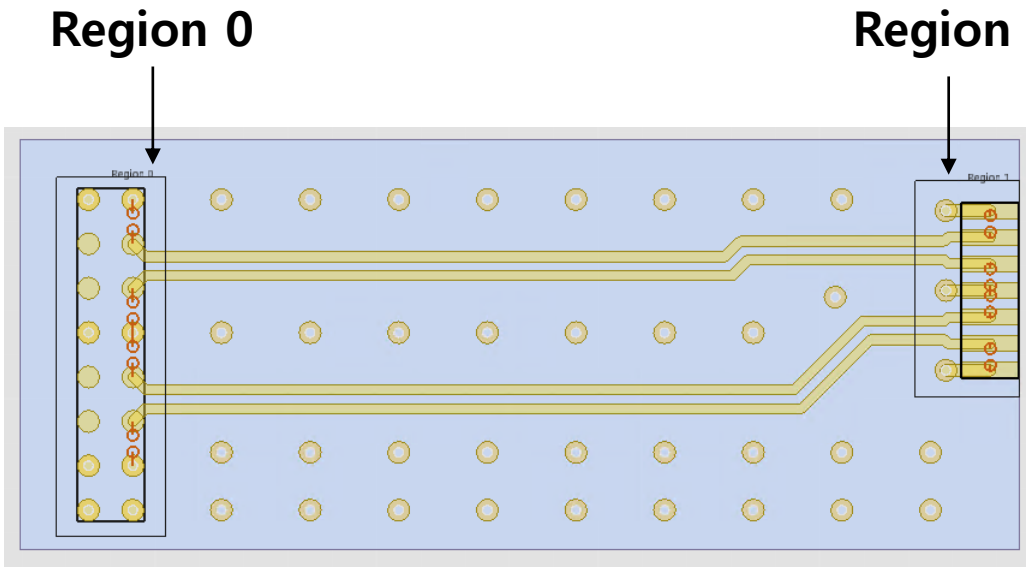


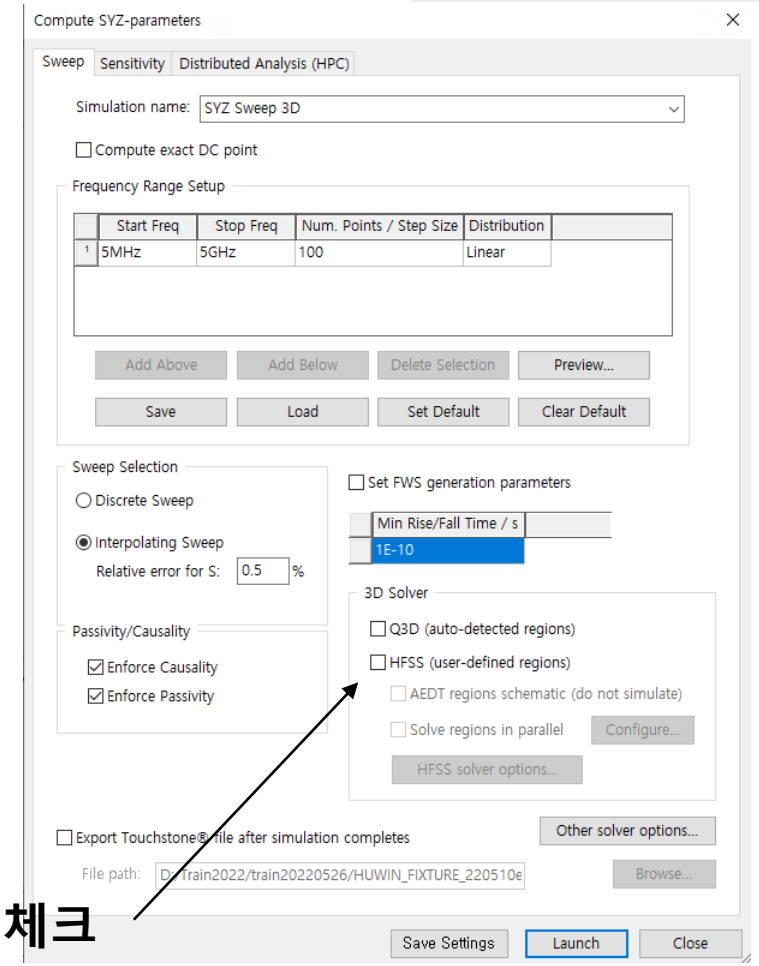



## HFSS를 이용한 PCB 해석 방법 : HFSS region 해석




- PCB만 해석하는 경우 3D 해석이 필요한 부분만 HFSS로 해석하는 방법
  - Port 설정 필요
  - HFSS로 해석할 region 지정 필요

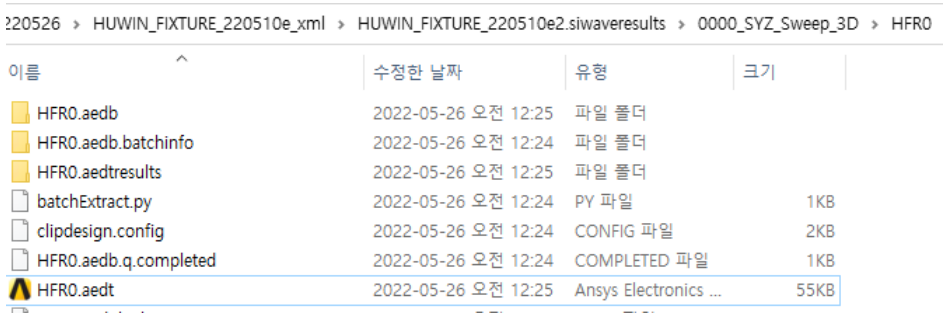


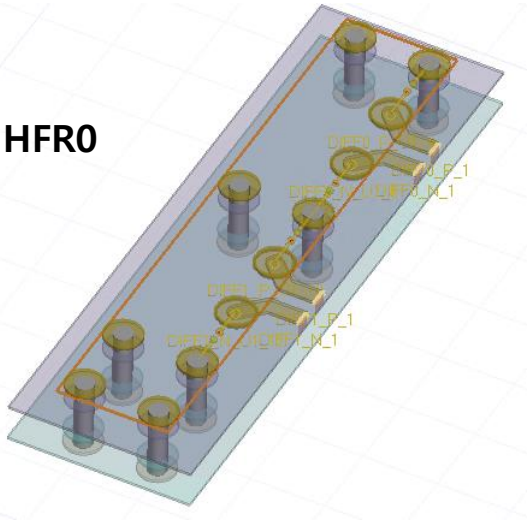



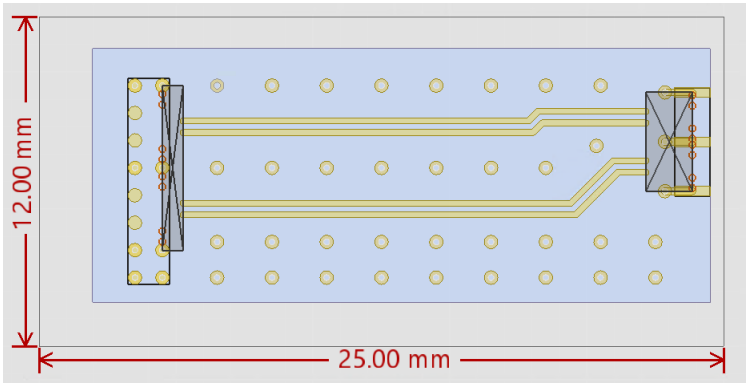

**HFSS 해석 시 체크**

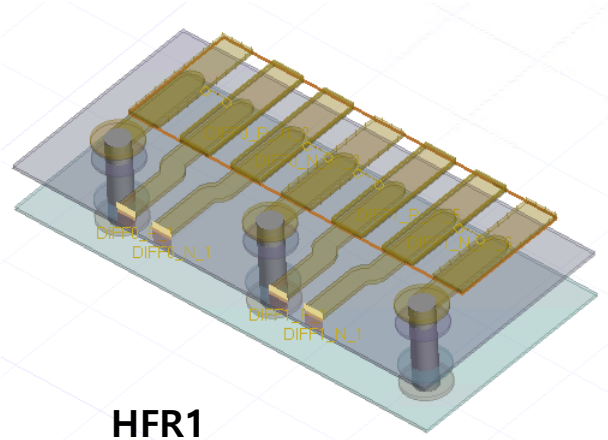
## HFSS를 이용한 PCB 해석 방법 : HFSS region 해석

- SIwave 해석의 solution name과 동일한 이름의 폴더에 저장됨
- 각 region이 따로 저장되고 region(숫자)는 HFR(숫자) 폴더에 저장됨
- SIwave 파일명 + "_wo_regions" 의 이름으로 나머지 부분이 저장됨



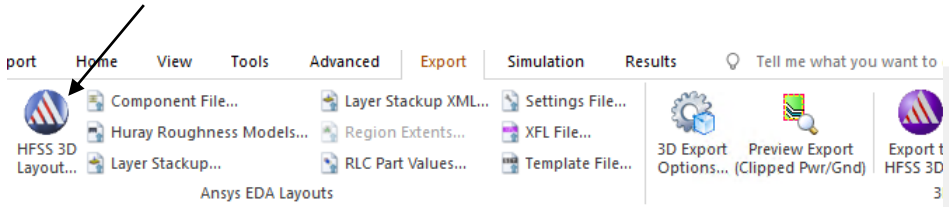



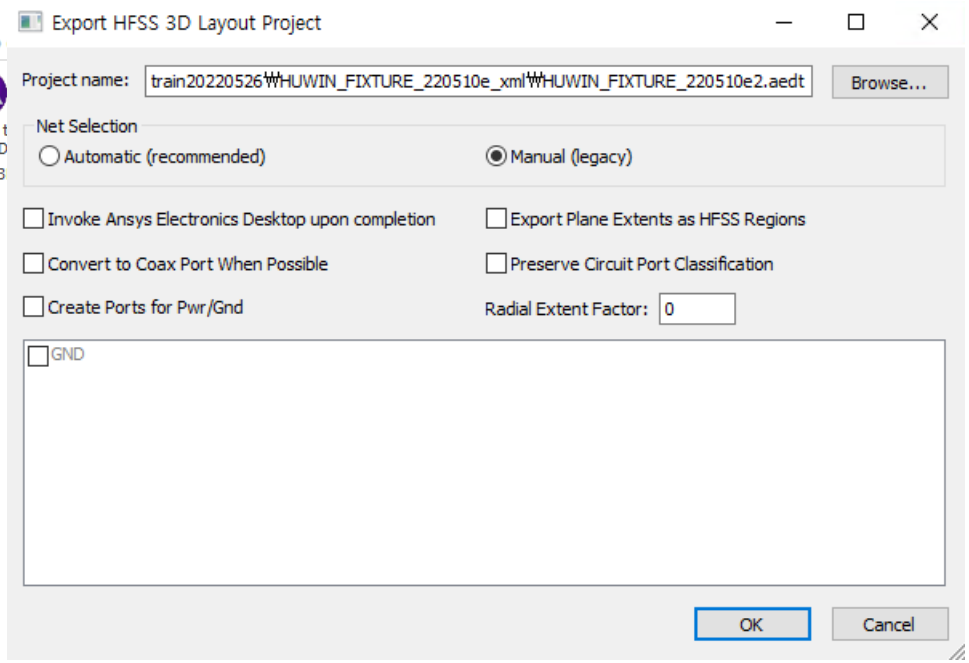



## HFSS를 이용한 PCB 해석 방법 : HFSS 3D layout

❖ 커넥터 또는 IC 모델이 없이 PCB만 해석하는 경우 HFSS 3D layout 활용 방안

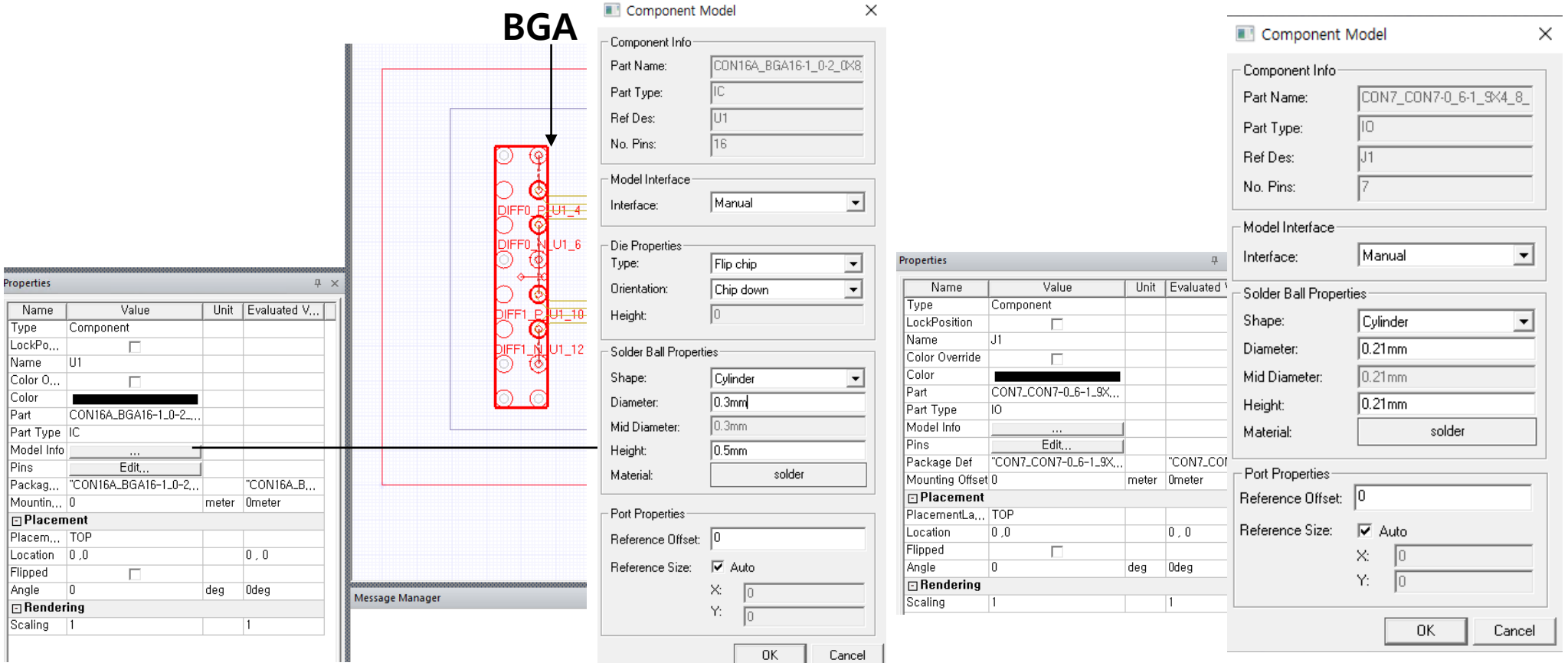
- Export > HFSS 3D Layout 클릭
- PCB 전체 선택 후 아래 그림과 같이 옵션 및 파일 위치 지정 후 OK 클릭
- 기본 Project name이 HFSS로 export와 동일하게 지정되므로 파일명 변경 필요
- 설정된 Region이 없는 경우에 export 가능



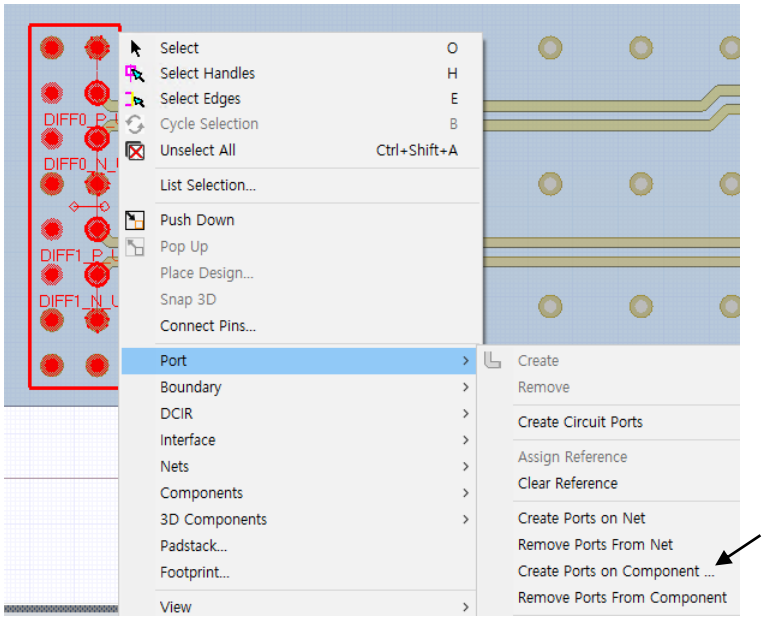
## HFSS를 이용한 PCB 해석 방법 : HFSS 3D layout

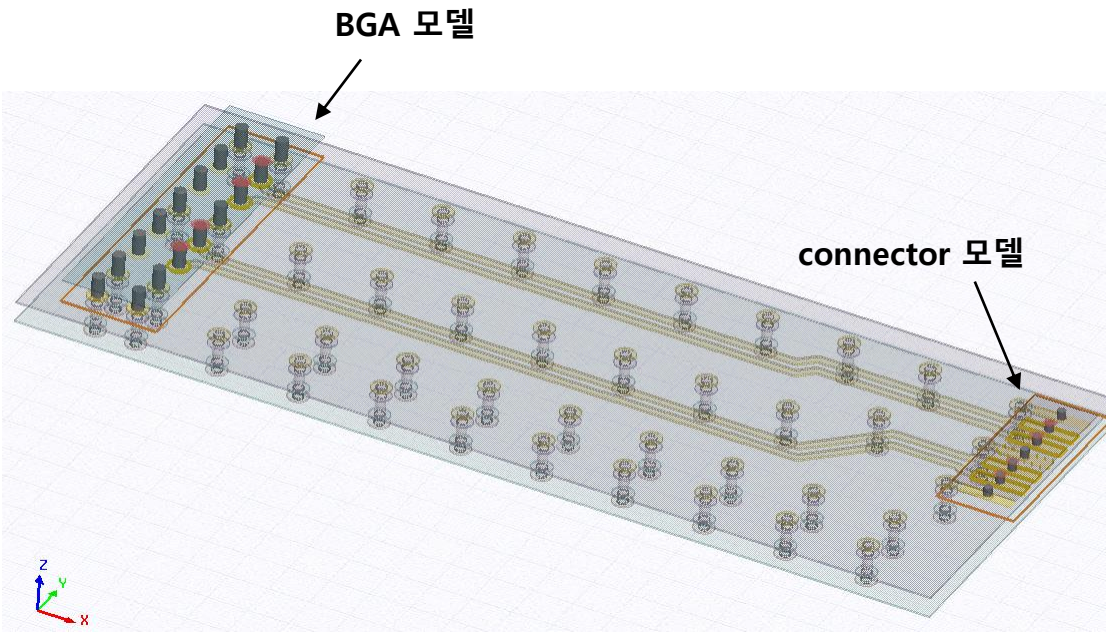
- ❖ BGA 선택 후 속성창의 Model info 클릭
- ❖ Component Model 창에서 BGA 모델 설정 후 OK 클릭
- ❖ 같은 방법으로 connector 모델도 동일하게 설정



## HFSS를 이용한 PCB 해석 방법 : HFSS 3D layout

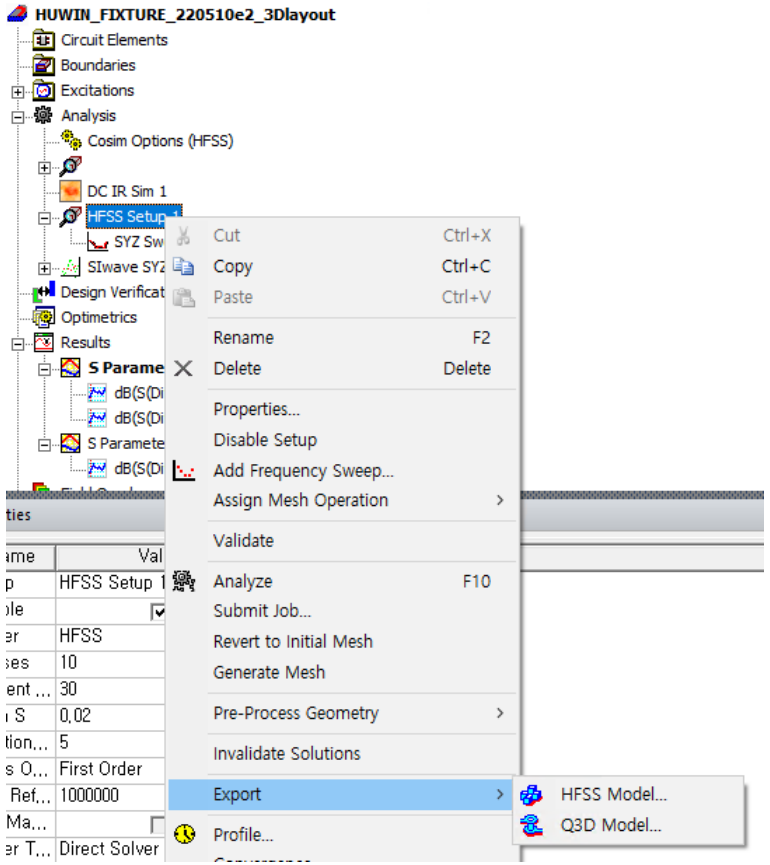
- ❖ BGA 모델 선택 후 우클릭 > Port > Create Ports on Component 클릭하여 port 생성
- ❖ 커넥터도 같은 방법으로 port 생성
- ❖ HFSS setup 선택 후 해석 진행

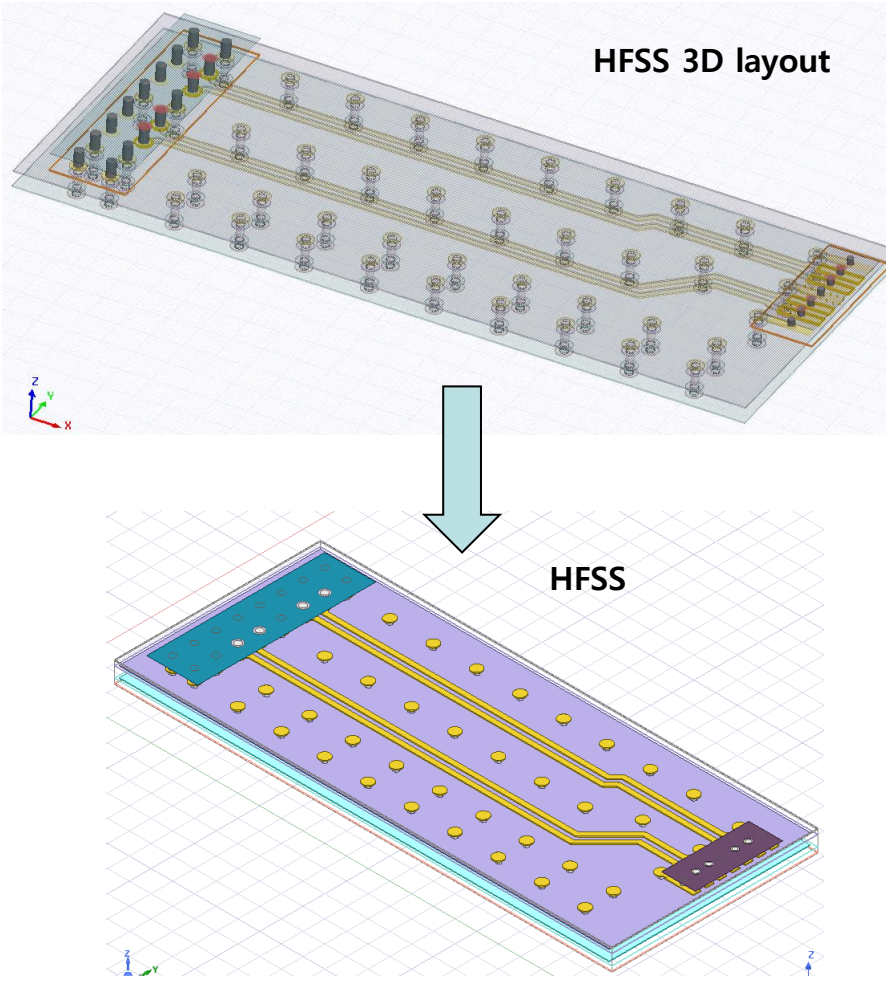


## HFSS를 이용한 커넥터를 포함한 PCB 해석 방법 : HFSS 3D layout에서 PCB export

❖ HFSS 3D layout의 solution 우클릭 > Export > HFSS Model 클릭하여 export



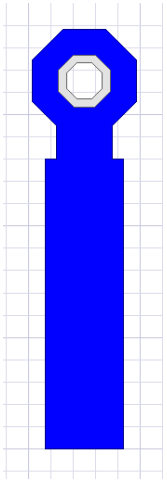



## SIwave to HFSS : HFSS를 이용한 PCB 해석

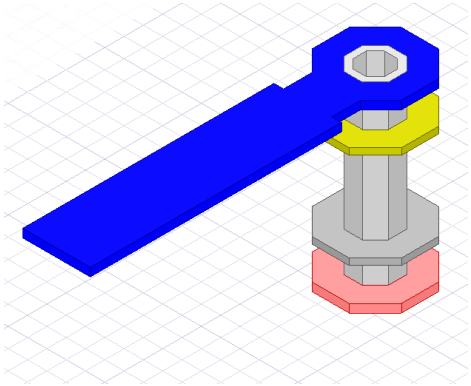
❖ SIwave는 PCB 데이터를 import하여 직접 해석하거나 주요 인자를 편집하여 HFSS로 export 가능함

❖ stack-up 편집
- ➢ PCB 데이터의 stack-up 수정이 가능하며, 모델링 작업 전 확인

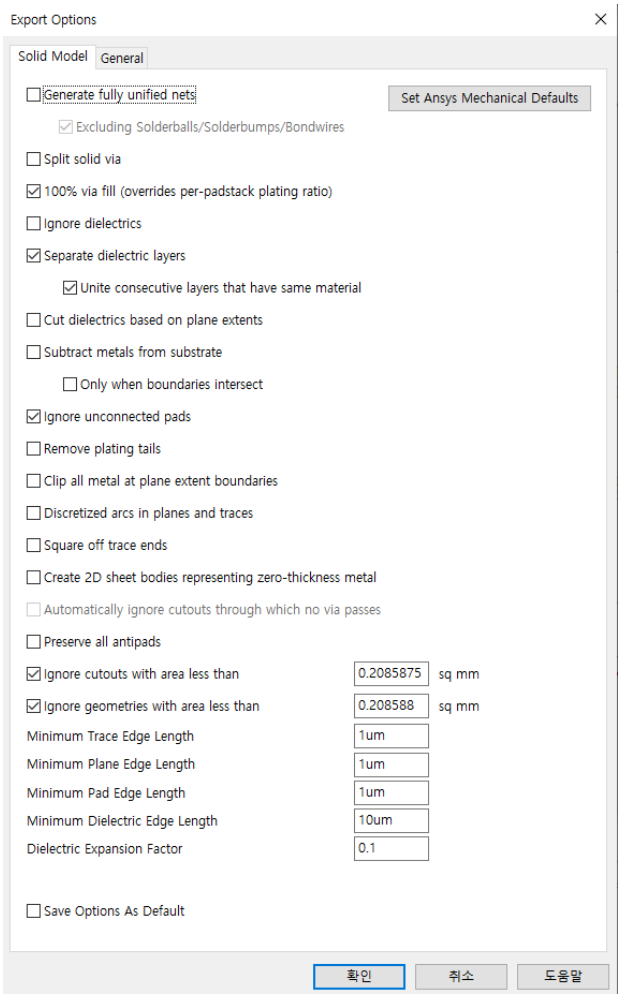
❖ SIwave export 옵션 설정
- ➢ 100% via fill: Pad stack editor의 Via Plating 무시
- ➢ Separate dielectric layers: 유전체 종류별로 분리
- ➢ Ignore unconnected pads: trace가 연결되지 않은 pad 무시



**100% via fill 체크 해제 형상**

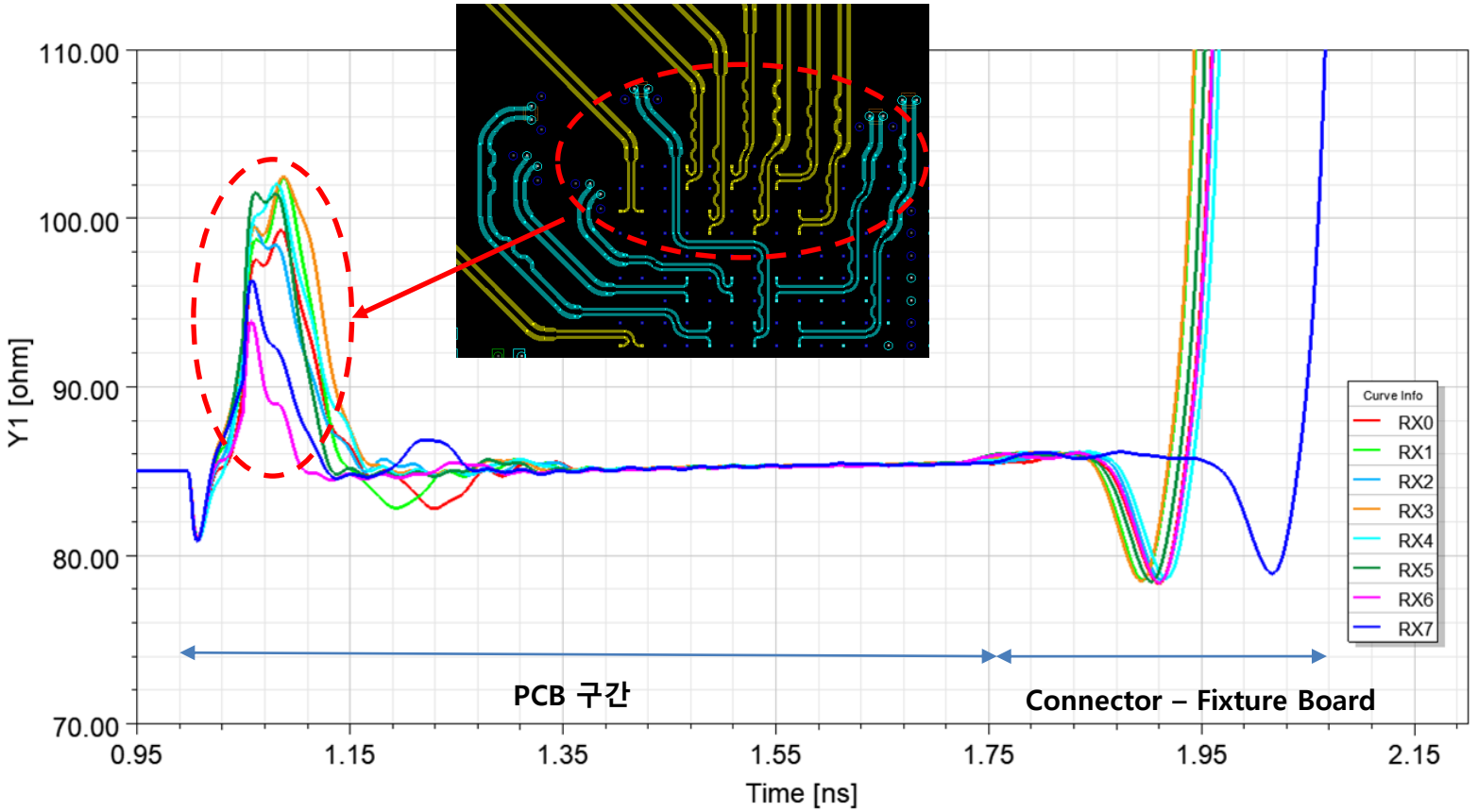


**Ignore unconnected pads 체크 해제 형상**



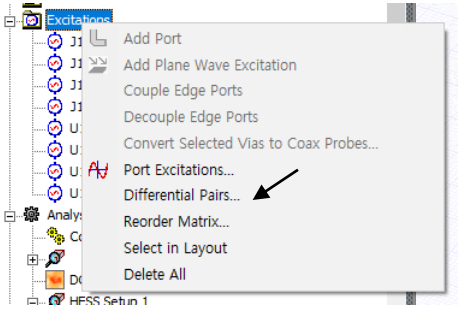
## HFSS 해석 사례 : 공간 부족으로 인한 임피던스 불연속

- BGA 또는 socket과 같이 trace 폭의 확보가 불가능한 경우 임피던스 불연속이 발생함
- 채널특성에 대한 영향 분석이 필요하고 개선을 위해서는 stack-up 변경 등이 필요함
- 정확한 분석을 위해 꼭 3D 해석이 필요함

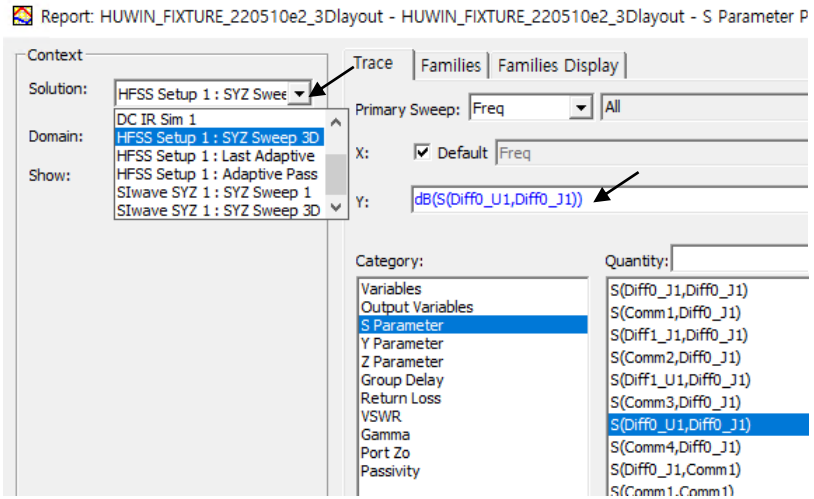


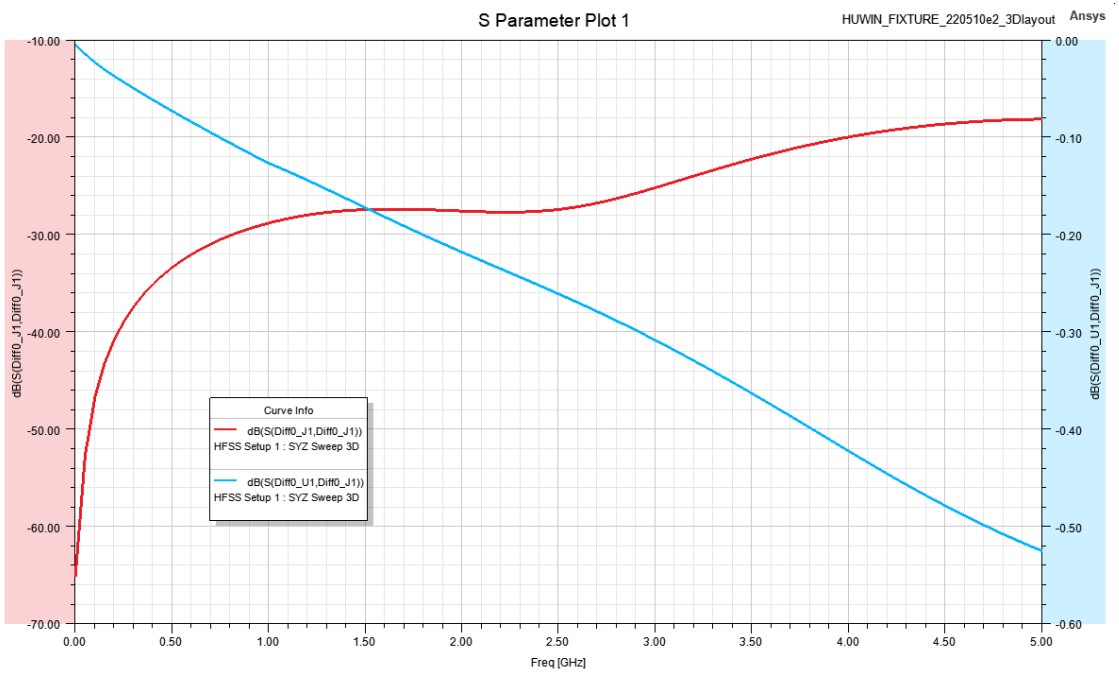
## HFSS를 이용한 PCB 해석 방법 : HFSS 3D layout

- ❖ 해석 완료 후 Excitations 우클릭하여 Differential Pairs 클릭하여 설정
- ❖ Report 창에서 해석한 Solution 선택 후 해석 결과 확인




| Terminals: | | Pairs: | | Differential Mode: | | Com |
|---|---|---|---|---|---|---|
| Positive | Negative | Enabled | Matched | Diff, Na... | Ref, Z (oh,... | Comr |
| J1,2,DIFF0_P | J1,3,DIFF0_N | ☑ | ☐ | Diff0_J1 | 85,00 | Comr |
| J1,5,DIFF1_P | J1,6,DIFF1_N | ☑ | ☐ | Diff1_J1 | 85,00 | Comr |
| U1,10,DIFF1_P | U1,12,DIFF1_N | ☑ | ☐ | Diff1_U1 | 85,00 | Comr |
| U1,4,DIFF0_P | U1,6,DIFF0_N | ☑ | ☐ | Diff0_U1 | 85,00 | Comr |

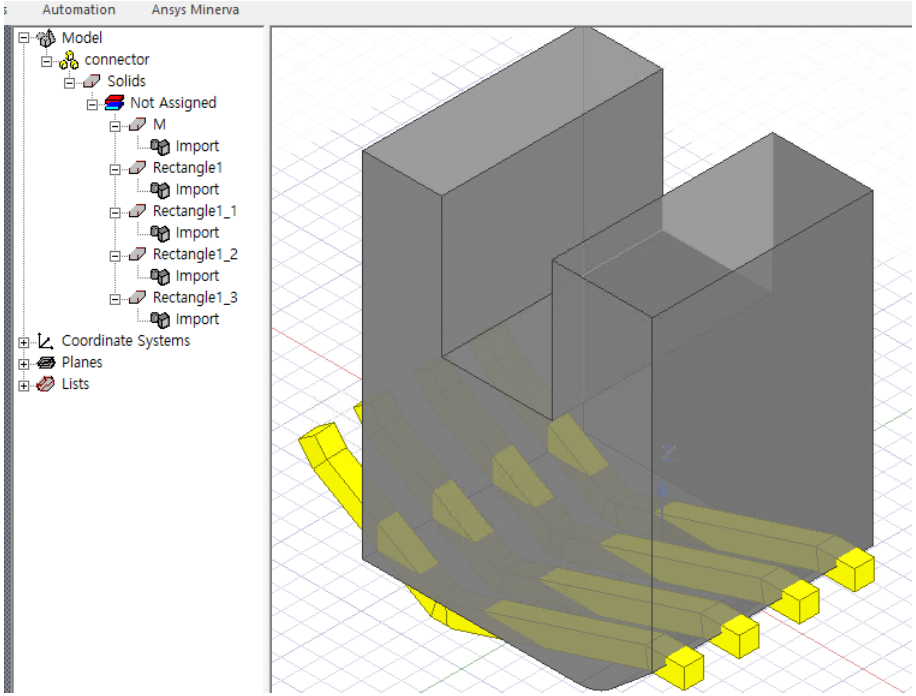


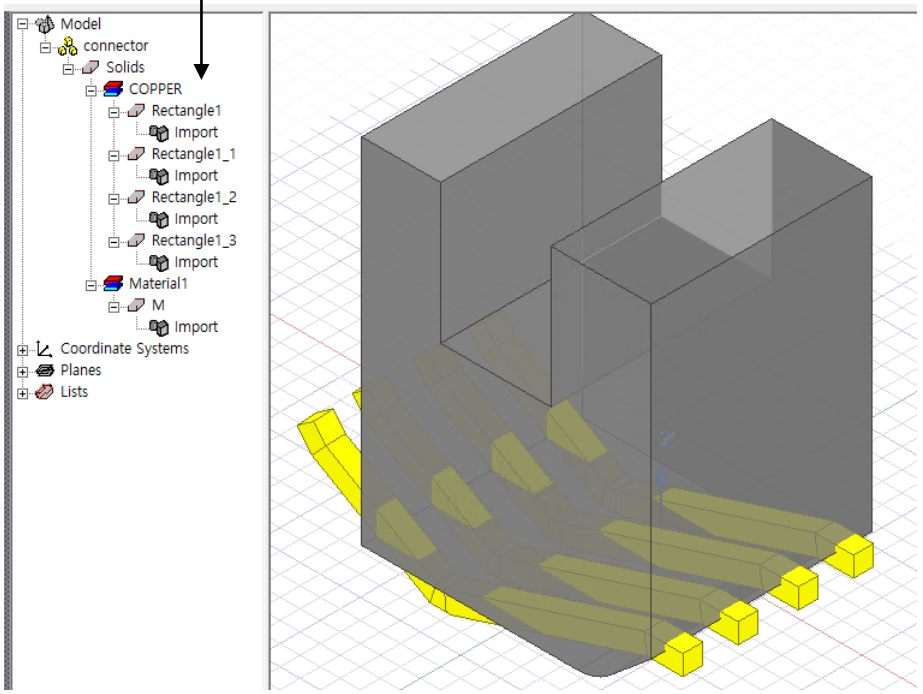
## HFSS를 이용한 커넥터를 포함한 PCB 해석 방법 : Connector import & 물성 입력

- ❖ 커넥터 부분 포트 및 PEC ground 삭제
- ❖ Menu bar의 Modeler > import 클릭 후 커넥터 모델 선택하여 열기
- ❖ 일반적인 커넥터 기구 파일은 import 후 전기적 특성 설정 필요

**Import 형상**

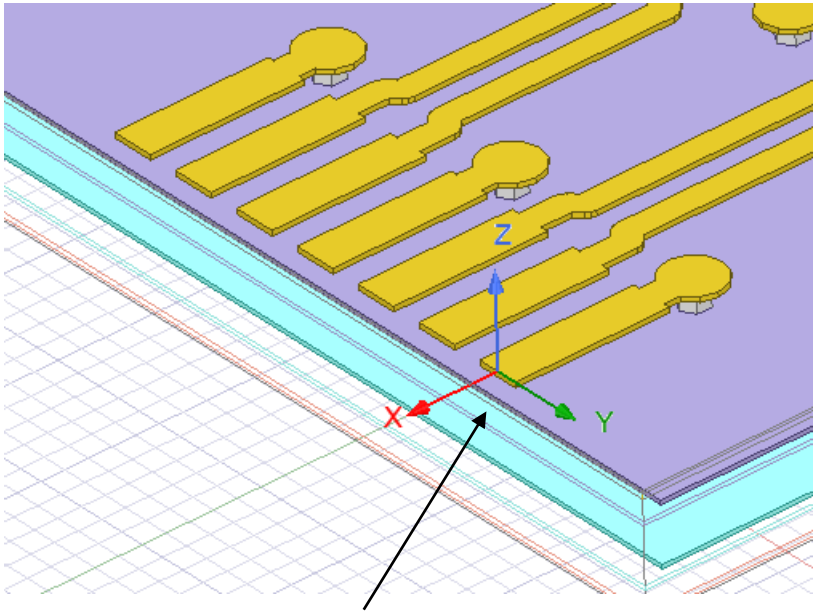



**물성 설정**

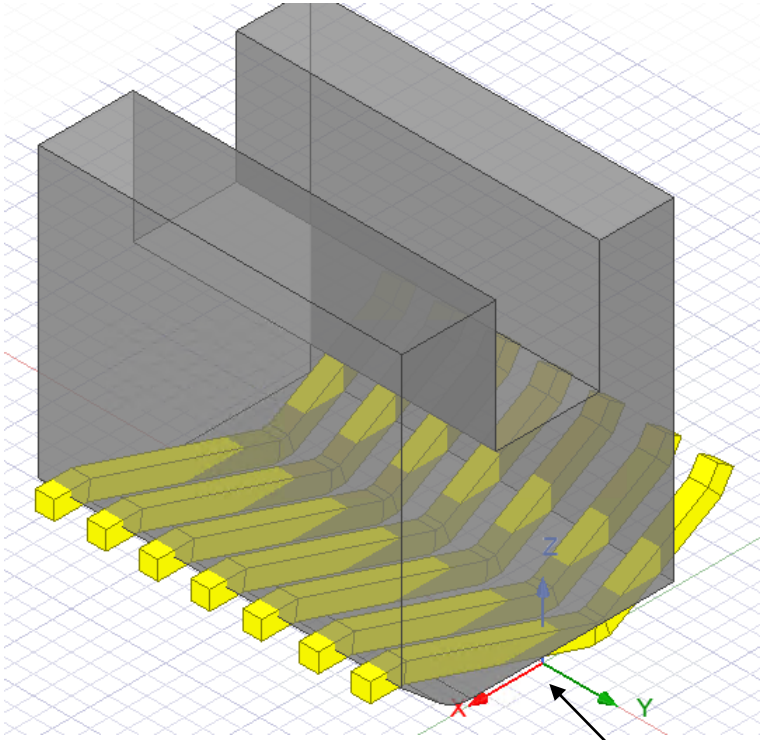


## HFSS를 이용한 커넥터를 포함한 PCB 해석 방법 : PCB에 커넥터 실장

- PCB 상의 커넥터 실장 지점에 상대 좌표 추가
- 커넥터를 복사하여 PCB 파일에 붙여넣기 할때 커넥터 파일의 global 좌표는 PCB 파일의 상대 좌표로 붙여넣기 됨



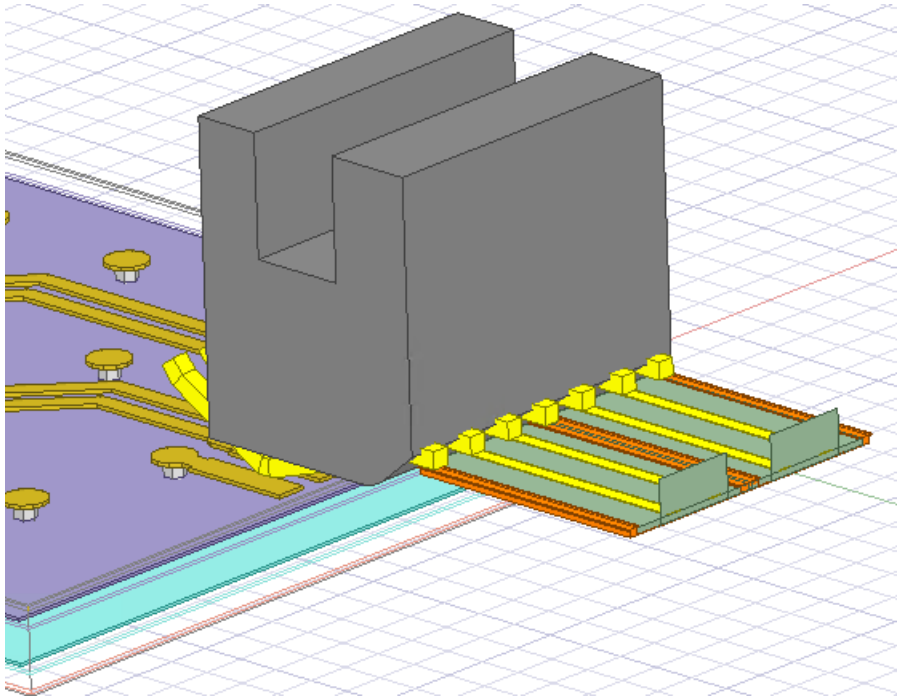

PCB 파일의 global 좌표

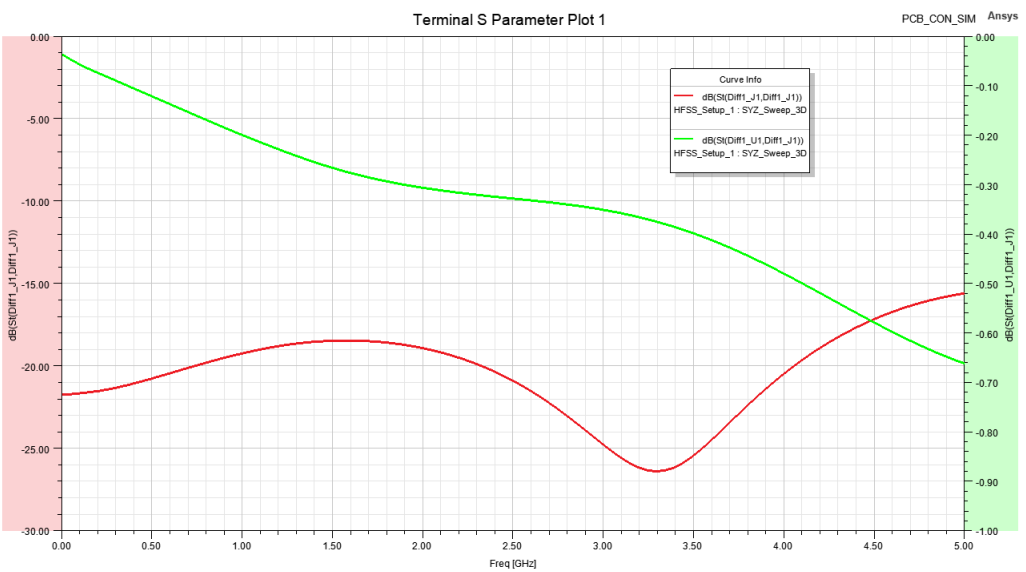



커넥터 파일의 global 좌표

## HFSS를 이용한 커넥터를 포함한 PCB 해석 방법 : 커넥터 port 설정

- ❖ 커넥터 해석 시 mate 상태로 해석해야 정확한 결과를 얻을 수 있음
- ❖ B2B 커넥터의 경우 상대 PCB 추가 필요

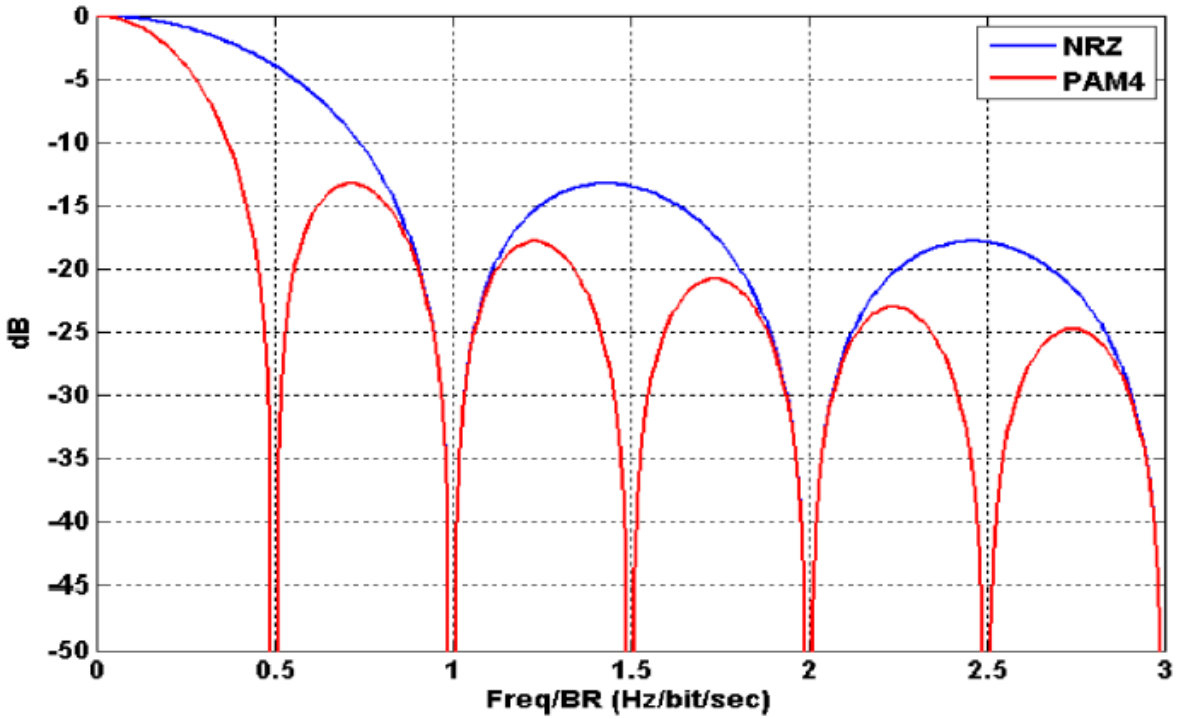




## MLCC PAM4 application design guide : PAM-4 Signaling

**Figure 2. Power Spectrum Density of NRZ and PAM4**

At 56 Gbps, PAM4 requires half of the Nyquist frequency as that of NRZ.




PAM4 $f_{Nyquist}$ = 56/4 = 14 GHz (Figure 1 on page 5)

NRZ $f_{Nyquist}$ = 56/2 = 28 GHz (Figure 2 on page 5)

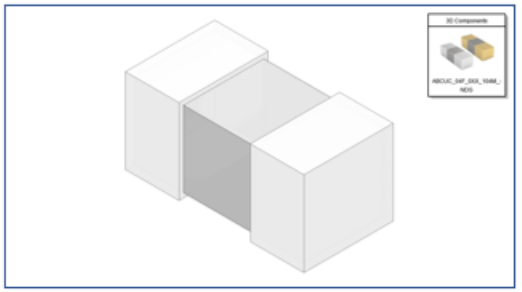
CEI-56G : 56Gbps PAM4 -> $f_{Nyquist}$ = 14GHz => BW : 5*14GHz=70GHz

## MLCC PAM4 application design guide : 70GHz AC coupling

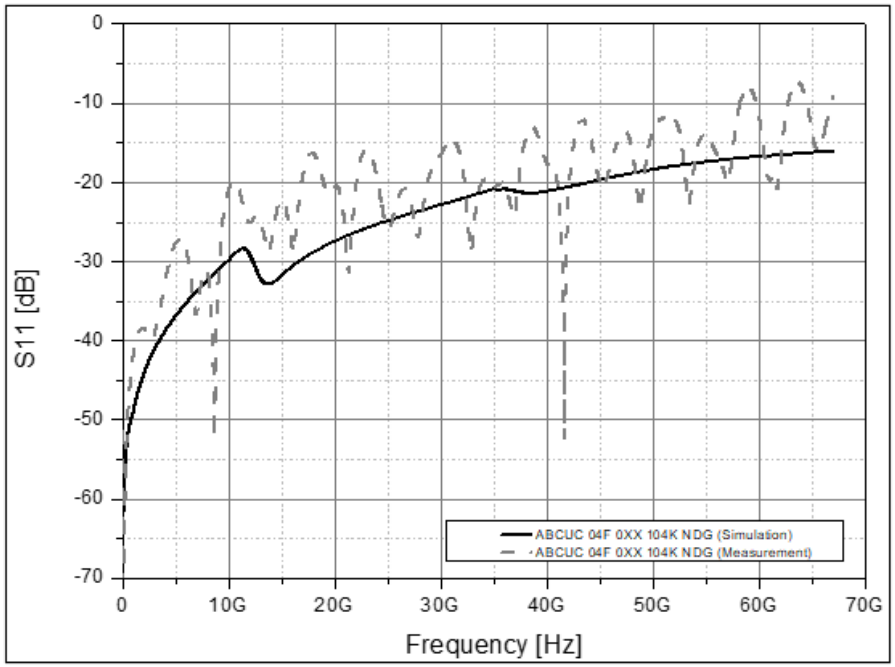
AMOTECH Broadband Capacitor

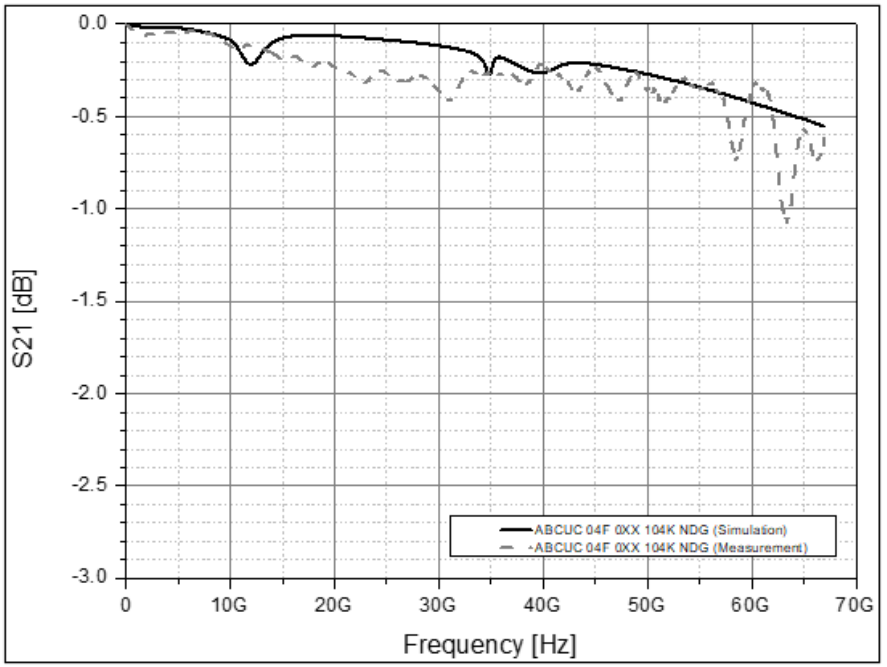
### HFSS 3D Components

ABCUC 04F 0XX 104K NDG

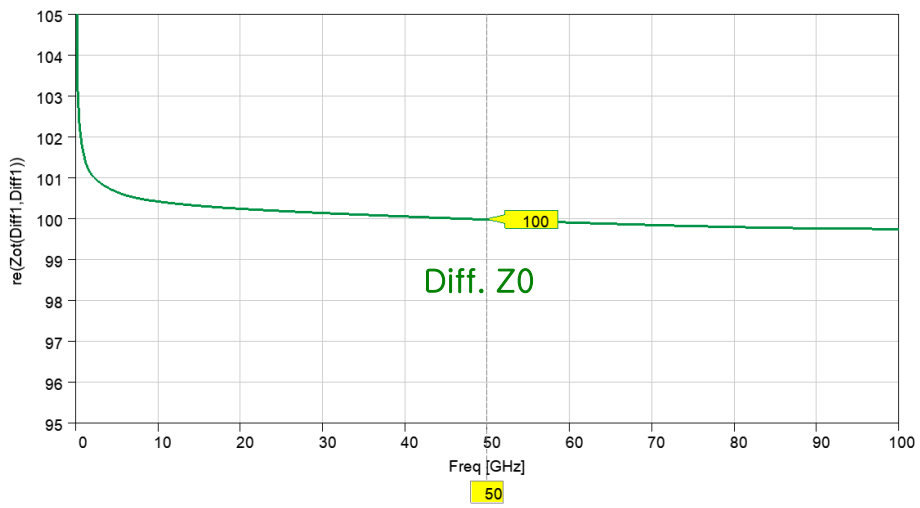


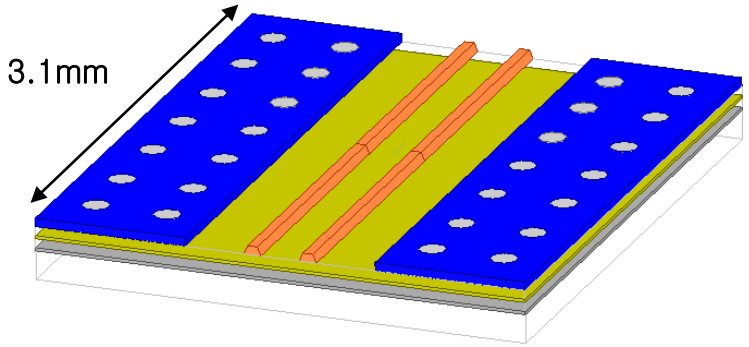
Simulation Result & Measurement [10MHz-67GHz (10MHz step)]

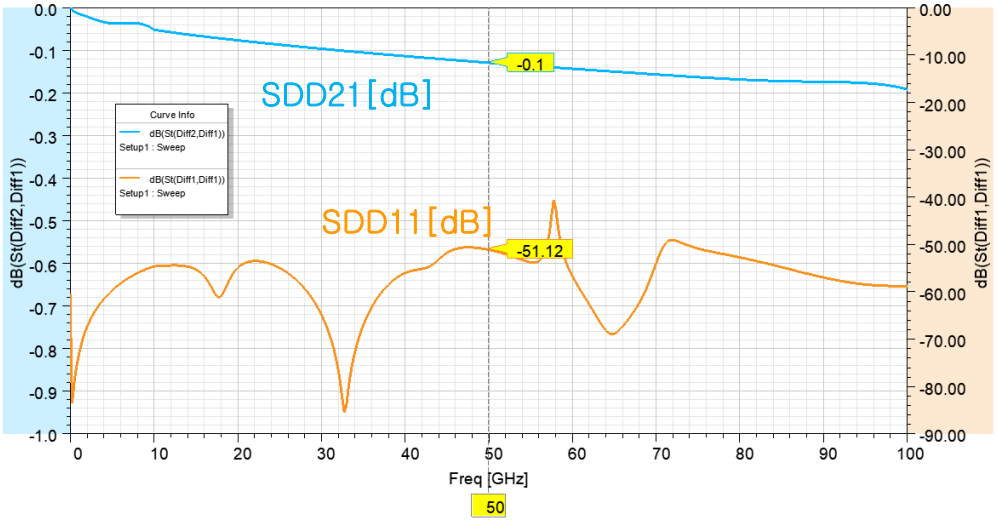


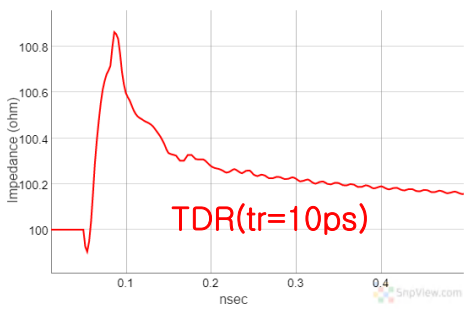



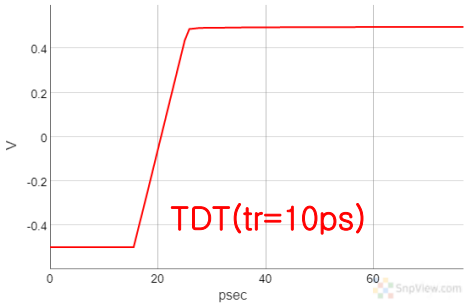
## Transmission Line only results

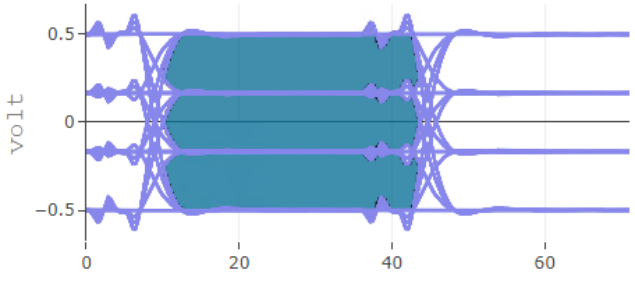


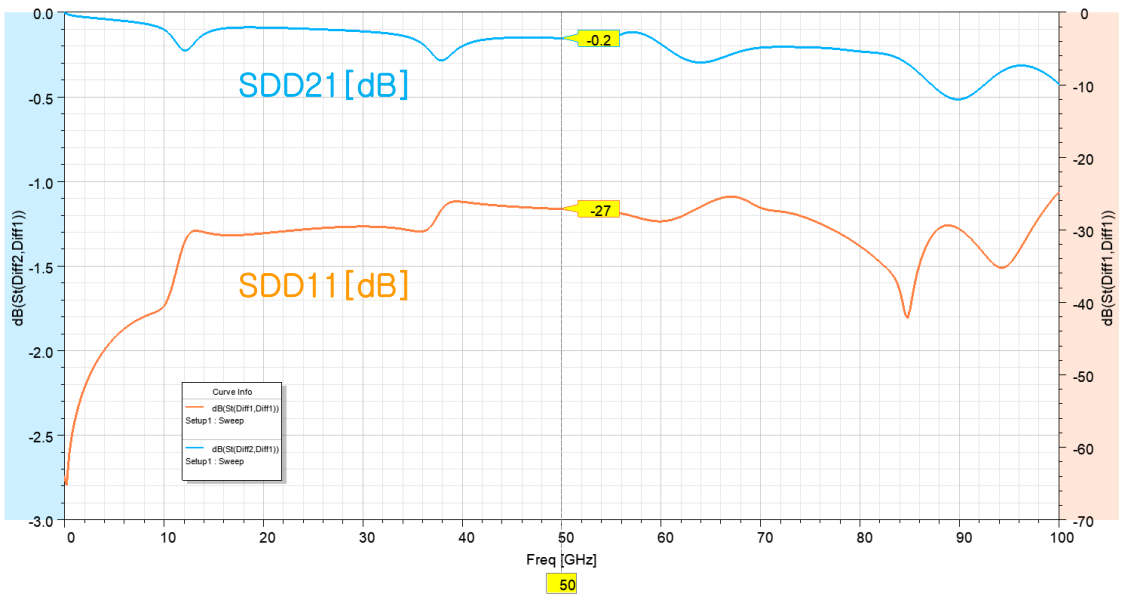



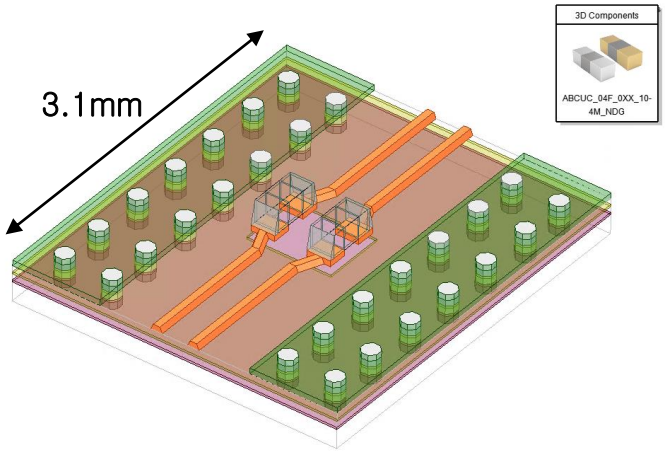



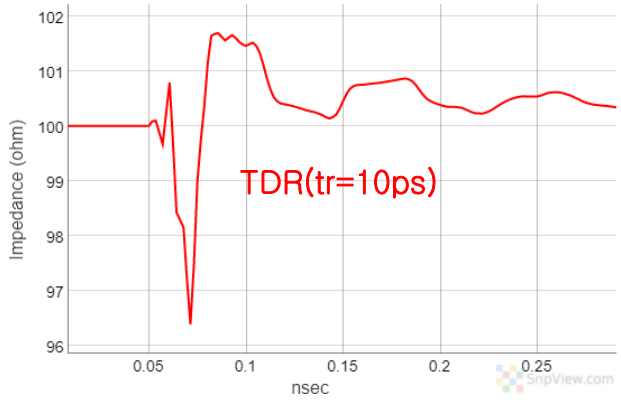



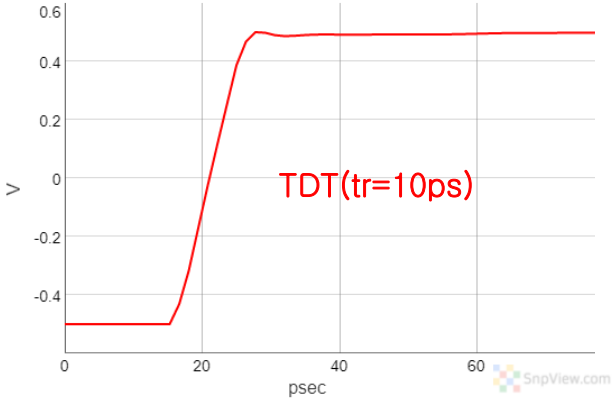

Eye Diagram

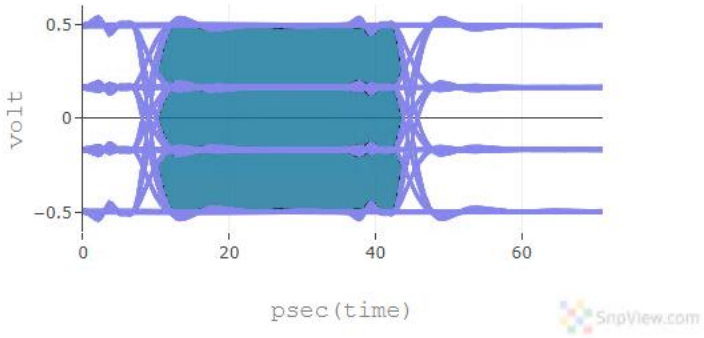
## Transmission Line + MLCC results



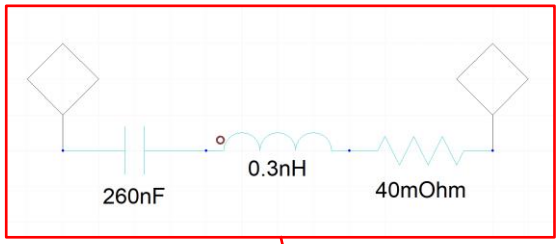



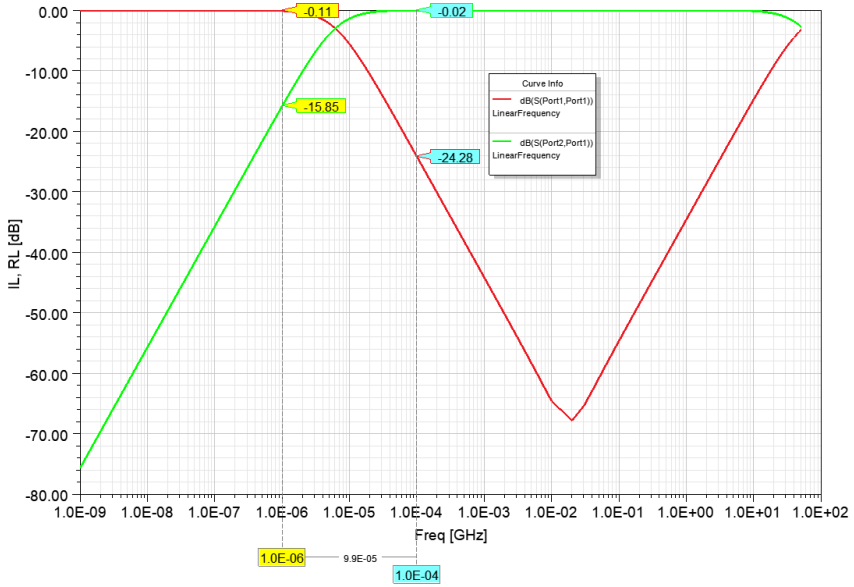

Eye Diagram

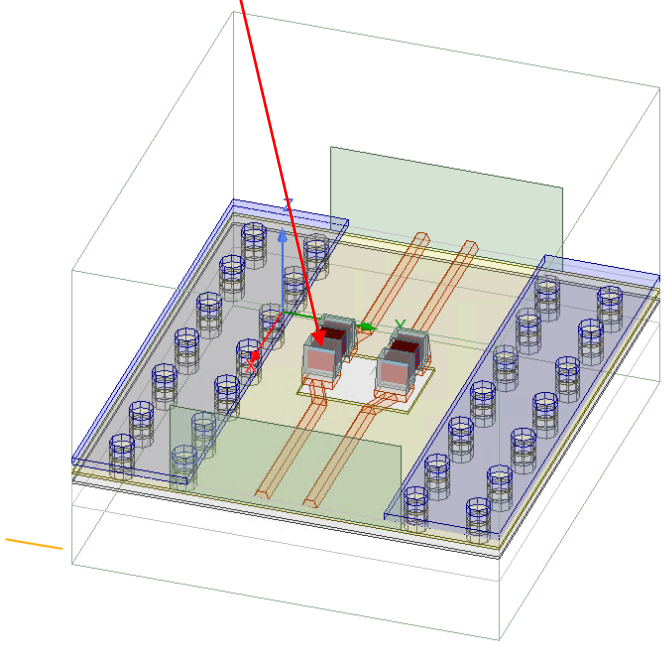
## Series Capacitor TDR 분석 개요

0402M MLCC (260nF , ESR: 40mΩ, ESL:0.3nH) 에 대한 TDR Test :




등가회로



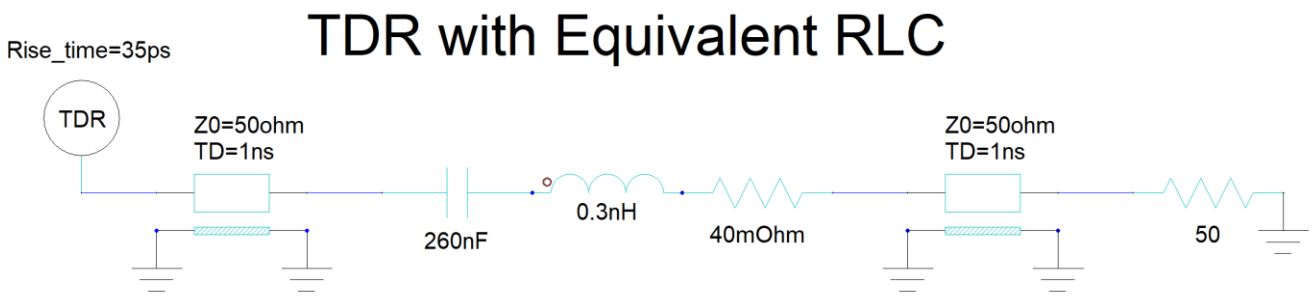
MLCC 3D EM model 이용한 분석

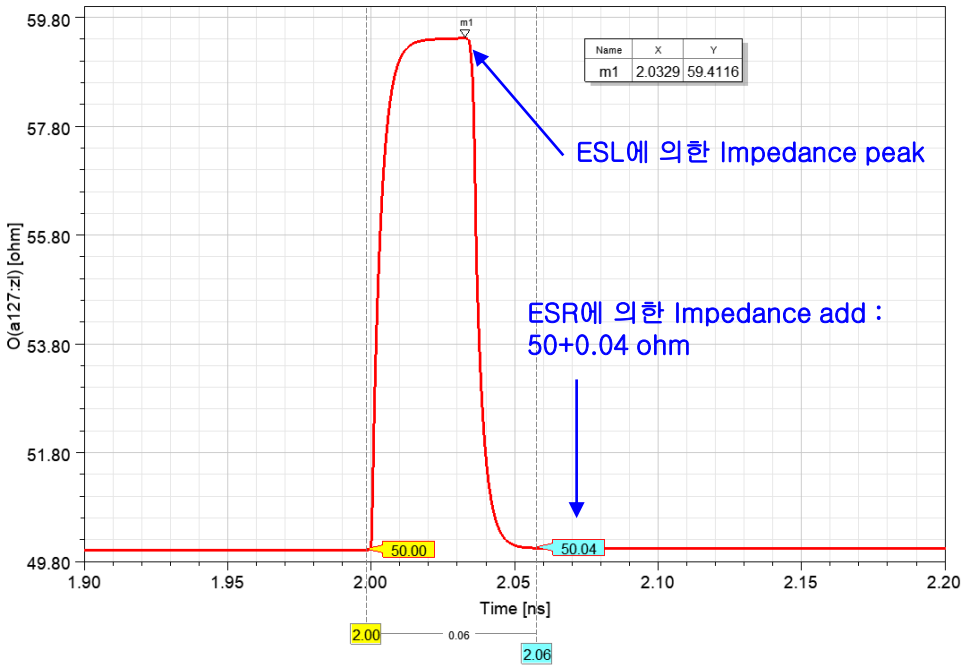
260nF Series Cap. 의 경우 1kHz ~100kHz 사이 S-parameter curve 의 변곡점 있으므로 정확한 Time 파형 분석을 위해 이 대역의 값이 필요함.

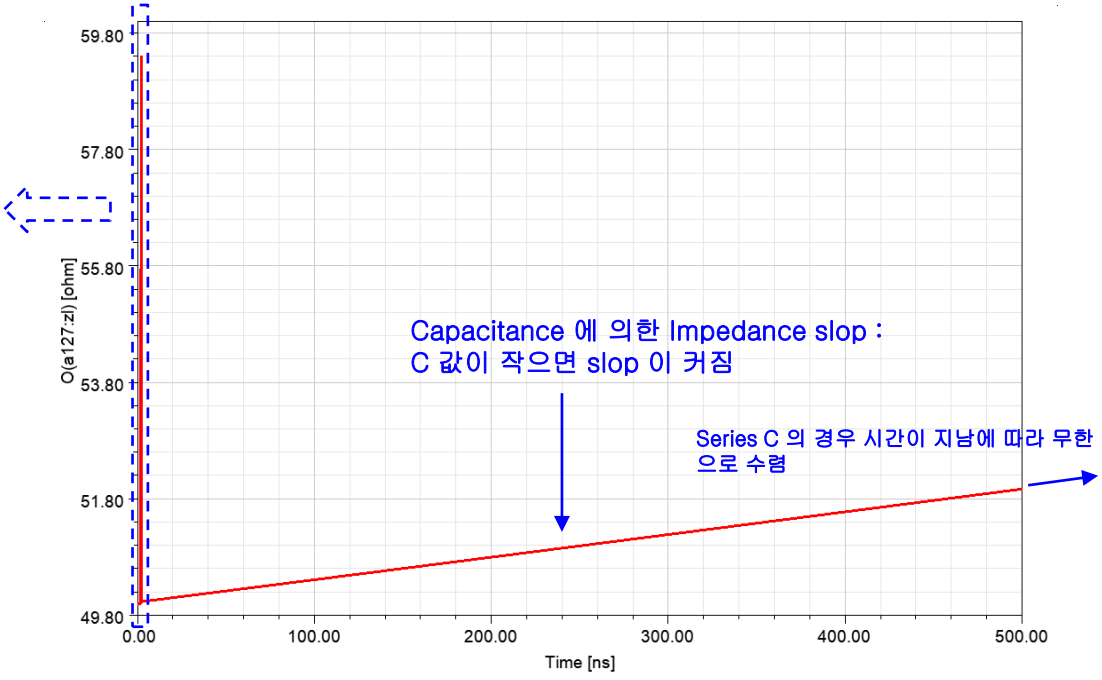
=> 측정이나 시뮬레이션 시 1kHz 이하 부터 Sweep 이 필요함.

## Series Capacitor 등가 회로의 TDR curve 특성

등가 회로에 대한 TDR Test :

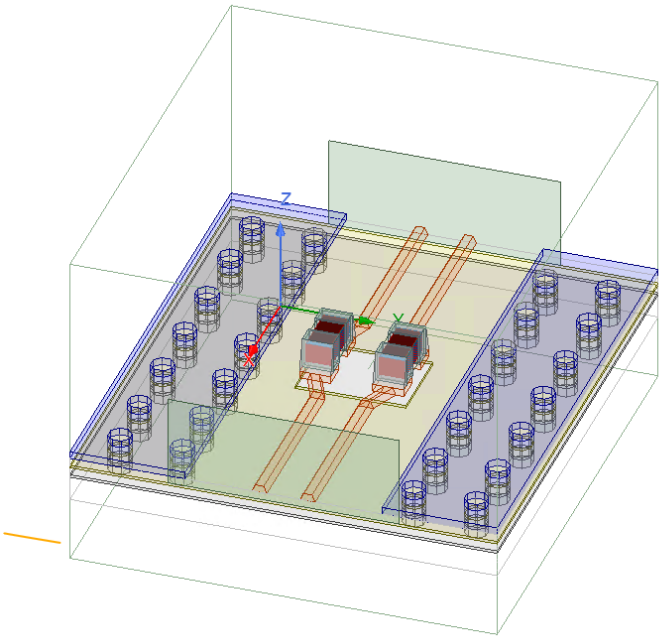


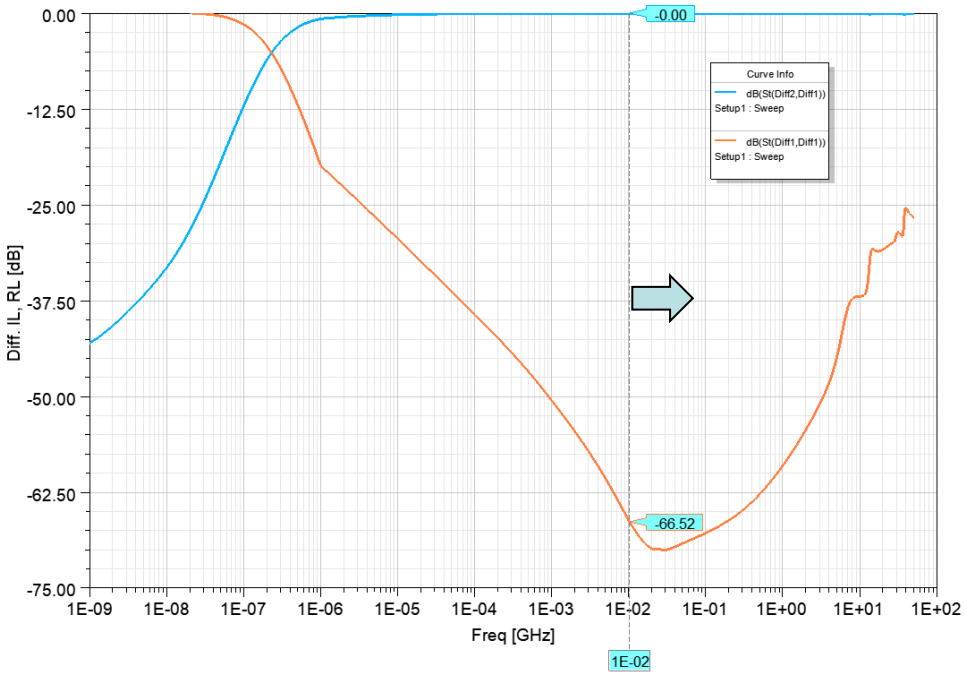



## MLCC 3D EM model 이용한 분석

IL, RL of Differential line with MLCC 3D EM model :



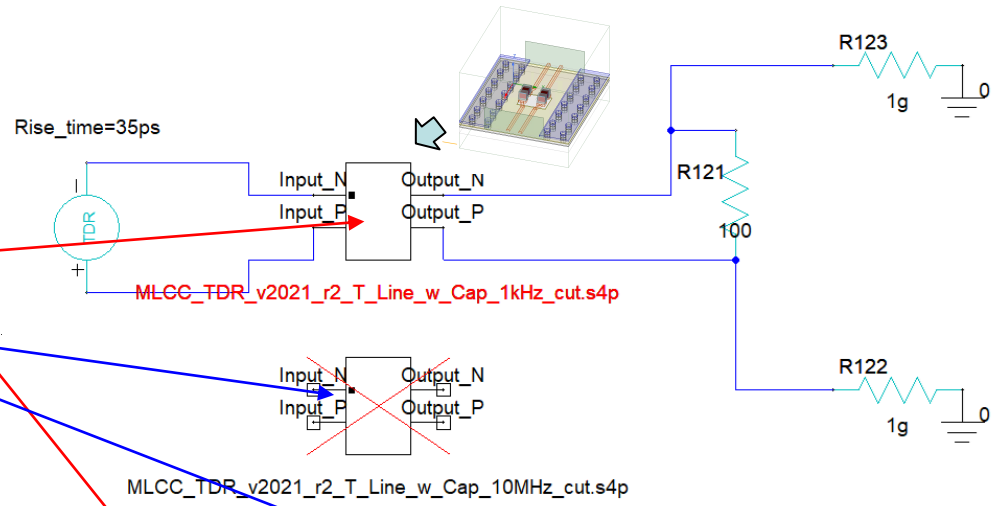

10MHz 이상 주파수부터 측정 또는 시뮬레이션 하는 경우 낮은 주파수에서의 결과가 정확하게 extrapolation 되지 않을 수 있음.

=> Capacitor 용량이 200nF 이상으로 큰 경우 1kHz 이하부터 측정 또는 시뮬레이션 권장.

## Series Capacitor 3D EM 모델의 TDR curve 특성

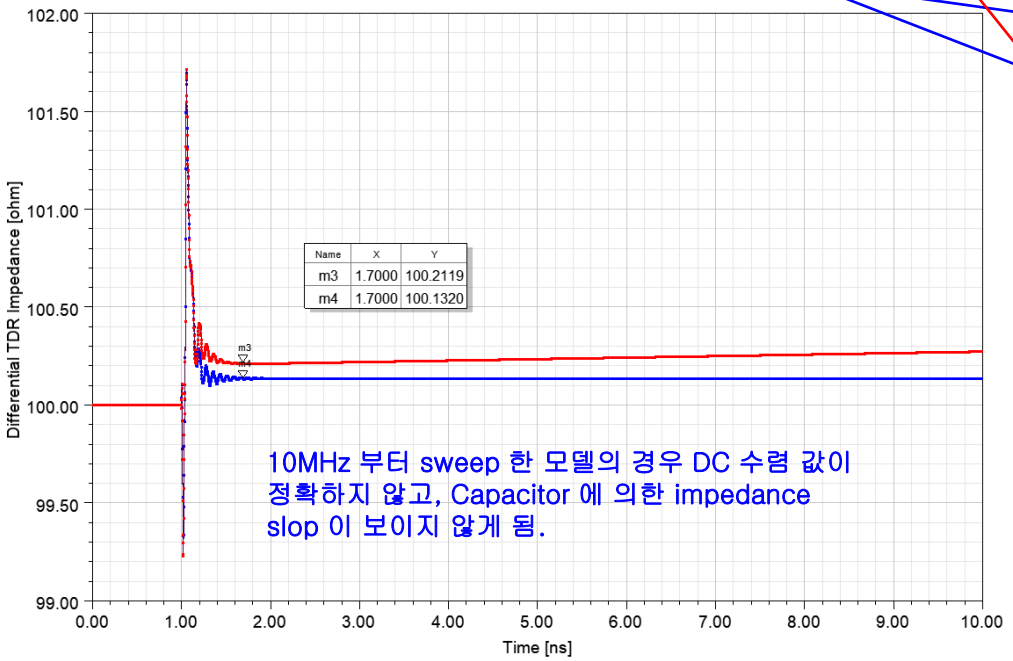
TDR of Differential line with MLCC 3D EM model :

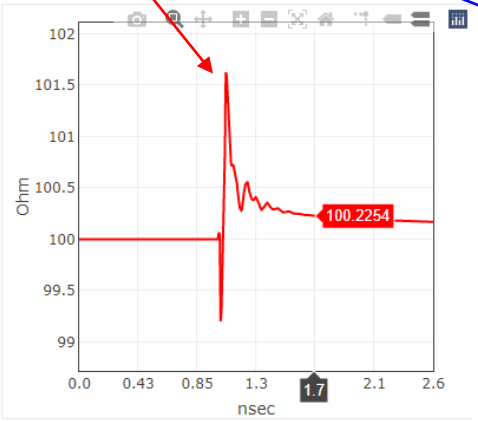
Differential Time Domain Reflectometer

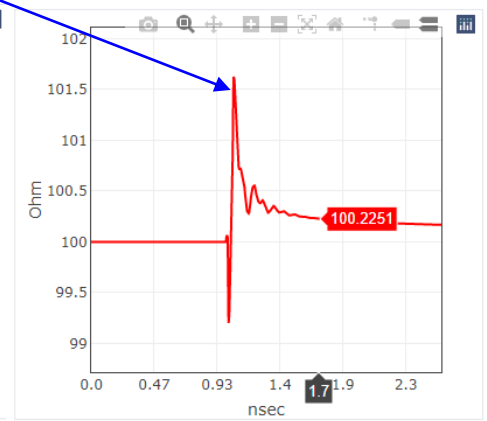



1kHz 이하부터 sweep 한 S-parameter 모델 (권장)

10MHz 부터 sweep 한 S-parameter 모델



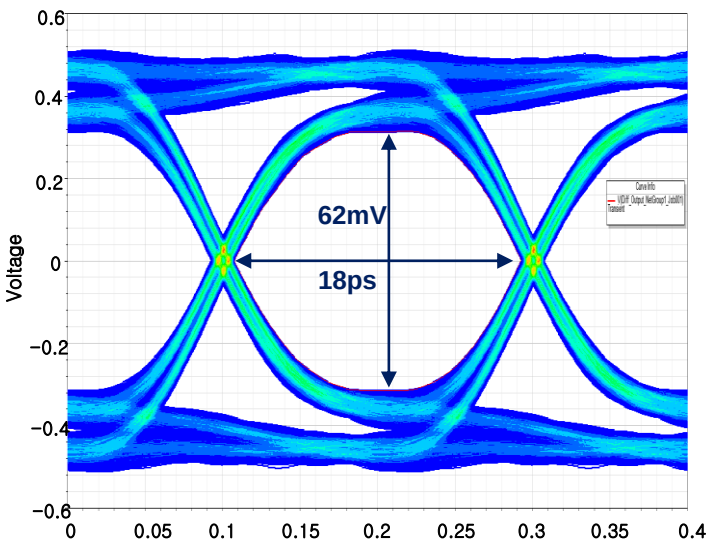



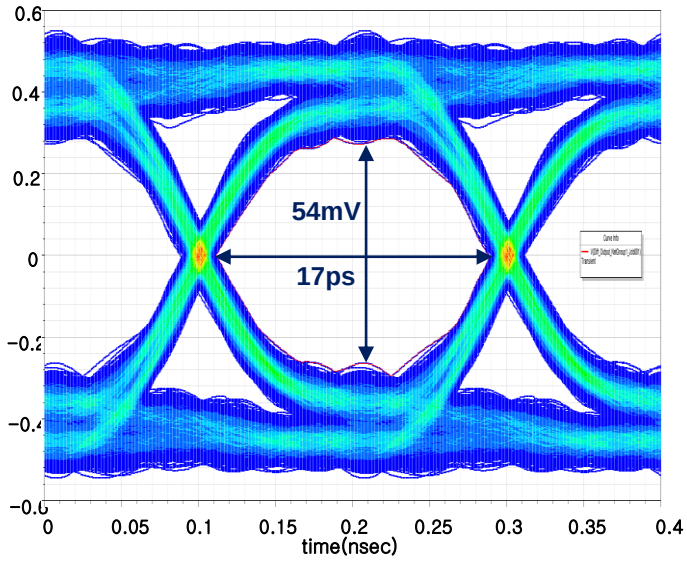




* Ref. TDR 결과 : www.snpview.com

## Transient Simulation : 분석 시 체크 사항 - 대역 조건

- S-parameter의 다양한 특성이 Eye-diagram 정확도에 영향을 미침
  - ➢ **S-parameter의 대역 조건, Causality, Passivity 특성을 사전에 파악하고 개선 필요**

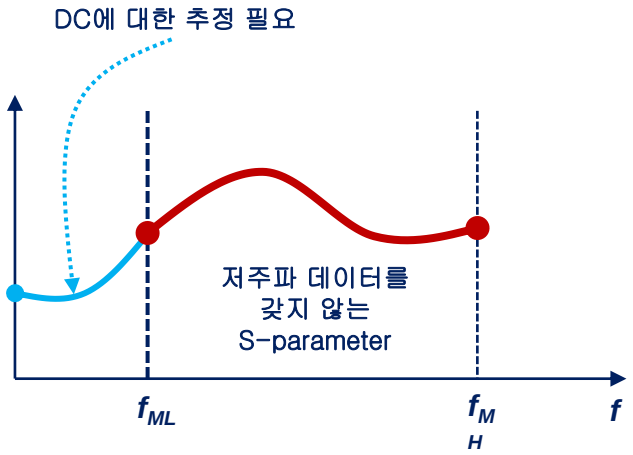



동일 채널의 **S-parameter**의 특성에 따른
**Eye-diagram** 결과 차이

## Transient Simulation : 분석 시 체크 사항 - DC 추정

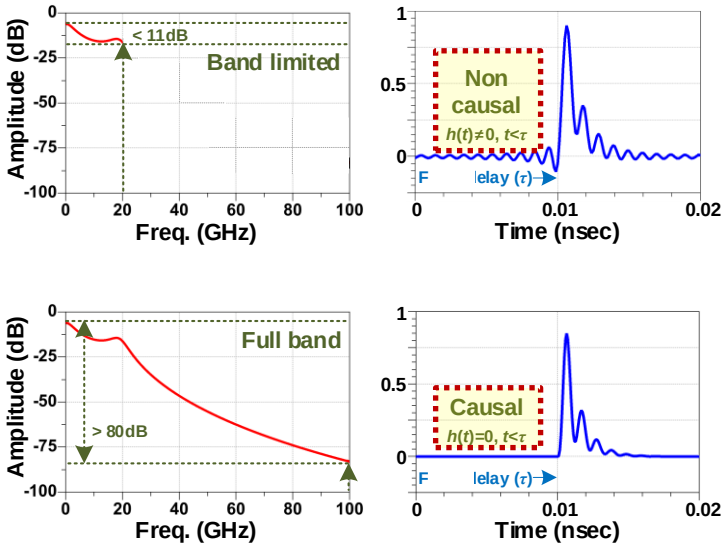
- 저주파 데이터를 갖지 않는 S-parameter에 대한 DC 추정
  - **S-parameter가 저주파 대역을 갖지 않는 경우 Transient 결과의 Steady state 정확도 감소**
  - **Designer Nexxim solver의 DC 추정 option 제공**



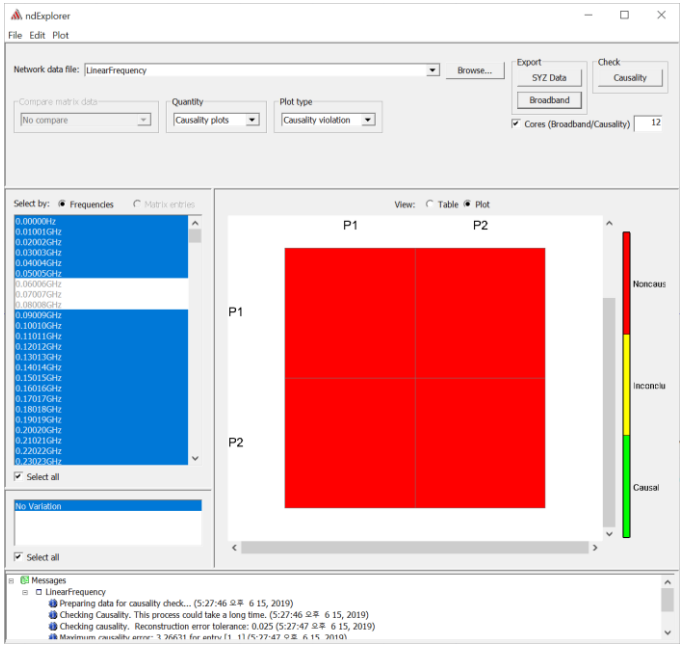

## Transient Simulation : 분석 시 체크 사항 – Causality

- 시간 응답이 delay time 이전에 값을 갖지 않는 특성 ($h(t_d)=0, t_d<0$)

➢ **Vector fitting 기법 적용으로 대역 제한된 S-parameter에 대한 Causality 문제 해결**
➢ **EM solver의 정확도 문제로 인한 S-parameter 자체의 Causality 문제는 Enforcing으로 해결**



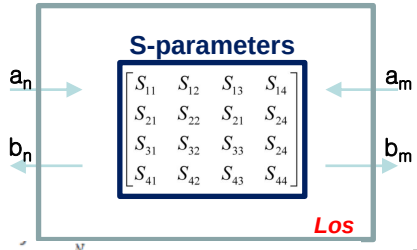

**Band-limited 특성에 의한 Causality 문제는 Vector fitting에 의해 해결**




**S-parameter 자체의 Causality 문제는 Causality check를 통해 확인 가능 (Enforcing option 제공)**

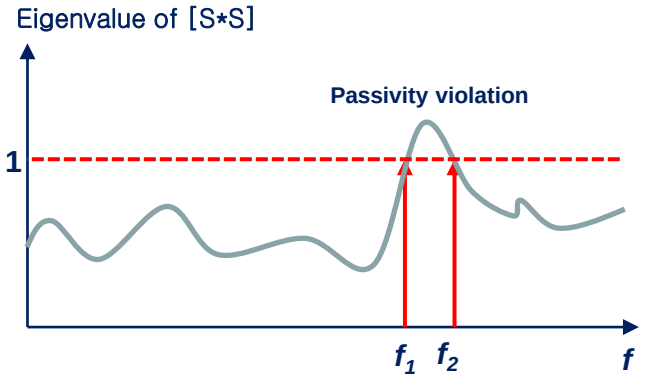
## Transient Simulation : 분석 시 체크 사항 - Passivity

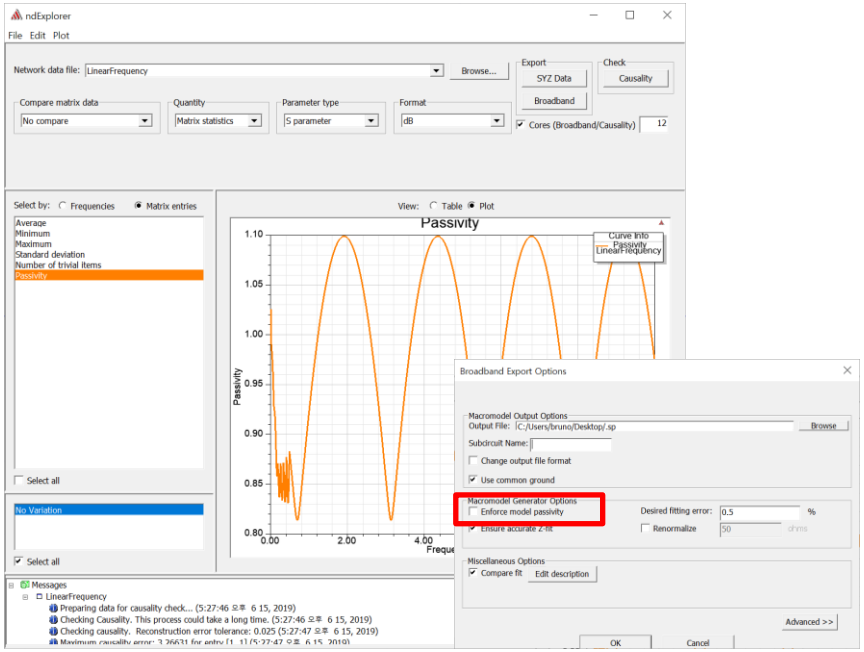
- 수동 소자의 S-parameter는 에너지 이득이 없는 특성
  - ➢ **에너지 보존 법칙 (고립계에서 에너지의 총합은 일정)이 수동 소자의 S-parameter에도 적용됨**
  - ➢ **Passivity 확인 및 Enforcing 기능 제공**




$$P_{in} = \sum_{n=1}^{N} |a_n|^2 - |b_n|^2 = \left[\bar{a}^* \cdot \bar{a} - \bar{b}^* \cdot \bar{b}\right] \geq 0$$

Transmitted power ($P_{in}$)의 총합은 0보다 큼




**S-parameter 의 Passivity 확인 및 Enforcing**

# Huwin ACVS

## (Automated Channel Verification System)

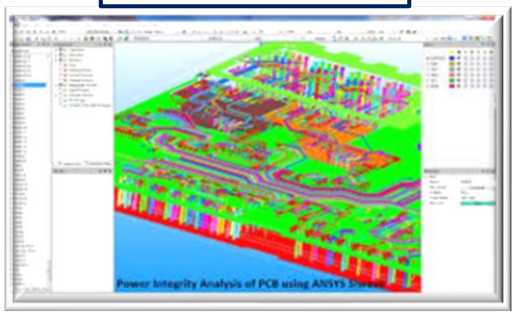
**Memory/SerDes 채널 자동 검증**

## Transient simulation：Basic principle

- **Hybrid time-frequency domain method**
  - **Split Freq./Time domain analysis → Higher efficiency, more flexible**
  - **Eye-diagram, BER, TDR, TDT**

**Hybrid time-frequency domain method**

**3D EM simulation (FEM, MoM, etc.)**

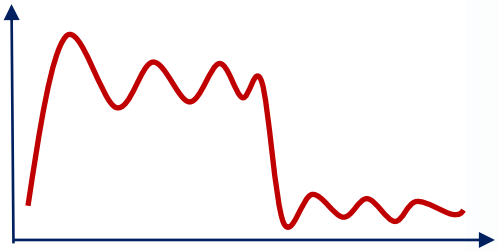


**Frequency response (S-parameter)**

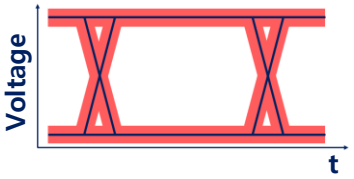
$$\begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{21} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{24} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix}$$

**Freq. to time domain transform**

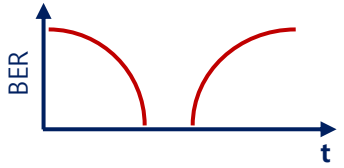
- **IFFT with extrapolation**
- **SPICE model using vector fitting**



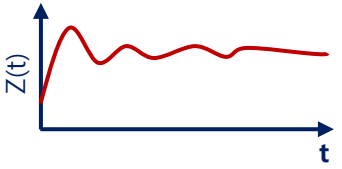
**Time response**



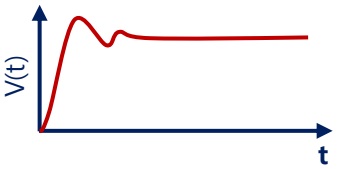

**Eye-diagram**




**Bit error ratio**



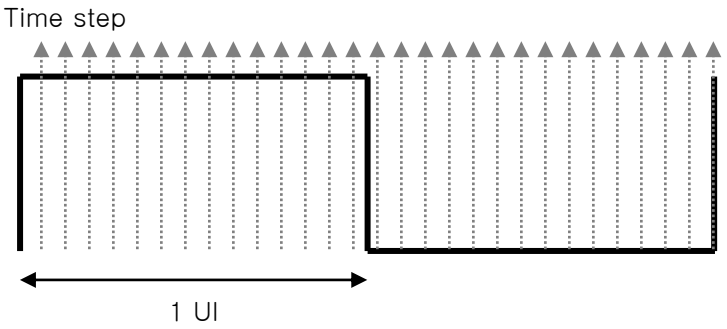

**TDR**

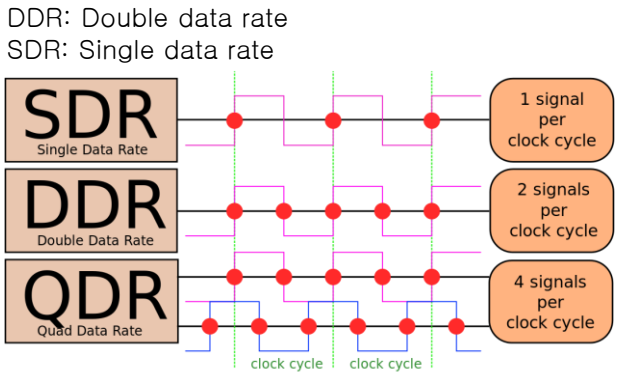



**TDT**

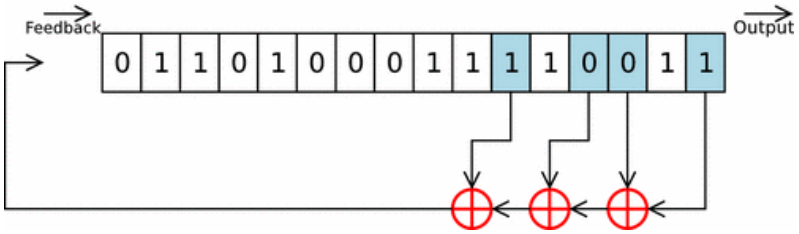
## Transient simulation : Simulation setup

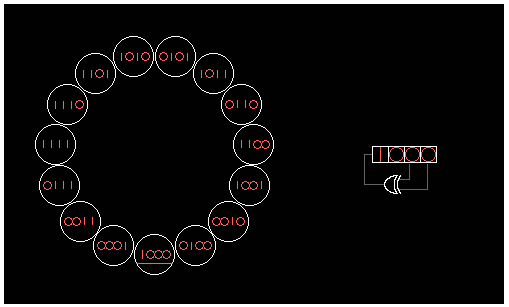
- **Data rate = 1/UI (unit interval)**
- **PRBS : Pseudo random bit sequence -> LFSR: Register length, Seed**
- **Time step : Sampling interval of output waveform**




(이미지 출처: Wikidoc)



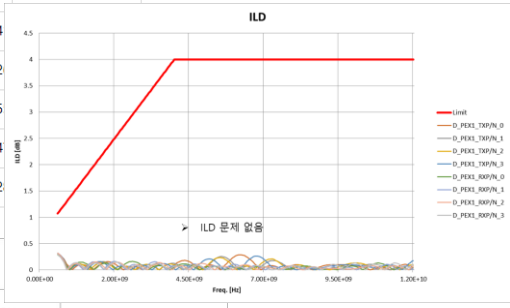



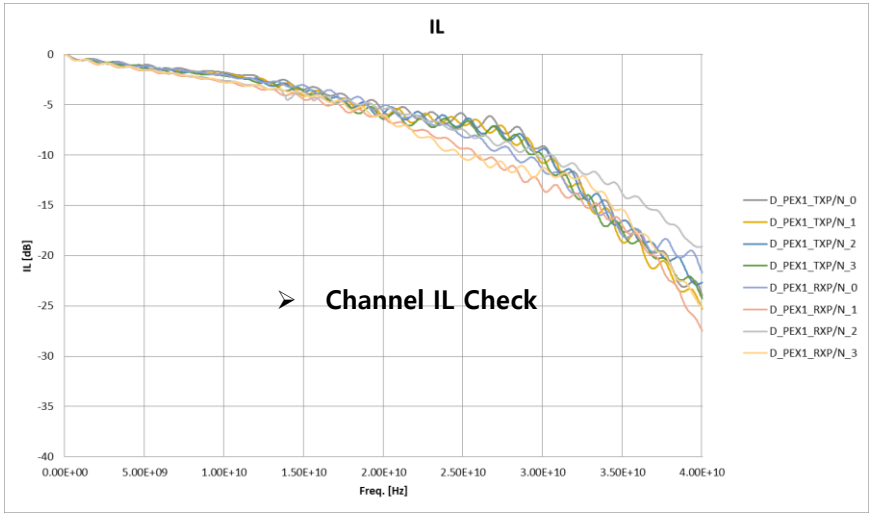
**PRBS => Linear feedback shift register (LFSR)**
**Check Register length, Seed**

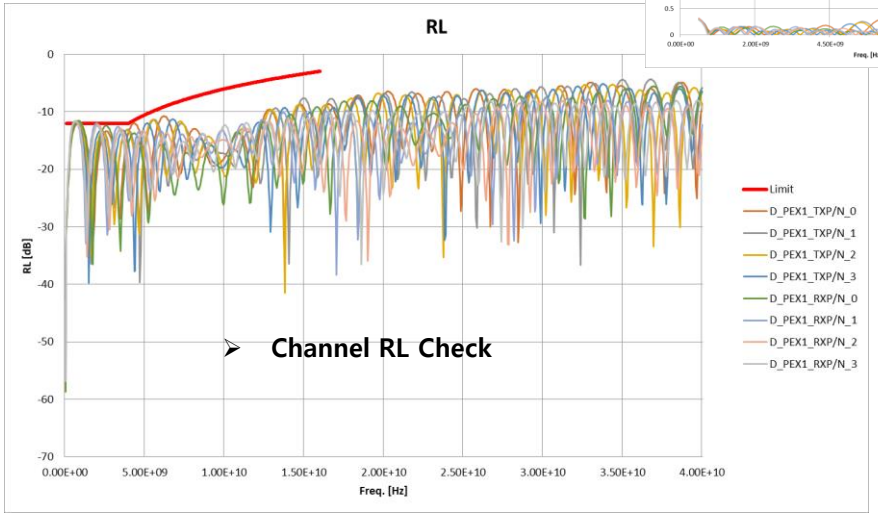
(이미지 출처: 위키피디아)

## Channel Loss Check

| Net Name | Length[mm] | Diff.[mm] | Layer | Width[mm] | Via Num. | Via Stub(Max)[mm] | Cap.[uF] | IL @2.5GHz | IL @5GHz | IL @8GHz | IL @13GHz | IL/100mm @2.5GHz | IL/100mm @5GHz | IL/100mm @8GHz | IL/100mm @13GHz |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D_PEX1_TXP_0 | 47.175 (3.865+43.31) | -0.055 | `TOP` / `TOP` | 0.221 / 0.221 | 0 + 0 | 0 (-)/0 (-) | 0.22 | -0.781 | -1.062 | -1.678 | -2.836 | -1.654 | -2.25 | -3.554 | -6.009 |
| D_PEX1_TXN_0 | 47.23 (3.865+43.365) | | `TOP` / `TOP` | 0.221 / 0.221 | 0 + 0 | 0 (-)/0 (-) | 0.22 | | | | | | | | |
| D_PEX1_TXP_1 | 52.125 (3.865+48.26) | -0.055 | `TOP` / `TOP` | 0.221 / 0.221 | 0 + 0 | 0 (-)/0 (-) | 0.22 | -0.836 | -1.209 | -1.697 | -3.035 | -1.604 | -2.319 | -3.253 | -5.82 |
| D_PEX1_TXN_1 | 52.18 (3.865+48.315) | | `TOP` / `TOP` | 0.221 / 0.221 | 0 + 0 | 0 (-)/0 (-) | 0.22 | | | | | | | | |
| D_PEX1_TXP_2 | 53.096 (3.865+49.231) | -0.055 | `TOP` / `TOP` | 0.221 / 0.221 | 0 + 0 | 0 (-)/0 (-) | 0.22 | -0.834 | -1.259 | -1.714 | -3.159 | -1.569 | -2.369 | -3.226 | -5.946 |
| D_PEX1_TXN_2 | 53.151 (3.865+49.286) | | `TOP` / `TOP` | 0.221 / 0.221 | 0 + 0 | 0 (-)/0 (-) | 0.22 | | | | | | | | |
| D_PEX1_TXP_3 | 56.516 (3.865+52.651) | -0.056 | `TOP` / `TOP` | 0.221 / 0.221 | 0 + 0 | 0 (-)/0 (-) | 0.22 | -0.838 | -1.474 | -1.833 | -2.804 | -1.483 | -2.606 | -3.24 | |
| D_PEX1_TXN_3 | 56.572 (3.865+52.707) | | `TOP` / `TOP` | 0.221 / 0.221 | 0 + 0 | 0 (-)/0 (-) | 0.22 | | | | | | | | |
| D_PEX1_RXP_0 | 52.622 | -0.074 | `BOTTOM` | 0.221 | 1 | 0 (0-0) | - | -0.922 | -1.174 | -1.717 | -2.729 | -1.751 | -2.229 | -3.2 | |
| D_PEX1_RXN_0 | 52.696 | | `BOTTOM` | 0.221 | 1 | 0 (0-0) | - | | | | | | | | |
| D_PEX1_RXP_1 | 67.613 | -0.063 | `BOTTOM` | 0.221 | 1 | 0 (0-0) | - | -0.893 | -1.58 | -2.202 | -3.434 | -1.321 | -2.336 | -3.25 | |
| D_PEX1_RXN_1 | 67.676 | | `BOTTOM` | 0.221 | 1 | 0 (0-0) | - | | | | | | | | |
| D_PEX1_RXP_2 | 65.329 | -0.063 | `BOTTOM` | 0.221 | 1 | 0 (0-0) | - | -0.921 | -1.623 | -2.253 | -3.509 | -1.41 | -2.483 | -3.44 | |
| D_PEX1_RXN_2 | 65.392 | | `BOTTOM` | 0.221 | 1 | 0 (0-0) | - | | | | | | | | |
| D_PEX1_RXP_3 | 66.375 | -0.079 | `BOTTOM` | 0.221 | 1 | 0 (0-0) | - | -0.895 | -1.559 | -2.144 | -3.435 | -1.347 | -2.347 | -3.22 | |
| D_PEX1_RXN_3 | 66.454 | | `BOTTOM` | 0.221 | 1 | 0 (0-0) | - | | | | | | | | |

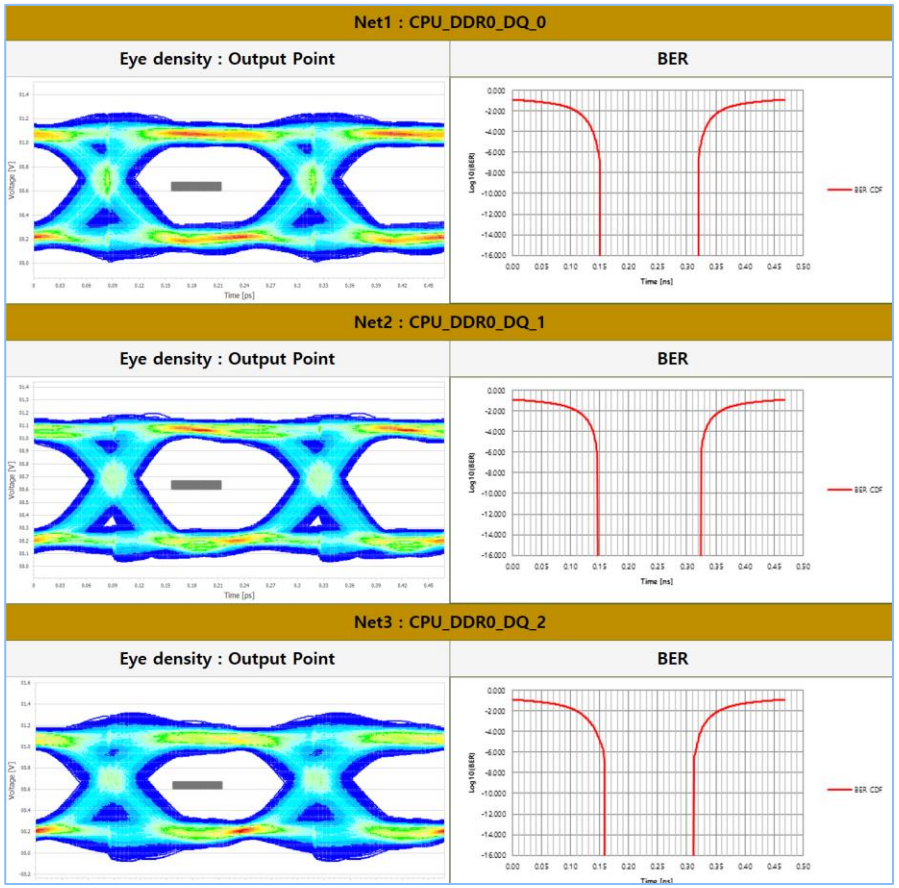


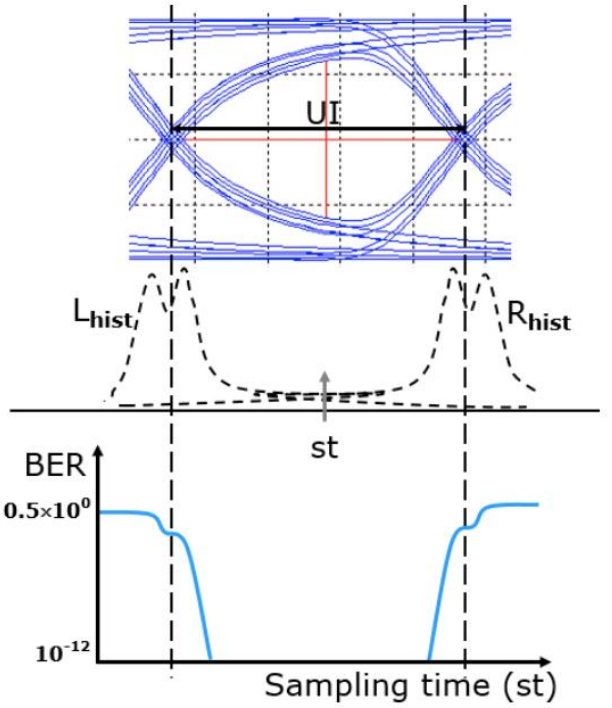



## Transient simulation : Eye-diagram, BER, Bathtub

- **Eye-diagram: UI 단위로 출력 파형 겹쳐 그림**
- **BER (Bit error ratio) : 출력 파형의 오류 확률 표현**
- **Bathtub : BER 결과를 도식화 -> BER의 CDF (Cumulative distribution function) 차트**




Eye-diagram, BER (Bathtub)

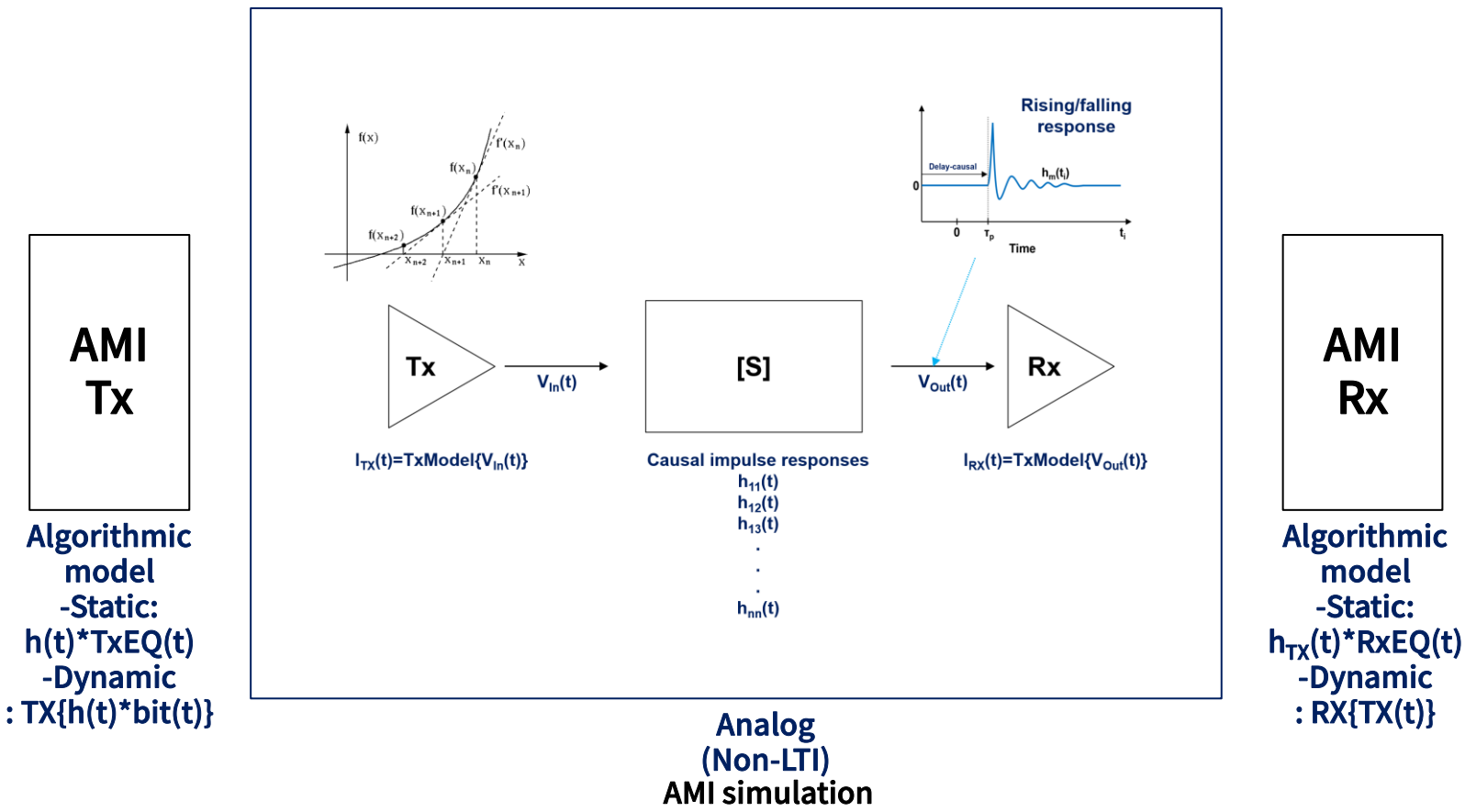



**Eye diagram, jitter histogram, BER bathtub curve의 관계도**

(이미지 출처: 김진국, 고속 신호전송 시 Bit Error Rate(BER)의 확률적 예측기술)

## AMI Simulation : Differential signaling (SerDes) : Basic principle

- **Hybrid type analysis: Non-LTI (Transient sim.) + LTI (AMI model)**
  - **Tx/Rx driver + Channel 의 Impulse response 추출**
  - **AMI model에 Impulse response를 입력하여 분석 결과 도출**
    **: Impulse response의 정확도가 분석 결과에 가장 큰 영향을 미침**



## AMI Simulation : Differential signaling (SerDes) : Tx/Rx equalizers

- **Static EQ: 입력 파형의 특성과 상관없이 동일한 특성으로 equalization**
  - **FFE (Feed-forward equalization), CTLE (Continuous time linear equalization)**
- **Dynamic EQ: 입력 파형의 특성이 equalization 결과에 영향**
  - **DFE (Decision feedback equalizer)**

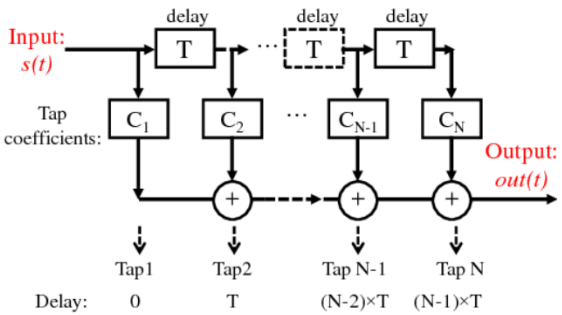
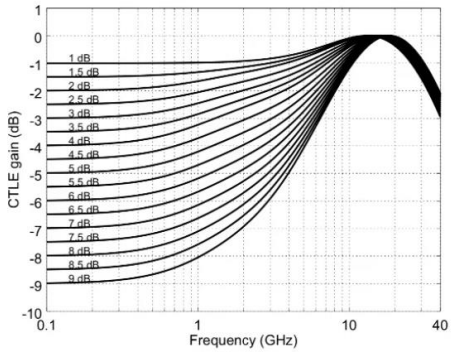


Figure 1: Schematic of a feed-forward equalizer.

FFE 기본구조

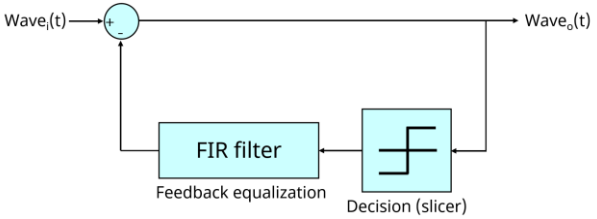
(이미지 출처: X. Li, Wireless Visible Light Communications Employing Feed-Forward Pre-Equalization and PAM-4 Modulation)

$$H(f) = \frac{GP_1P_2P_{LF}}{Z_1Z_{LF}} \times \frac{j2\pi f + Z_1}{(j2\pi f + P_1)(j2\pi f + P_2)} \times \frac{j2\pi f + Z_{LF}}{j2\pi f + P_{LF}}$$




CTLE 기본구조

(이미지 출처: Jeffry. W, Understanding the math of CTLE definition in IEEE 802.3 which used by 50G PAM4 ( 200GAUI-4/400GAUI-8) )




DFE 기본구조

## AMI Simulation : Differential signaling (SerDes) : AMI parameters

- **Reserved_parameters: AMI 표준 공통 설정값**
  - **Init_Return_Impulse, GetWave_Exists, Ignore_Bits, Jitter등**
- **Model_Specific: 해당 모델에만 해당되는 설정값**
  - **Equalizer 설정**

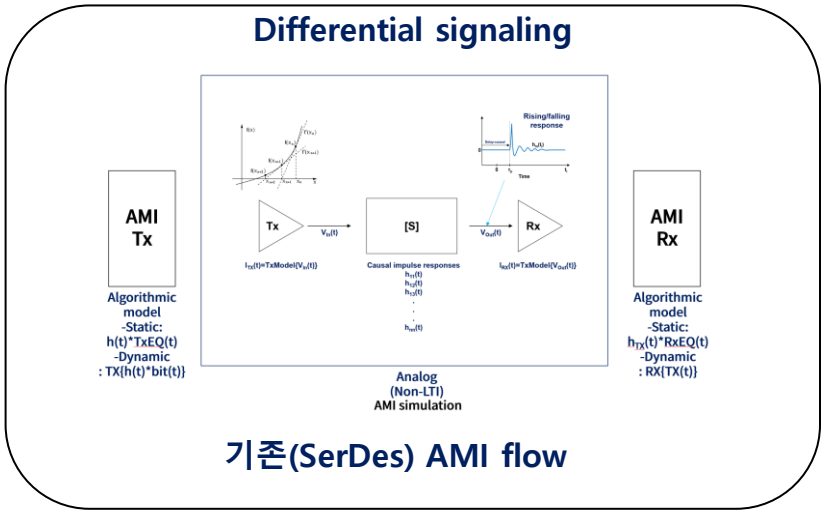
```
(Reserved_Parameters
   (AMI_Version (Usage Info) (Type String) (Value "6.1")
      (Description "The first IBIS version that supports this AMI file. Results may not be valid in earlier
   )
   (Init_Returns_Impulse (Usage Info) (Type Boolean) (Value True)
      (Description "When True, this model supports AMI_Init (statistical) simulation.")
   )
   (GetWave_Exists (Usage Info) (Type Boolean) (Value True)
      (Description "When True, this model supports AMI_GetWave (time domain) simulation.")
   )
   (Max_Init_Aggressors (Usage Info) (Type Integer) (Value 50)
      (Description "The number of crosstalk aggressors supported by this model.")
   )
   (Modulation (Usage In) (Type String) (Value "NRZ")
      (Description "Specifies whether the model will operate as NRZ or PAM4.")
   )
   (Tx_Dj (Usage Info) (Type UI) (Value 0.075)
      (Description "Tx Bounded Jitter in UI")
   )
   (Tx_Rj (Usage Info) (Type UI) (Value 0.0057)
      (Description "Tx Random Jitter in UI")
   )
)
```

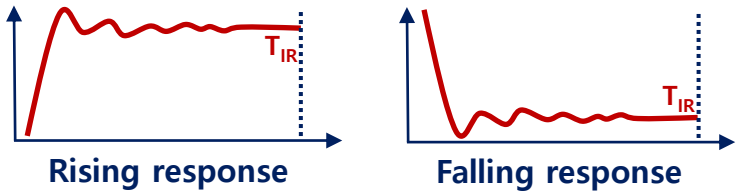
```
(Reserved_Parameters
   (Ignore_Bits (Usage Info) (Type Integer) (Default 0)
      (Description "Ignore four bits to fill up tapped delay line."))
   (Max_Init_Aggressors (Usage Info) (Type Integer) (Default 0)
      (Description "Number of aggressors is actually unlimited."))
   (Init_Returns_Impulse (Usage Info) (Type Boolean) (Default True)
      (Description "Both impulse and parameters_out returned."))
   (GetWave_Exists (Usage Info) (Type Boolean) (Default True)
      (Description "GetWave is well and truly provided in the module."))
   (Use_Init_Output (Usage Info) (Type Boolean) (Default False)
      (Description "GetWave and Init function independent of each other."))
)
(Model_Specific
   (DFE_vth (Usage In) (Type Float) (Format Range 0 0.332 1.13) (Default 0.731)
         (Description "the middle of Vswing at RX pad"))
   (DFE_coeffs
      (Description "DFE 1-tap coeff in Volt")
      (1 (Usage In) (Type Tap) (Format Range 0 0.000 1.260) (Default 0.630)
                    (Description "1st tap coeff in Volt"))
      (2 (Usage In) (Type Tap) (Format Range 0 0.000 0.630) (Default 0.315)
                    (Description "2nd tap coeff in Volt. Set to 0 for 1-tap DFE"))
      (3 (Usage In) (Type Tap) (Format Range 0.000 0.000 0.001) (Default 0.000)
                    (Description "Reserved for Synopsys internal usage"))
      (4 (Usage In) (Type Tap) (Format Range 0.000 0.000 0.001) (Default 0.000)
                    (Description "Reserved for Synopsys internal usage"))
   ) | end DFE_coeffs
) | end Model Specific
```

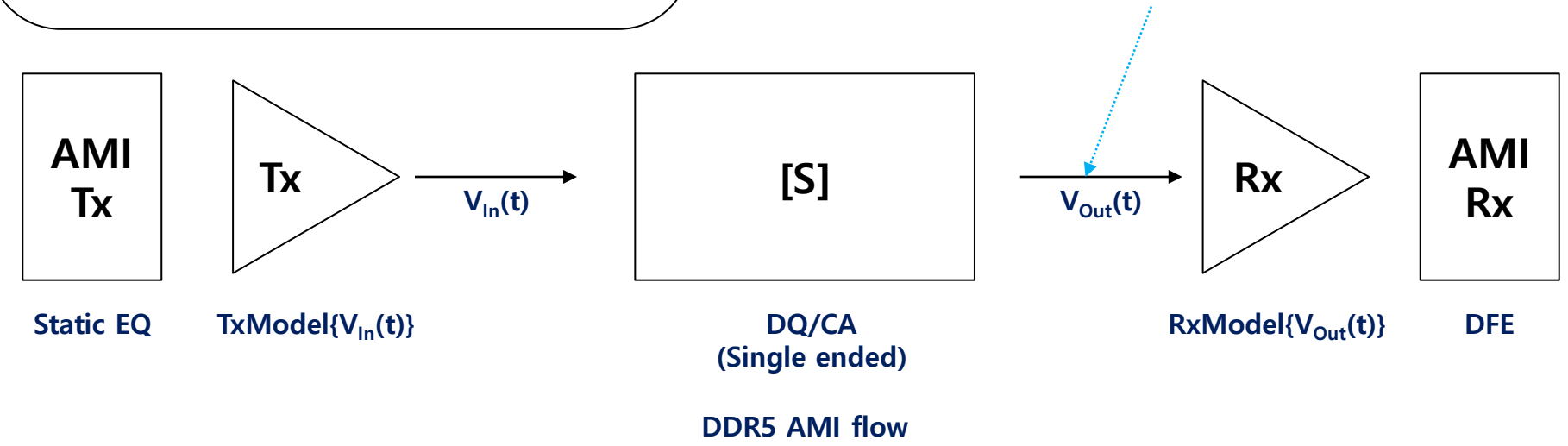
**Tx, Rx ignore bits를 Simulation 설정에 반영**
**-> Bit length, offset time**

## AMI Simulation : Single-ended (DDR5): Basic principle

- Transient simulation -> Rising/falling response 추출
  - SerDes AMI: Single edge response 이용하여 해석 (Rising/falling 특성 동일)
  - DDR5는 Single ended로 Rising/Falling 2가지 종류의 response 이용 필요

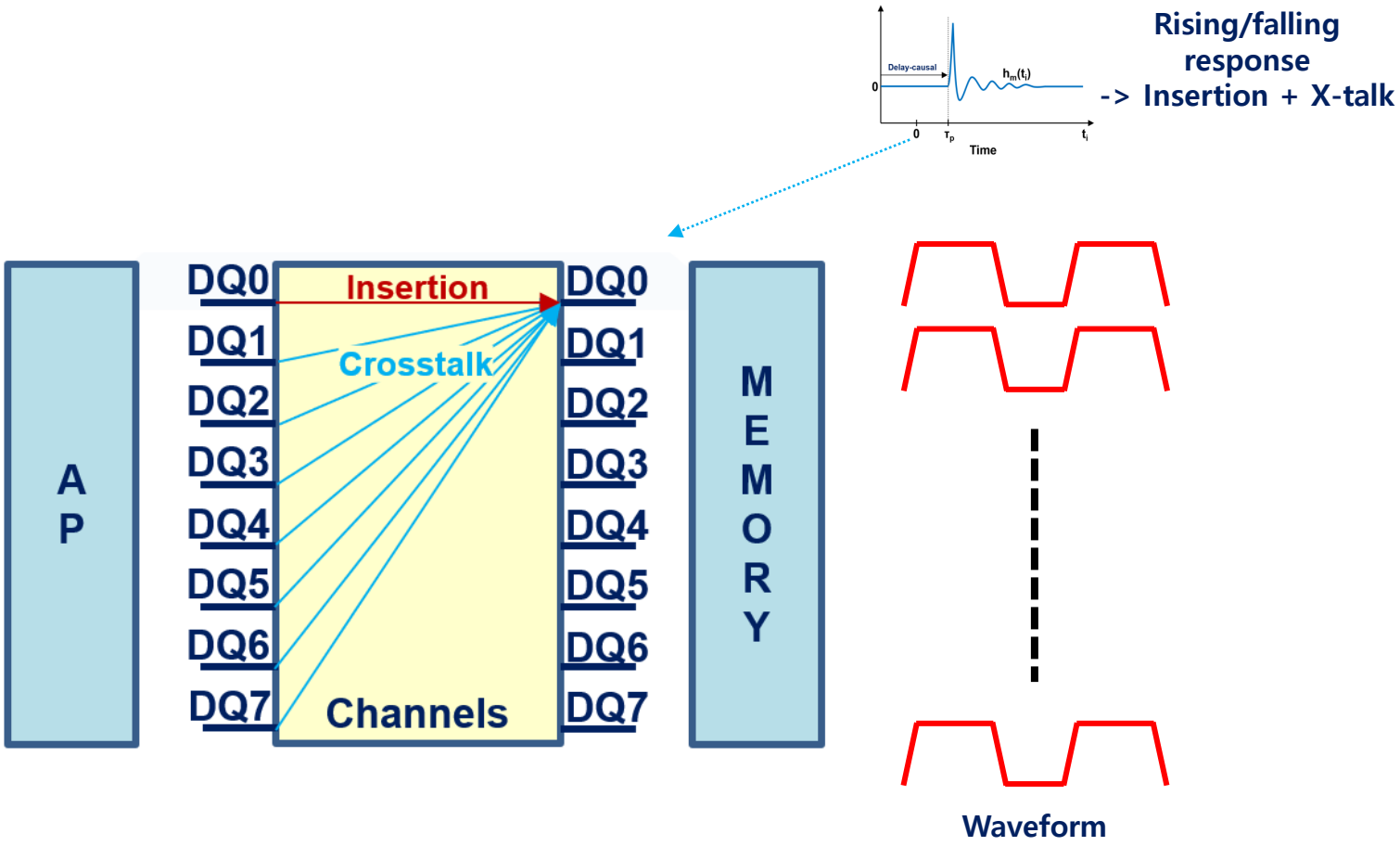


## AMI Simulation : Single-ended (DDR5) : Basic principle

- X-talk response 추출
  - ➢ 모든 Net의 X-talk 성분에 대한 Response 추출: Transient simulation 자동화 적용
  - ➢ 각 Net별 X-talk이 포함된 Waveform 합성



## AMI Simulation : Single-ended (DDR5) : DC offest

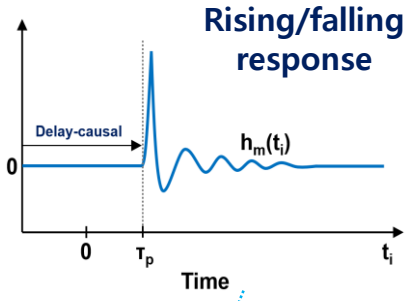
- **SerDes AMI: Differential signaling으로 DC offset이 없음 (0V 기준 Swing)**
- **Single-ended AMI: DC offset 정보 필요**
  - **Rising/falling impulse response와 함께 DC offset 값 추출 및 AMI 출력에 적용 기능 필요**

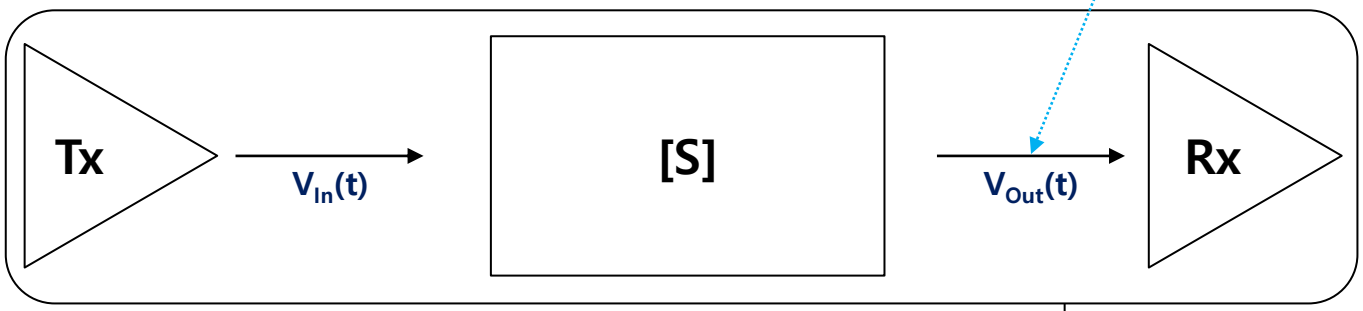
*Parameter:* DC_Offset
*Required:* ~~No, and illegal~~ before AMI_Version 7.1
*Direction:* Rx
*Descriptors:*

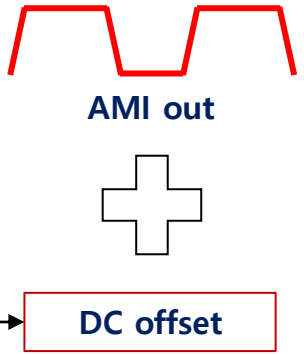
| | |
|---|---|
| Usage: | In |
| Type: | Float |
| Format: | Value |
| Default: | <numeric_literal> |
| Description: | <string> |

*Definition:* The input value of DC_Offset is the mean value of the steady state high and low voltages of the analog channel step response at the Rx pad.

*Usage Rules:* If the impulse response was generated by differentiating the analog channel step response, then the input value of DC_Offset should be the same as the average of the step response initial and final voltages.




The EDA tool ignores the DC_Offset value specified in the .ami file. It is the responsibility of the EDA tool to determine the input value of DC_Offset. The EDA tool may use any method to do this. The EDA tool may use the input value of DC_Offset to post process data returned by the AMI model to graphically compare the waveform output of Rx AMI_GetWave to the input waveform without the DC_Offset subtracted.

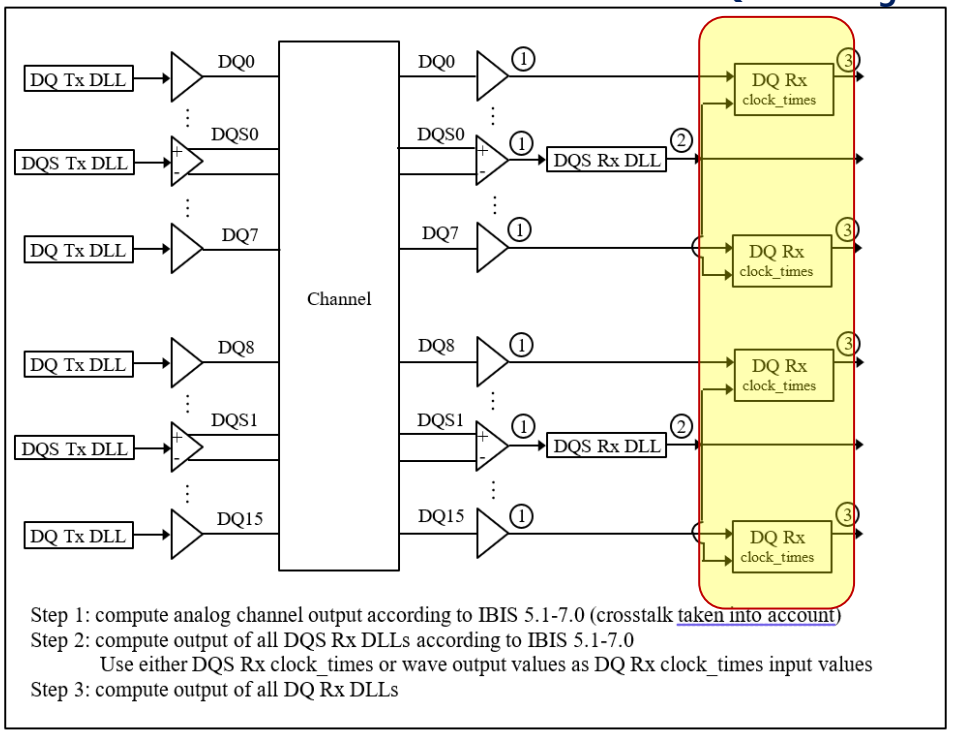
## AMI Simulation : Single-ended (DDR5) : Forward clocking

- **SerDes AMI: CDR을 이용하여 내부에서 clocking 신호 생성 (출력 파라미터: clock_times)**
- **Single-ended AMI: External clock 신호(DQS)를 이용하여 signal clocking (DQ)**

**BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)**

| | |
|---|---|
| **BIRD NUMBER:** | 204 |
| **ISSUE TITLE:** | DQ_DQS GetWave Flow for Clock Forwarding Modeling |
| **REQUESTOR:** | Walter Katz, The MathWorks |
| | Fangyi Rao, Keysight |
| | Wendem Beyene, Intel |
| | Ambrish Varma, Cadence |
| **DATE SUBMITTED:** | April 22, 2020 |
| **DATE REVISED:** | |
| **DATE ACCEPTED:** | June 26, 2020 |

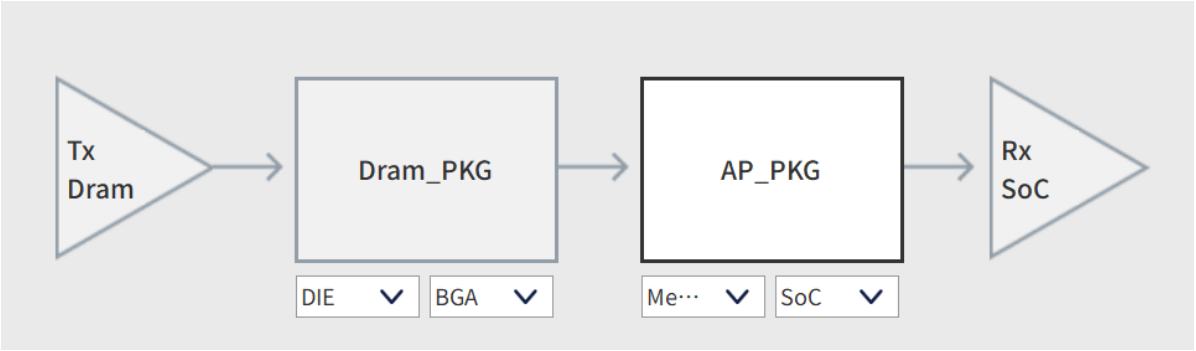
**Rx DFE w DQS clocking**



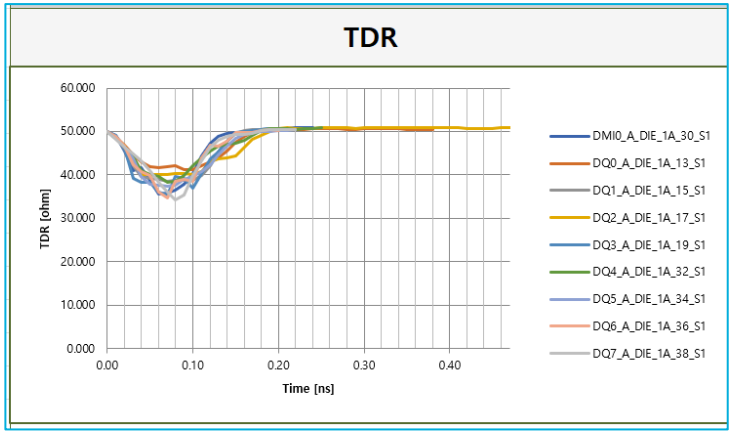

Step 1: compute analog channel output according to IBIS 5.1-7.0 (crosstalk taken into account)
Step 2: compute output of all DQS Rx DLLs according to IBIS 5.1-7.0
Use either DQS Rx clock_times or wave output values as DQ Rx clock_times input values
Step 3: compute output of all DQ Rx DLLs

## AMI Simulation : DDR simulation (Transient)

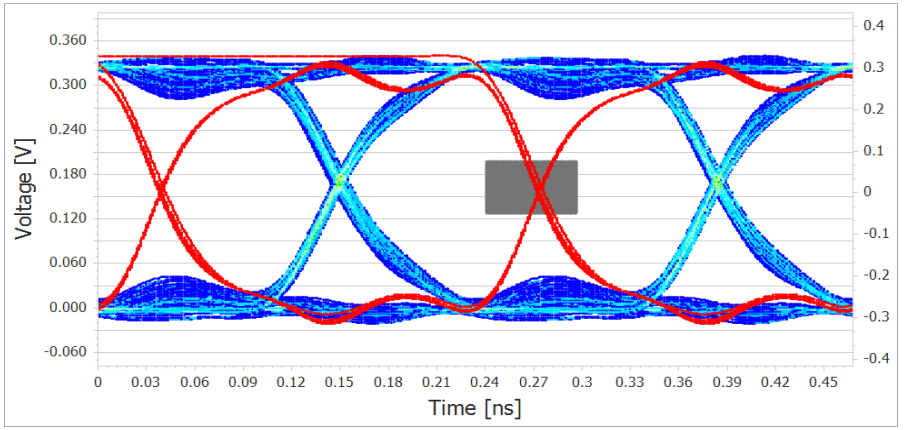
- **IBIS model + Dram pkg + SoC pkg 구성**
- **Write mode, 4266Mbps (Byte0/1 + CA)**
- **Basic SI + Eye-diagram report**




**Channel configuration**




**Basic SI results**
**(TDR, TDT etc.)**

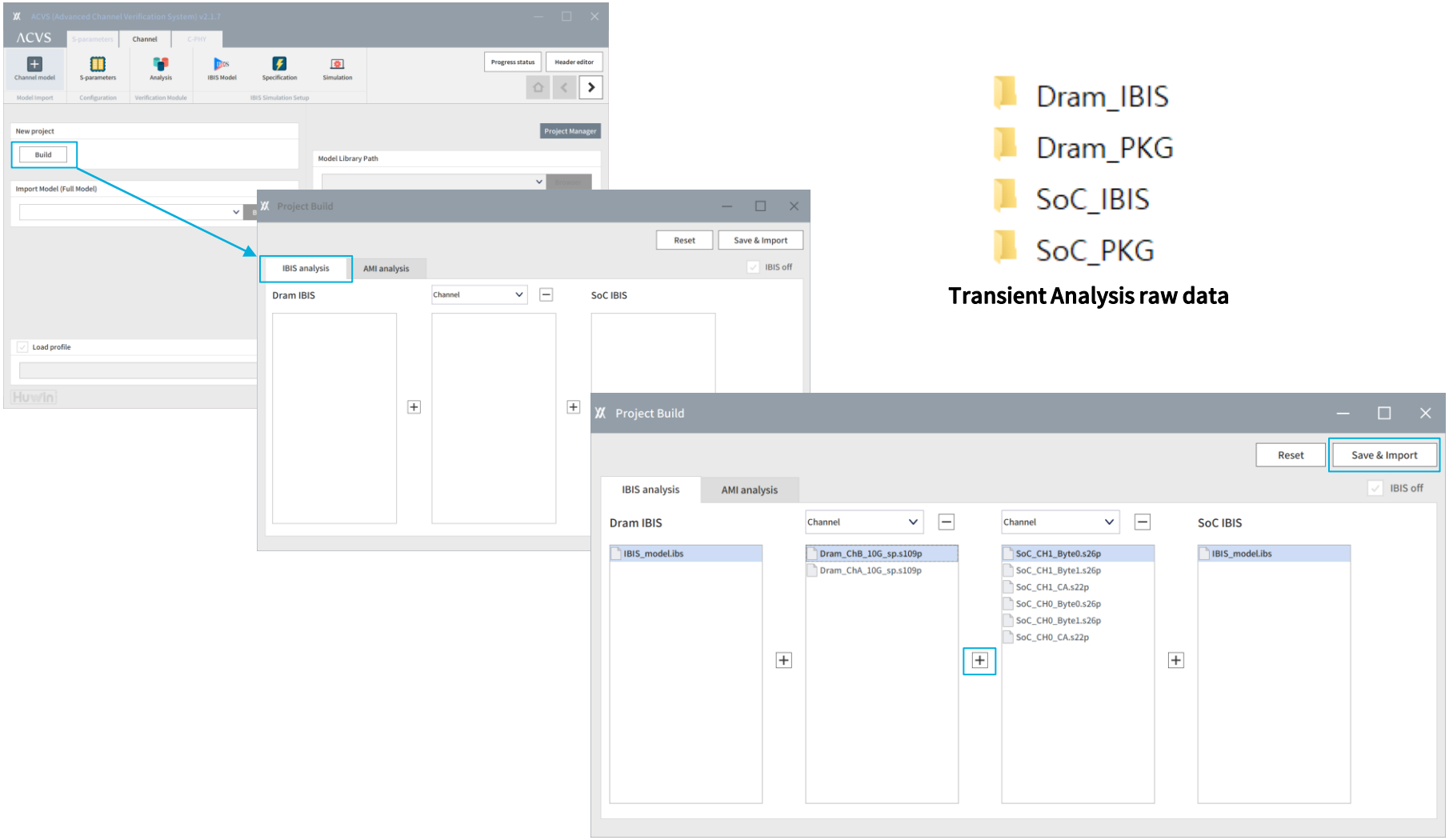



**Eye-diagram results**

## Transient Simulation Build project :

- **Build project**

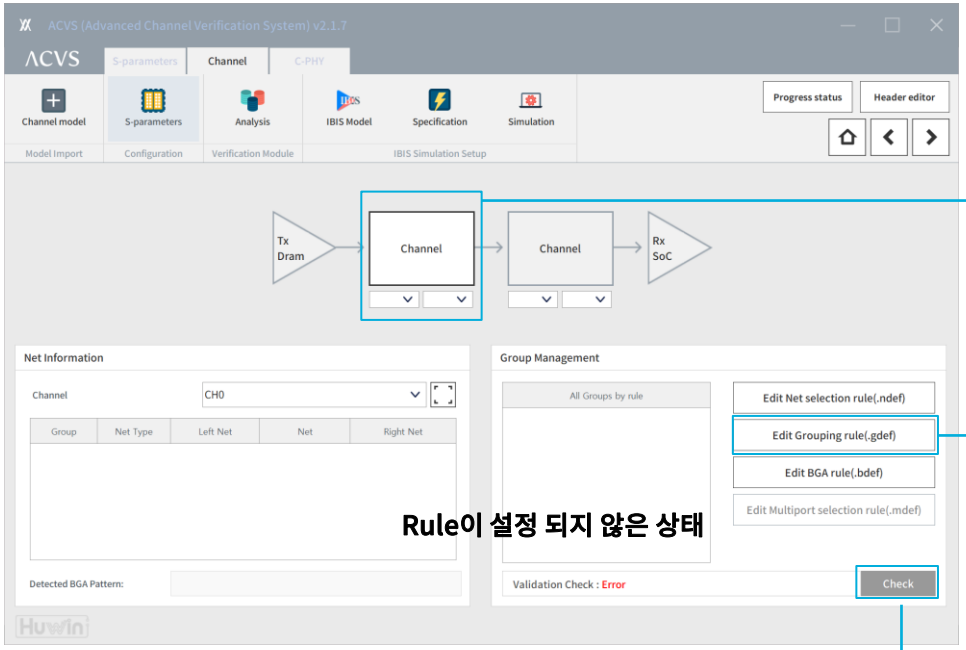
➢ **Build -> IBIS analysis -> + channel -> Drag IBIS, Snp files -> Save & Import**



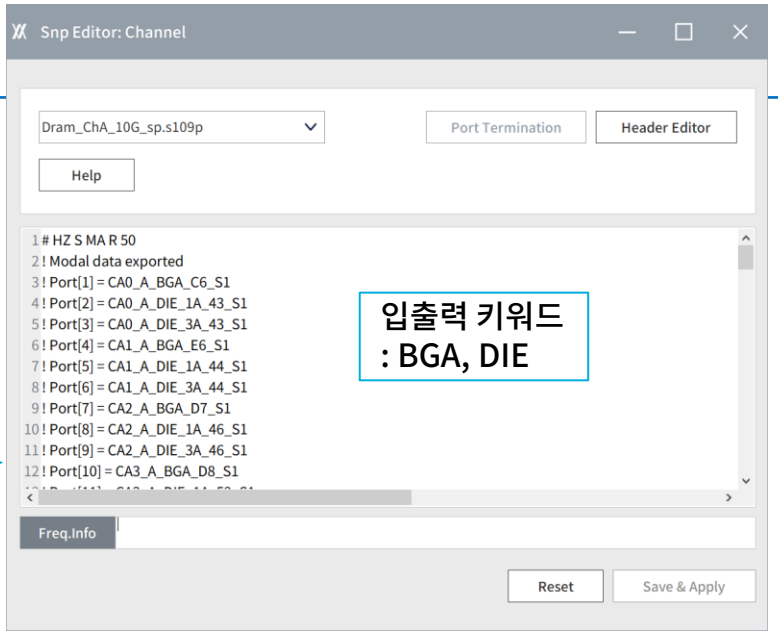

**Transient Analysis raw data**

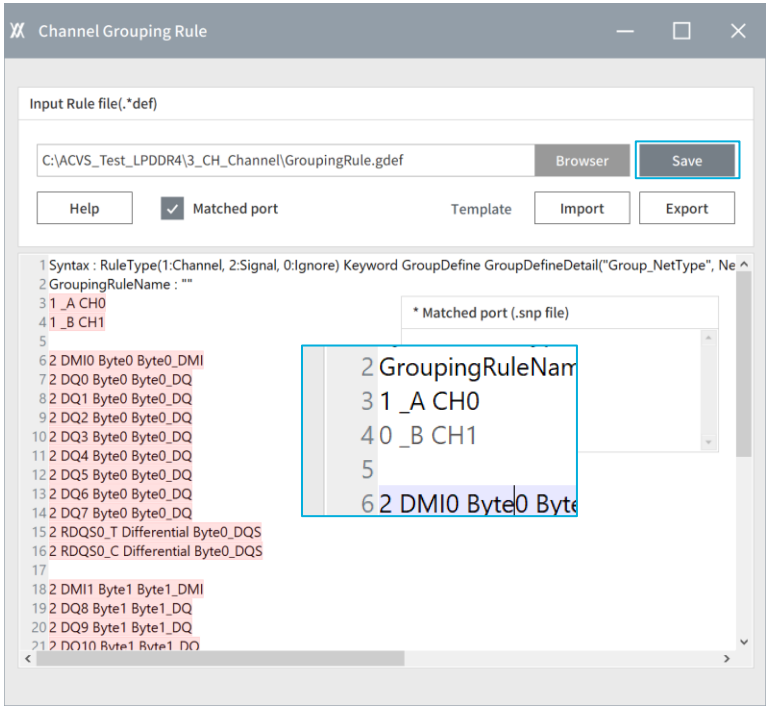
## Transient Simulation : Channel configuration

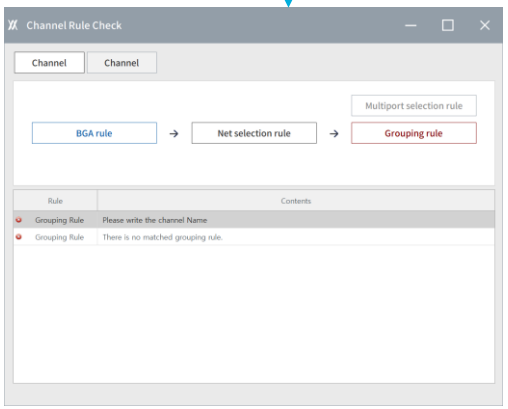
- **Channel configuration by rule**
  - ➢ **모든 Snp file의 net 연결 및 termination 처리**




**Rule이 설정 되지 않은 상태**




**<Rule 설정 순서>**
**1. BGA rule** : net의 입출력 관련 키워드 설정
(ex. BGA, DIE)

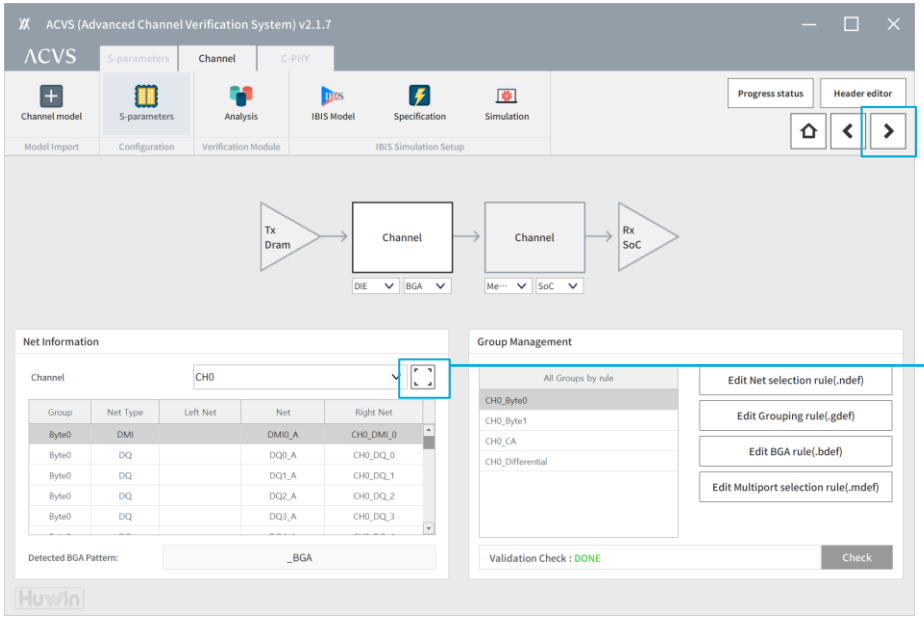
**2. Grouping rule** : net의 분류화
-> Channel, Byte, CA 로 분류

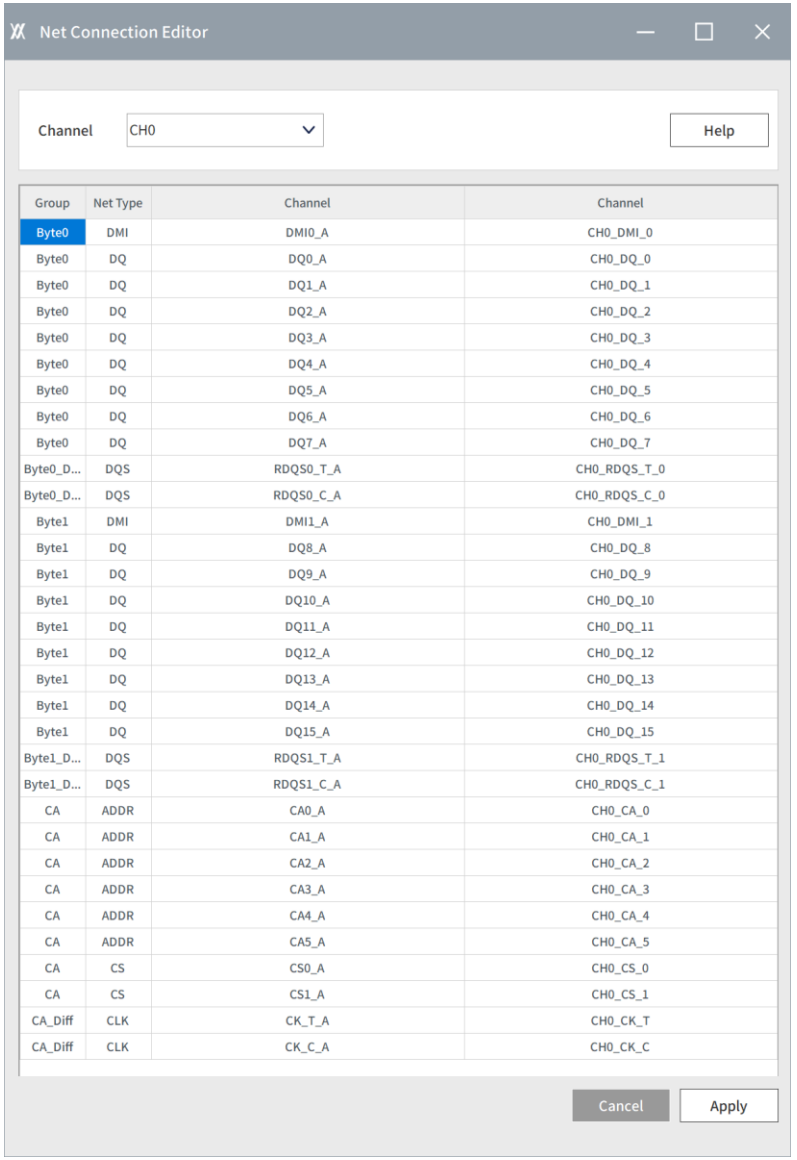
**3. Net selection rule** : 비 분석 대상 net의 설정
(생략가능)

**4. Multiport rule** : 다수의 DIE 조건에서 선택 DIE 설정 (생략가능)

## Transient Simulation : Channel configuration

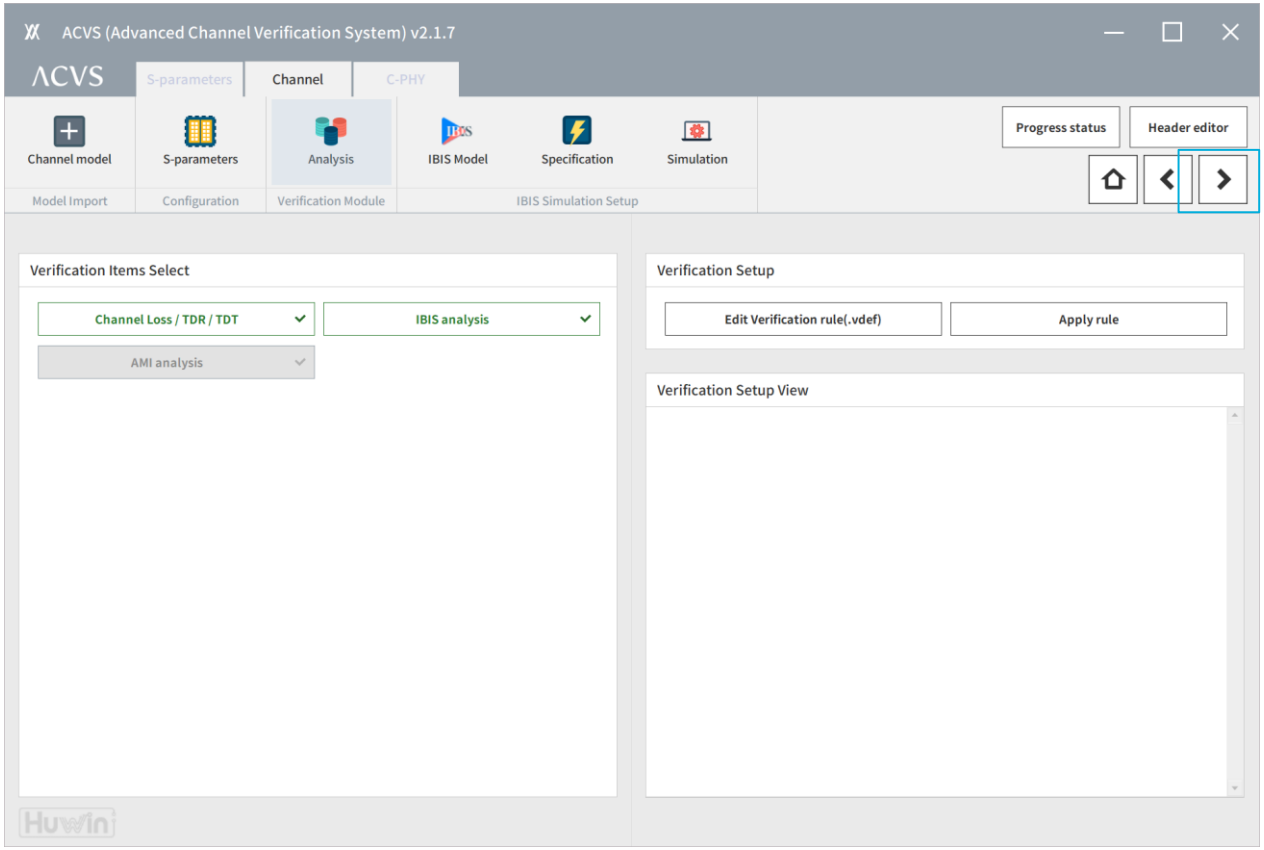
- 채널 구성 확인



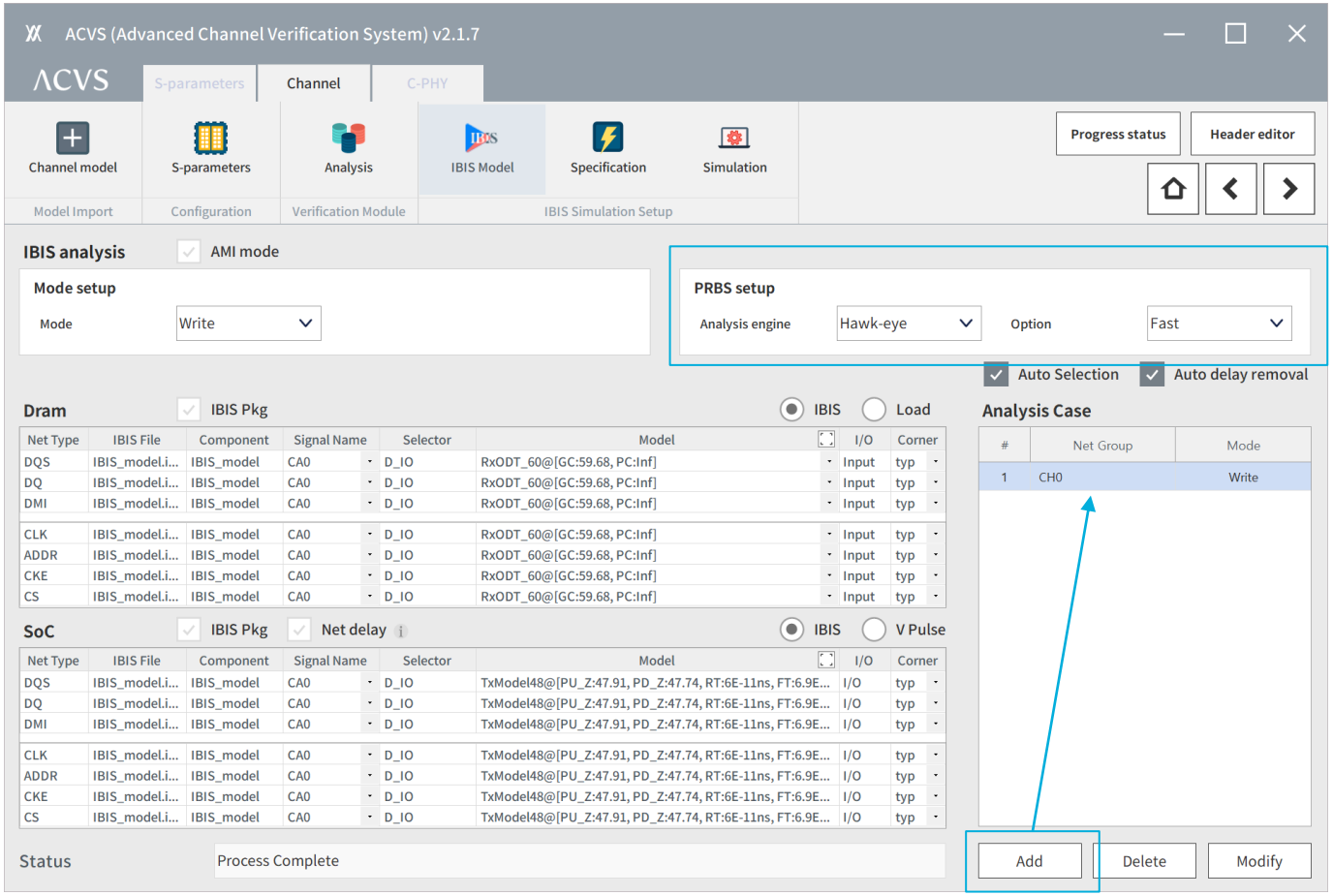
## Transient Simulation : 설정

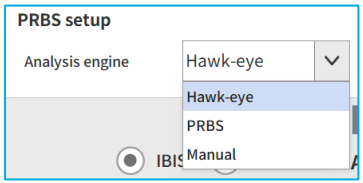
- **Simulation 설정**
  - **Basic SI, IBIS simulation**



## Transient Simulation :

- IBIS 설정
  - Dram: RxODT_60 선택, SoC: TxModel48 선택
  - Write mode 선택, Hawk-eye Fast 선택
  - 'Add' click




**PRBS setup**

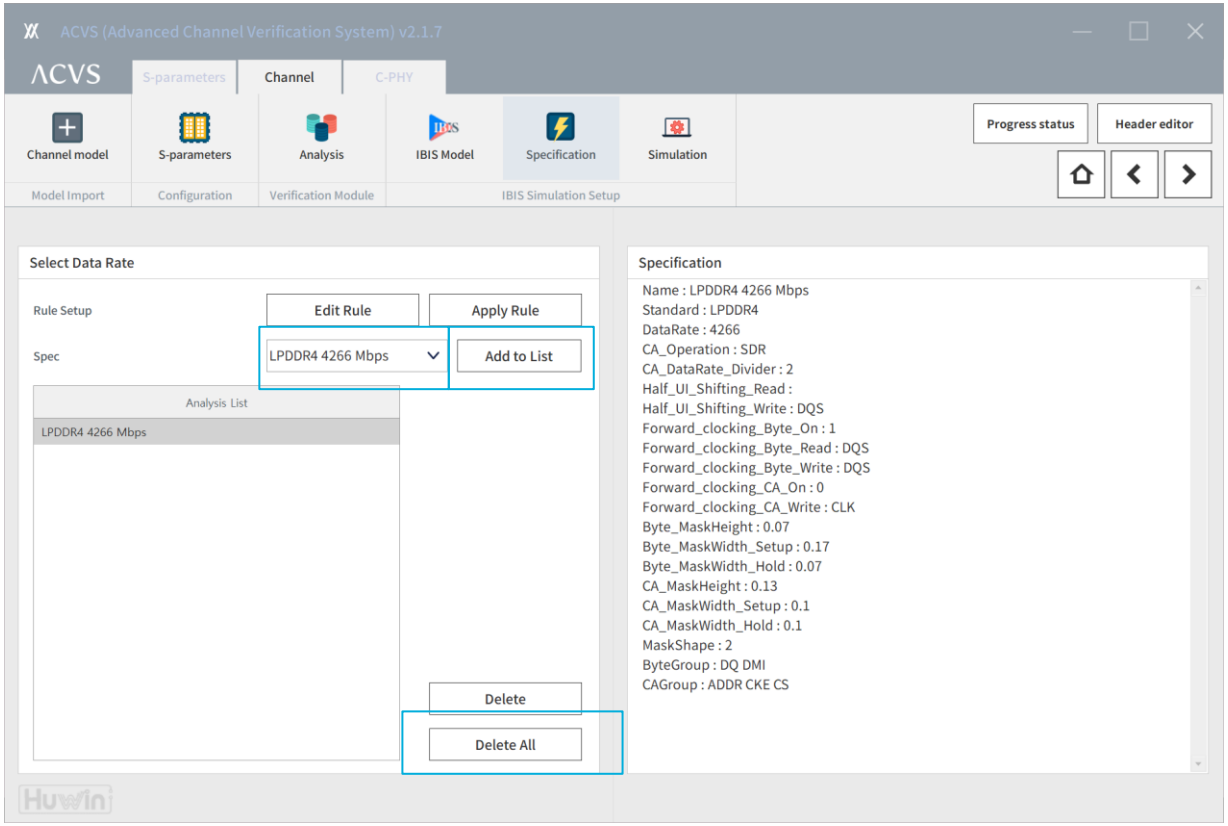
**1) Hawk-eye**
**: Pseudo-worst bit pattern (Fast/Optimal/Strict)**

**2)PRBS**
**: Linear feedback shift register**

**3) Manual**
**: User bit pattern**

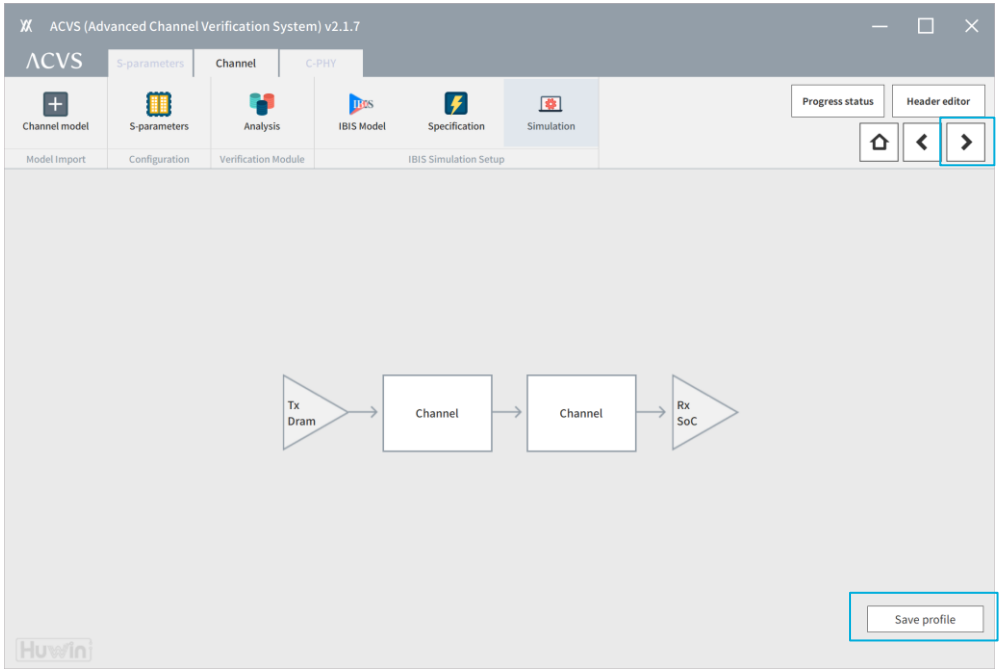
## Transient Simulation : 분석 선택

- Data rate, Mask, 기타 설정

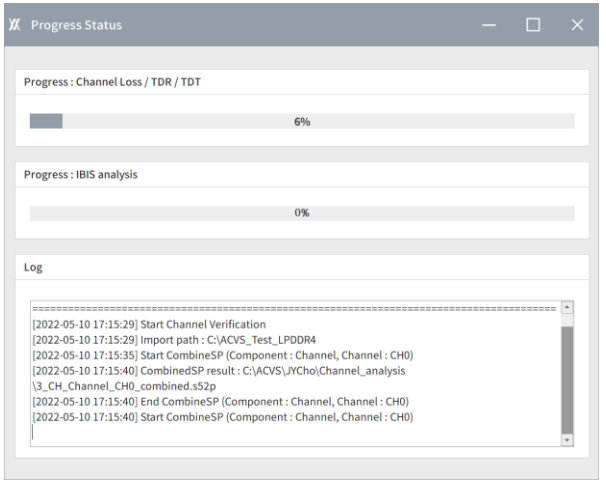


## Transient Simulation : 분석 실행

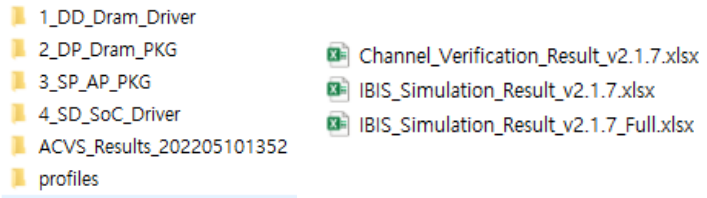
- **Run**
  - ➢ **현재 설정 저장: Save profile click**




**profile 저장 및 Run**



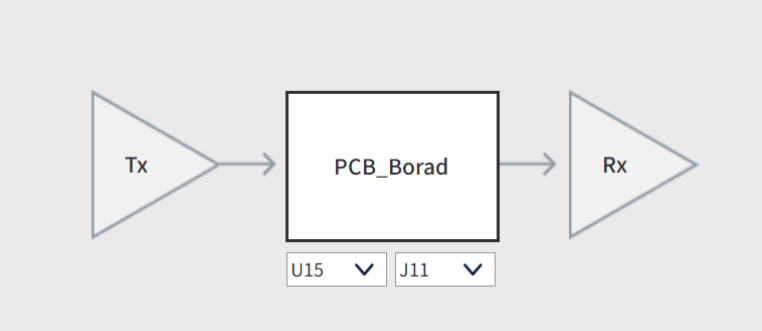

**Simulation 진행**



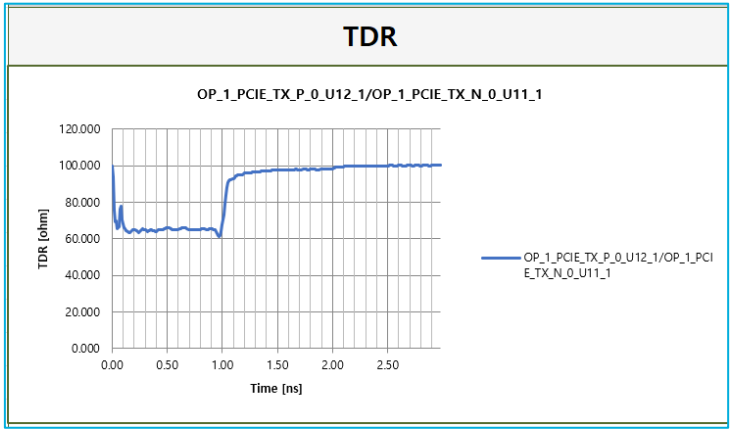

**Report 자동 생성**

## Transient Simulation : PCIe Gen5 (Differential AMI)

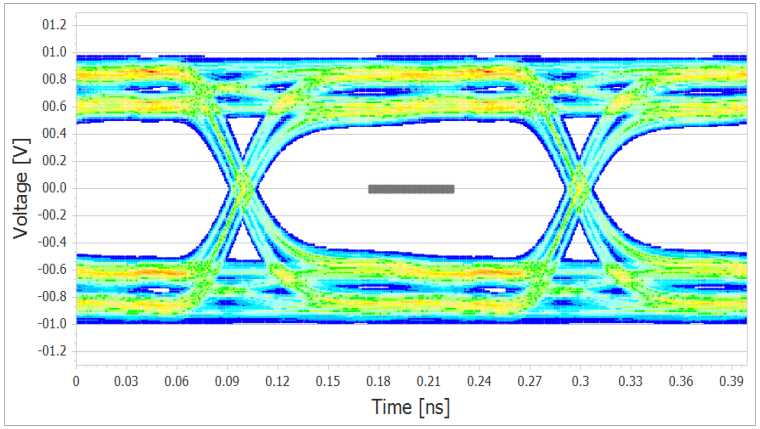
- **AMI model + PCB 구성**
- **Basic SI + Eye-diagram report**




**Channel configuration**




**Basic SI results (TDR, TDT etc.)**

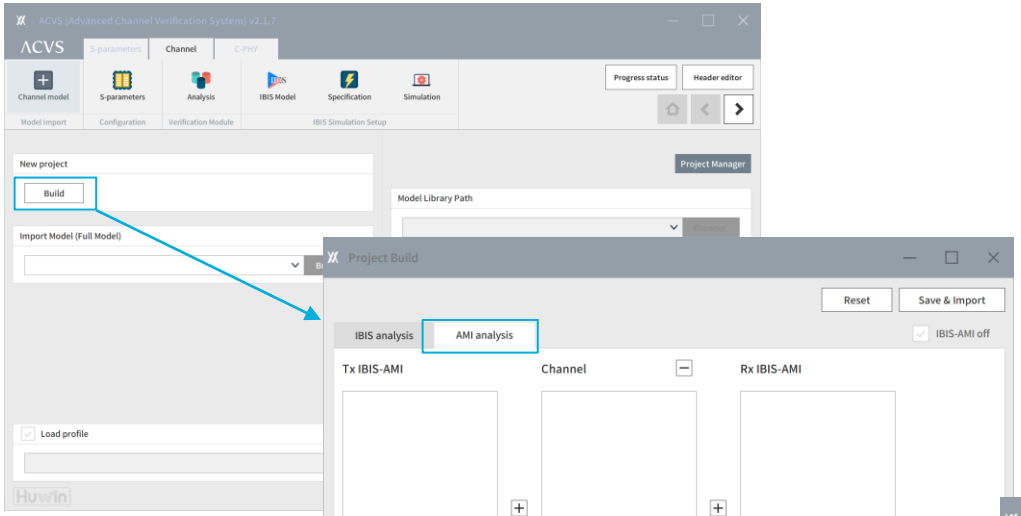


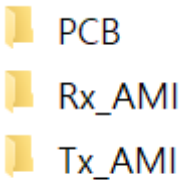

**Eye-diagram results**

## Transient Simulation : PCIe Gen5 (Differential AMI)

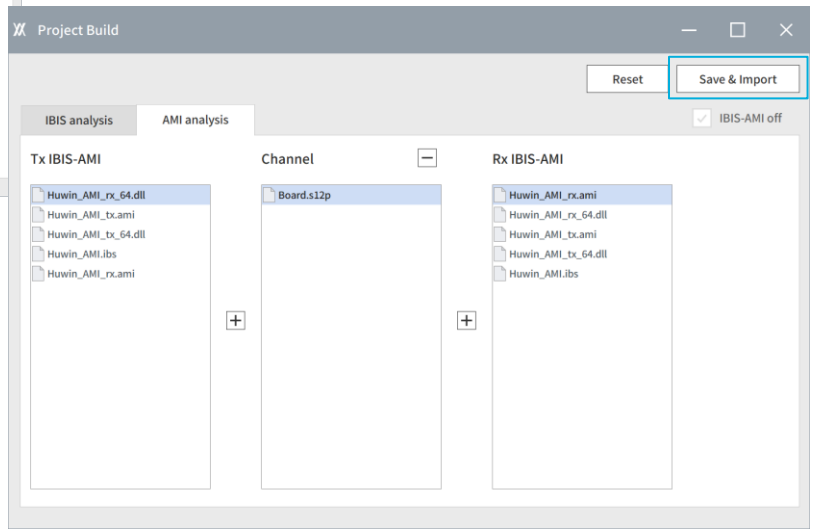
- **Build project**

➢ **Build -> AMI analysis -> + channel -> Drag IBIS, Snp files -> Save & Import**



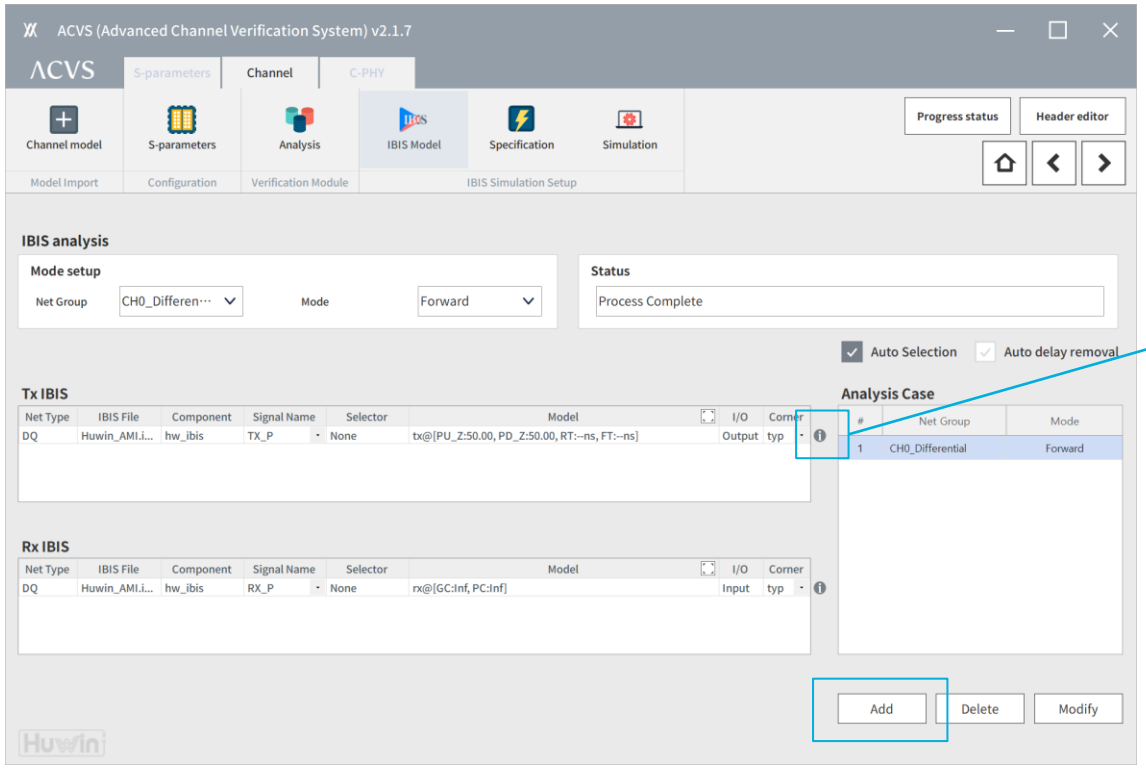



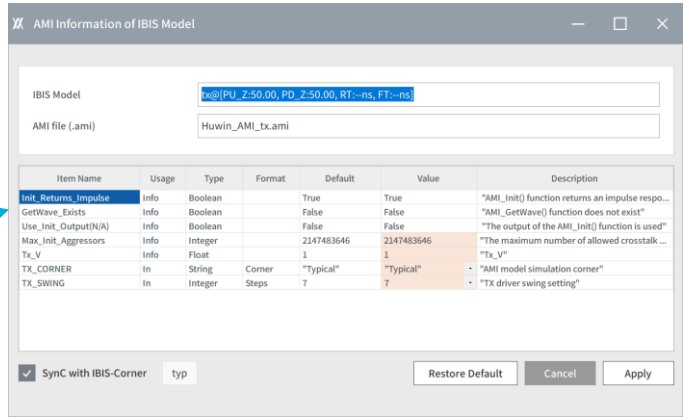

**PCIe raw data**



## Transient Simulation : PCIe Gen5 (Differential AMI)

- **AMI 설정**
  - **IBIS 모델 선택 및 AMI 설정 후 'Add' click**

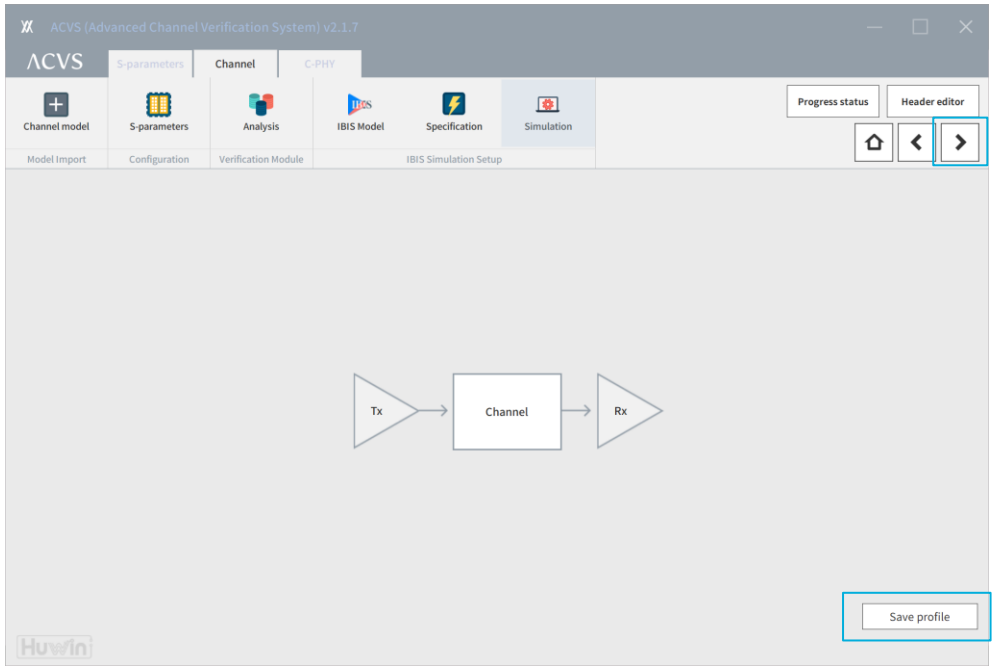


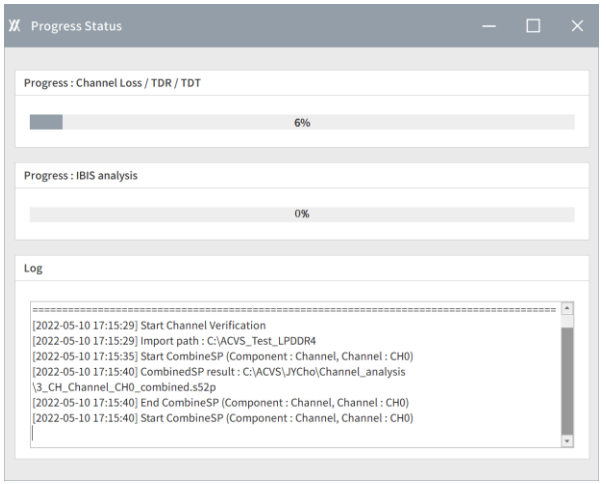

**AMI 설정 값 확인 및 변경**

## Transient Simulation : PCIe Gen5 (Differential AMI)

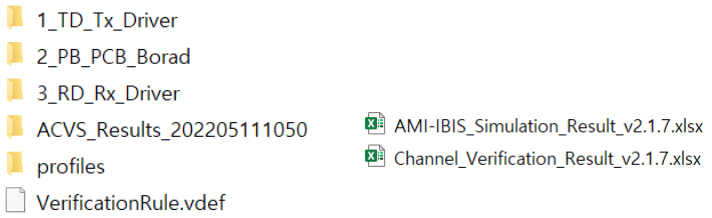
- **Run**
  - **현재 설정 저장: Save profile click**




**profile 저장 및 Run**



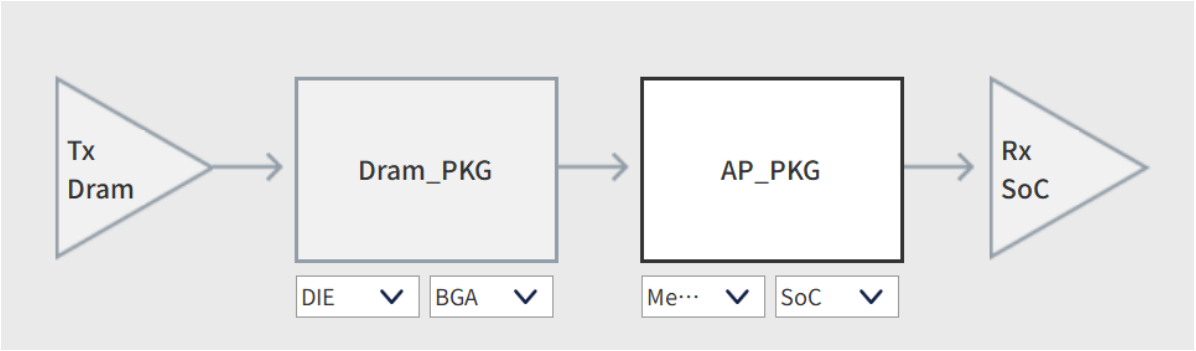

**Simulation 진행**



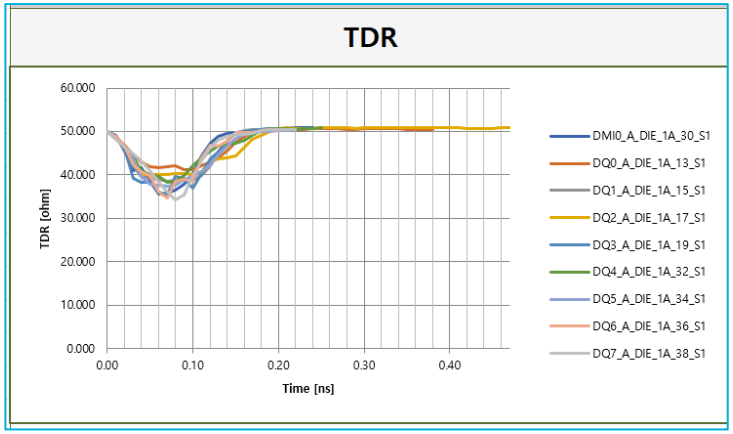

**Report 자동 생성**

## Transient Simulation : DDR5 simulation (Single-ended AMI)

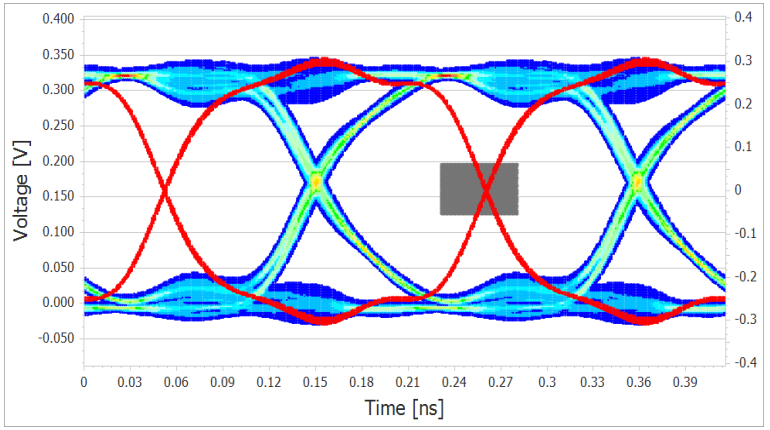
- **IBIS model + Dram pkg + SoC pkg 구성**
- **Write mode, 4800 Mbps (Byte0/1)**
- **Basic SI + Eye-diagram report**




**Channel configuration**



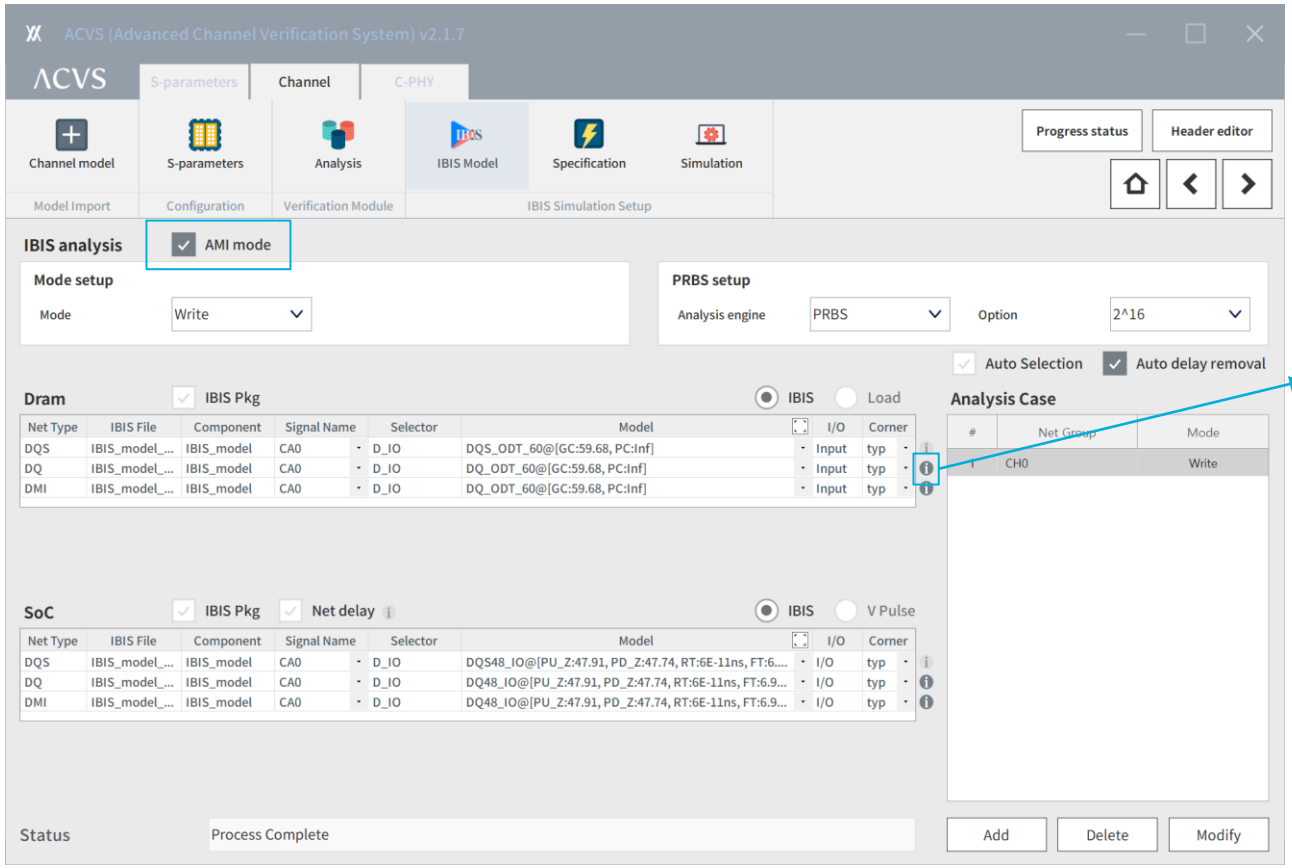

**Basic SI results**
**(TDR, TDT etc.)**

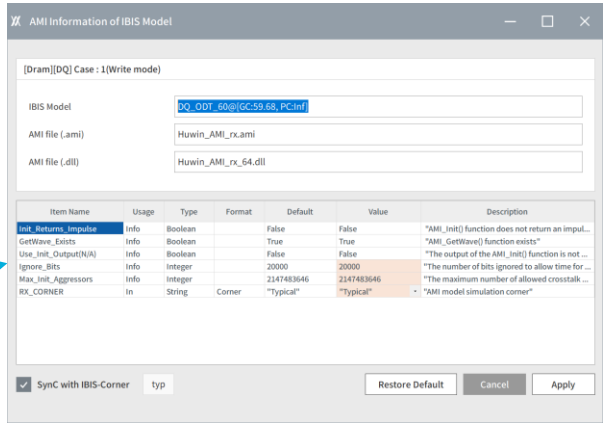



**Eye-diagram results**

## Transient Simulation : DDR5 simulation (Single-ended AMI)

- **IBIS 설정**
  - **AMI mode 설정: Signle-ended AMI 분석 진행**
  - **저장된 설정 값: Write mode, PRBS 2^16**

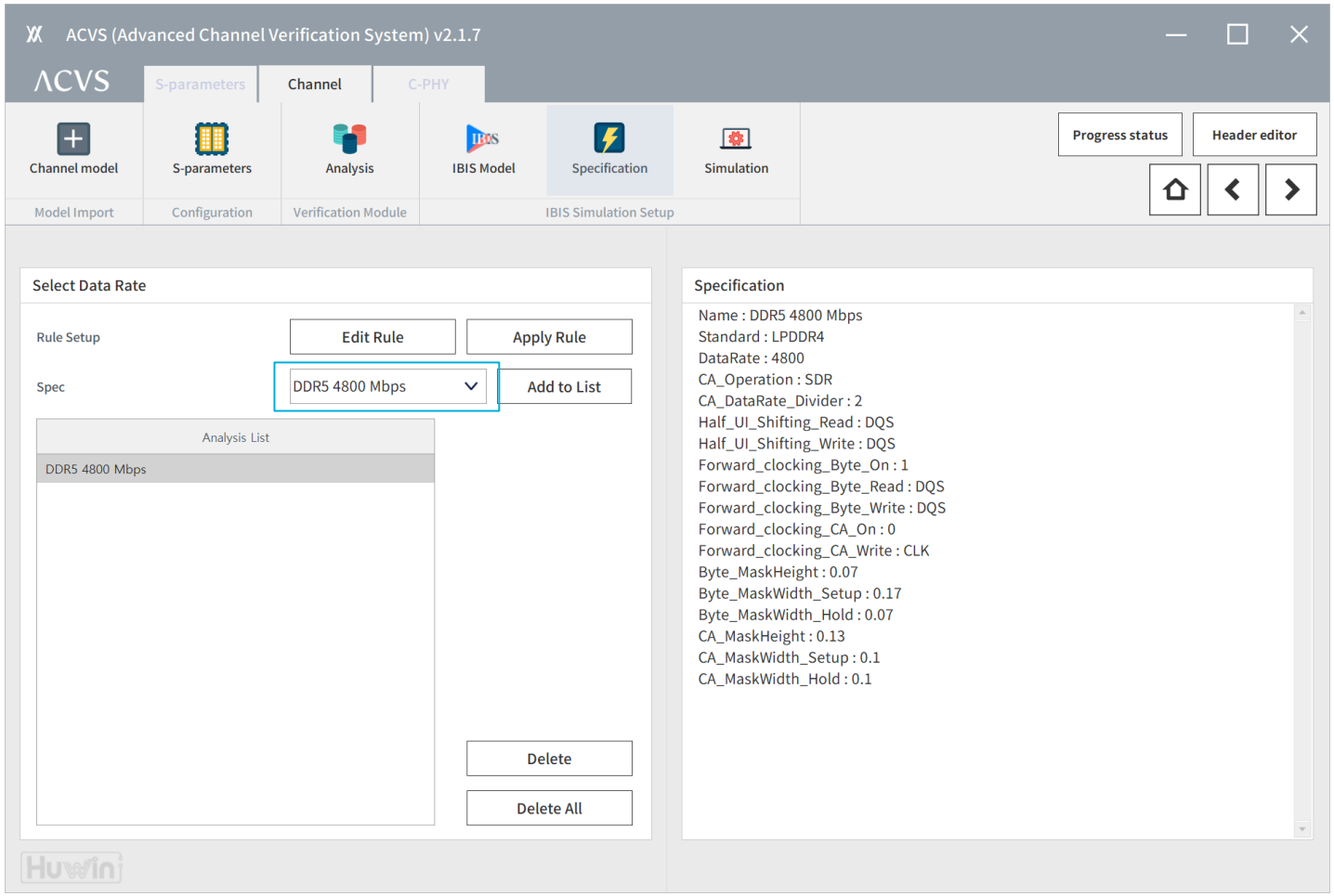



**AMI 설정 값 확인**

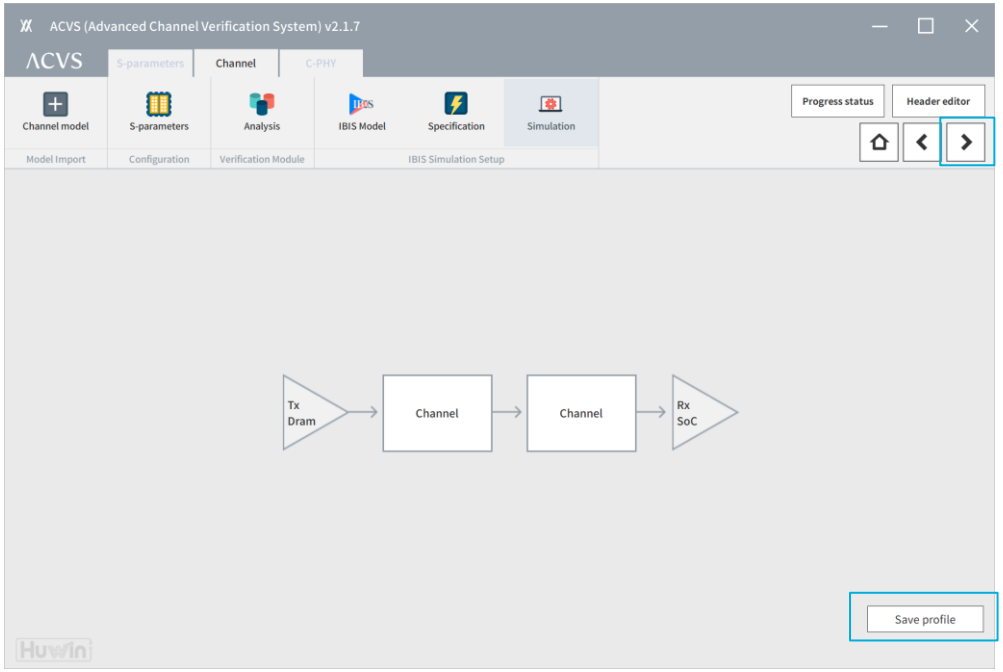
## Transient Simulation : DDR5 simulation (Single-ended AMI)

- **Data rate, Mask, 기타 설정**
- **저장된 설정 값: DDR5 4800 Mbps**

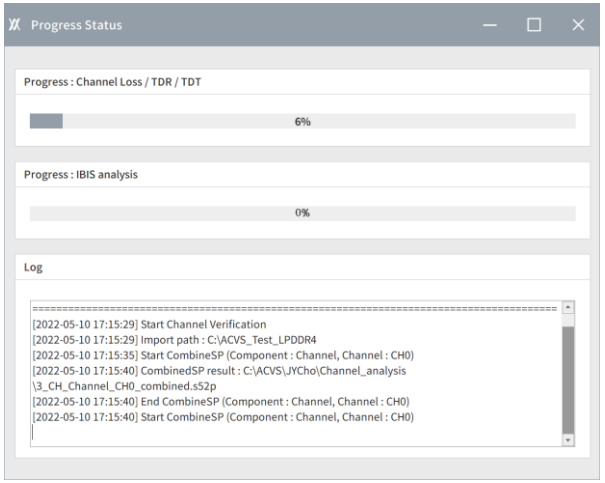


## Transient Simulation : DDR5 simulation (Single-ended AMI)

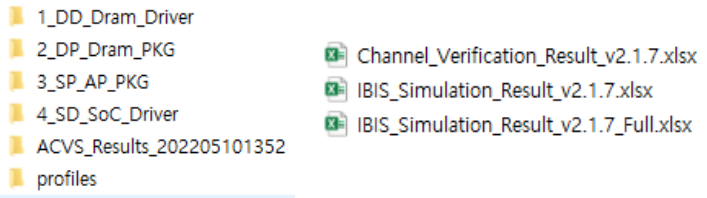
- **Run**




**Run**




**Simulation 진행**

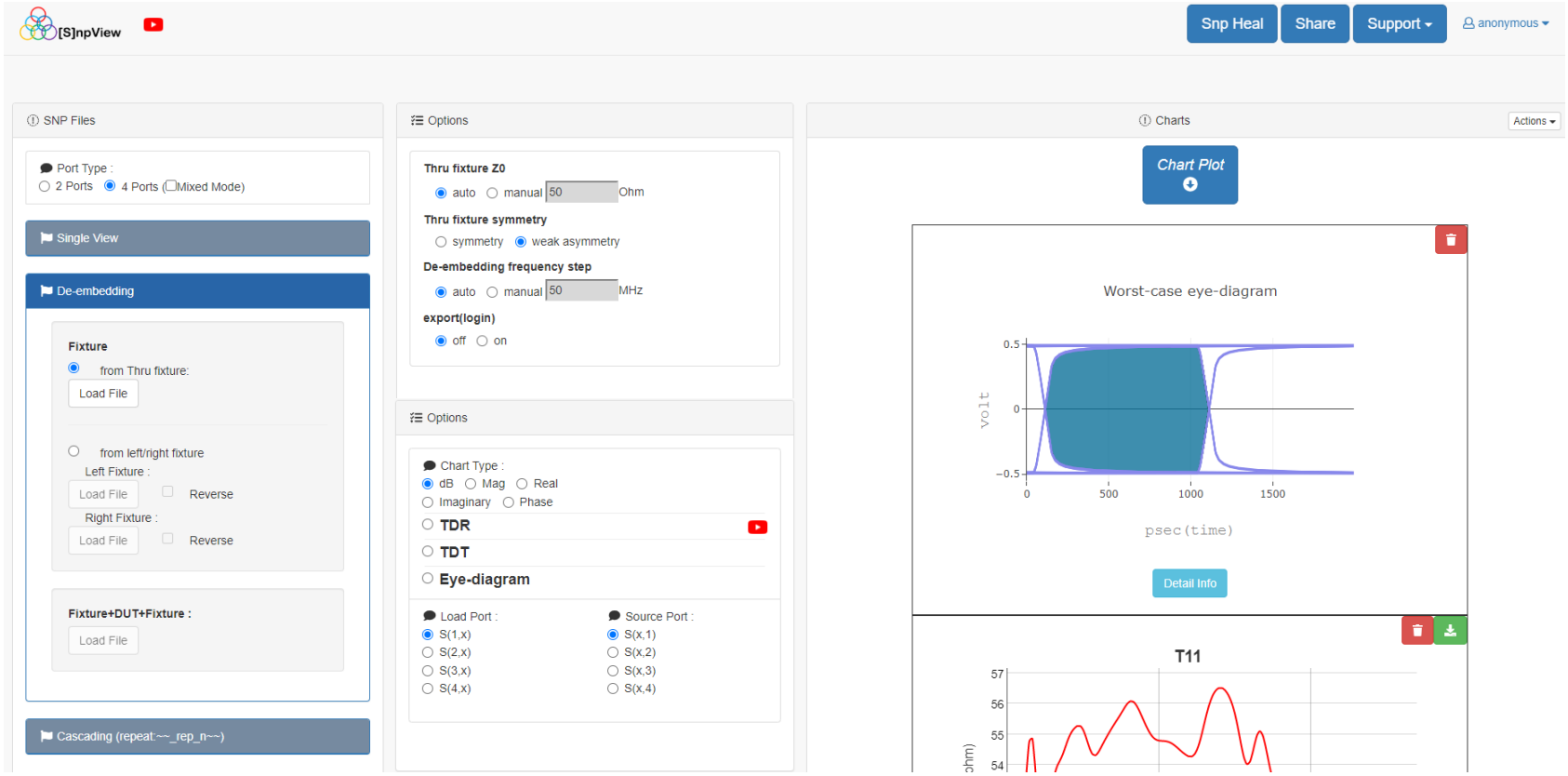



**Report 자동 생성**

## SnpView.com

Huwin Web-Based Free SnP view/heal/share, TDR, Eye Diagram, 2x THRU de-embedding

Plan to add IBIS, IBIS-AMI simulation



ANSYS Huwin

# Thank You