Tech. Seminar :

Next Gen High Performance Integrity :
Advanced Silicon/Package/PCB Interconnection Design

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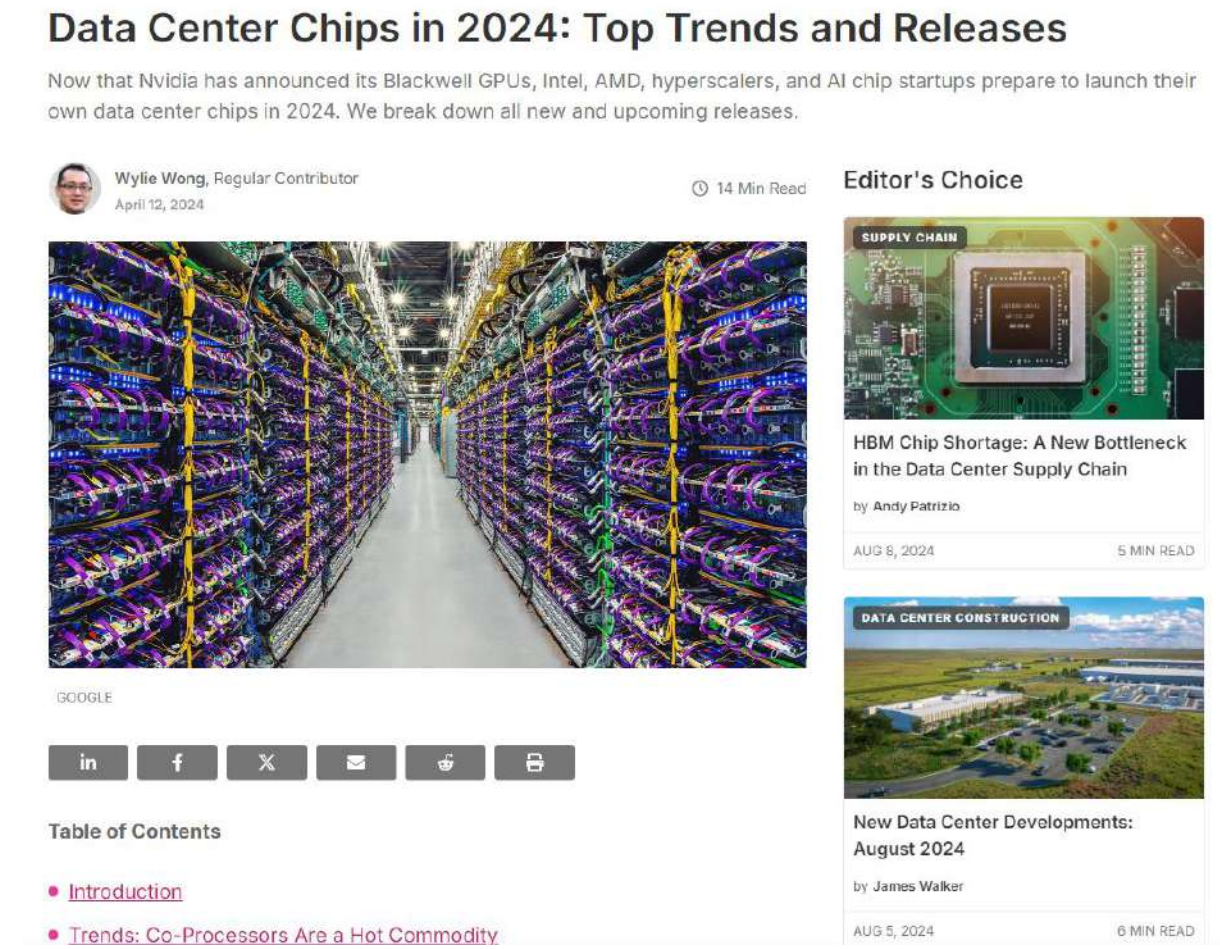

Data Center Chips in 2024: Top Trends and Releases

Now that Nvidia has announced its Blackwell GPUs, Intel, AMD, hyperscalers, and AI chip startups prepare to launch their own data center chips in 2024. We break down all new and upcoming releases.

Wylie Wong, Regular Contributor
April 12, 2024
14 Min Read

GOOGLE

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Editor's Choice

SUPPLY CHAIN

HBM Chip Shortage: A New Bottleneck in the Data Center Supply Chain

by Andy Patrizio

AUG 8, 2024 5 MIN READ

DATA CENTER CONSTRUCTION

New Data Center Developments: August 2024

by James Walker

AUG 5, 2024 6 MIN READ

2025년 데이터 센터
AI 어플리케이션 비중 => 30%

2024년 H100 => 200만개 판매
⇒ 2.5GW (LA 전력 소비량)

2025년 2배 증가(미국 전체 10%)

MS, Google, Amazon
⇒ 원자력 발전소

효율적인 반도체, 전력 공급

1V 1000A 프로세서 -> 1mΩ
load => 전력 경로 저항 100uΩ
이하 설계

https://www.datacenterknowledge.com/data-center-chips/data-center-chips-in-2024-top-trends-and-releases

1. Advanced Silicon/Package/PCB SPGTI Design 기술동향

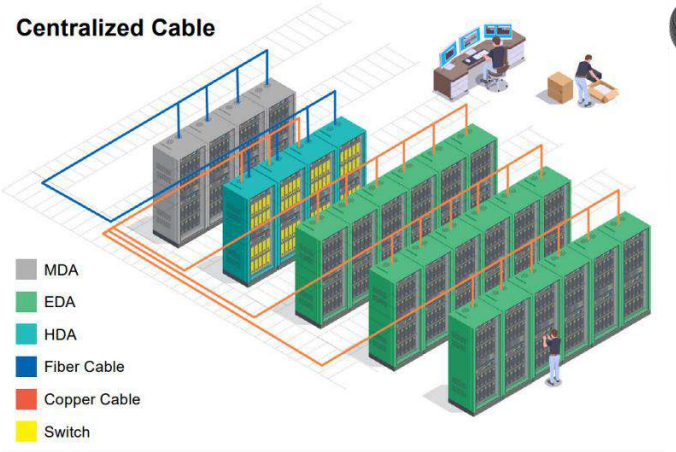
AI, Data center 확대에 따른 Issue(1)

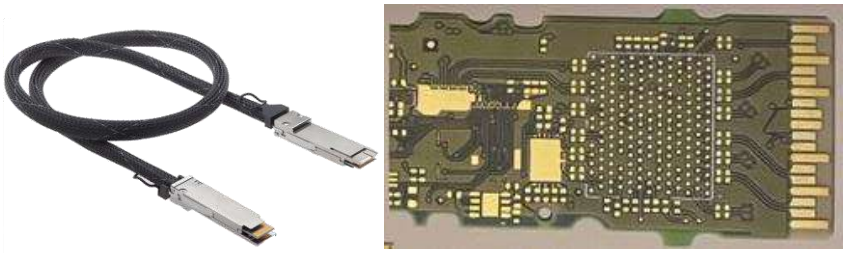
1) Cable 성능 (Server, Switch, Storage 간 고속 데이터 전송을 위한 cable)

- DAC (Direct Attach Copper) : Passive, Copper cable, 3m 미만, 같은 랙 내 서버와 스위치 간 짧은 연결
- AEC (Active Electrical Cable) : Active(신호 증폭 회로 포함), Copper cable, ~10m, 랙 간 연결
- AOC (Active Optical Cable) : 광섬유, electrical ↔ optical 변환 회로 포함, 수 백m, 데이터 센터 간 연결

+800Gbps → Copper 기반 cable의 loss ↑, EMI 영향 증가 → 광 기반 고속 인터페이스 적용 (PAM4, QSFP-DD 등)

- AOC Cable 내 DSP chipset 포함한 SI 해석 필요
- 100GHz 이상 측정 시 S-G pitch 200um 이하 권장 : 그러나 ball pitch 600~800um, Pad 는 1000um 수준
- Differential pair 설계 및 검증 중요, Via, Component pad의 size 및 anti pad size 영향 고려 필요





[AOC Cable 예]

[Data center 내 Cabling 예]

1. Advanced Silicon/Package/PCB SPGTI Design 기술동향

AI, Data center 확대에 따른 Issue(2)

2) PCB 제작 문제

- low loss substrate 선택 필요 Dk 3 수준, Df 0.002↓
- P사 Megatron series 비용 문제로 대부분 업체에서 대만의 E사 기판 사용 경향

[대만 E사 EM-S532K Datsheet]

Basic Laminate Property

Property	Item		Typical Value	Unit	Test Condition	IPC-TM-650
Thermal	Tg		N/A	℃	DSC	2.4.25
			180	℃	TMA	2.4.24
			215	℃	DMA	2.4.24.4
	CTE, X/Y-axis		12/13	ppm/℃	< Tg, TMA	2.4.24.5
	CTE, Z-axis		40~45	ppm/℃	< Tg, TMA	2.4.24
			185~205	ppm/℃	> Tg, TMA	
	Z-axis Expansion		1.8	%	50~260℃	2.4.24
	Td		420	℃	TGA (5% W.L)	2.4.24.6
	T288		>60	Min	Clad	2.4.24.1
			>60	Min	Etched	
	Thermal Conductivity		0.46	W/m.K	-	ASTM D5470
Electrical	Dk (R/C: 55/70%)	1 GHz	3.11/2.93	-	C-24/23/50	2.5.5.9
		10 GHz	3.00/2.84			Cavity Resonator
			3.00/2.84			SPC method
	Df (R/C: 55/70%)	1 GHz	0.0014/0.0012	-	C-24/23/50	2.5.5.9
		10 GHz	0.0019/0.0017			Cavity Resonator
			0.0015/0.0013			SPC method
Physical	Water Absorption		0.07	%	E-1/105+D-24/23	2.6.2.1
	Peel Strength (LP)	H oz	0.6	kN/m	As Received	2.4.8
	Flame Resistance		V-0	-	C-48/23/50	UL-94

Above typical values are tested under specified constructions and not intended for specification.

[일본 P사 Megatron6, 7 Datsheet]

Property			Units	Test Method	Condition	Typical Value
THERMAL	Glass Transition Temp (Tg)		C	DSC	As received	185
				DMA	As received	210
	Thermal Decomposition Temp (Td)		C	TGA	As received	410
	Time to Delam (T288)	Without Cu	Min	IPC TM-650 2.4.24.1	As received	> 120
		With Cu	Min	IPC TM-650 2.4.24.1	As received	> 120
	CTE : α1	X - axis	ppm / C	IPC TM-650 2.4.24	< Tg	14 - 16
		Y - axis	ppm / C	IPC TM-650 2.4.24	< Tg	14 - 16
		Z - axis	ppm / C	IPC TM-650 2.4.24	< Tg	45
	CTE : α2	Z - axis	ppm / C	IPC TM-650 2.4.24	> Tg	260
ELECTRICAL	Volume Resistivity		MΩ - cm	IPC TM-650 2.5.17.1	C-96/35/90	1 x 10^9
	Surface Resistivity		MΩ	IPC TM-650 2.5.17.1	C-96/35/90	1 x 10^8
	Dielectric Constant (Dk)	@ 1GHz	-	IPC TM-650 2.5.5.9	C-24/23/50	3.40
		@ 12GHz	-	*Note 1	C-24/23/50	3.35
	Dissipation Factor (Df)	@ 1GHz	-	IPC TM-650 2.5.5.9	C-24/23/50	0.002
		@ 12GHz	-	*Note 1	C-24/23/50	0.004
PHYSICAL	Water Absorption		%	IPC TM-650 2.6.2.1	D-24/23	0.14
	Peel Strength	1oz (H-VLP)	kN / m	IPC TM-650 2.4.8	As Received	0.8
	Flammability		-	UL	C-48/23/50	94V-0

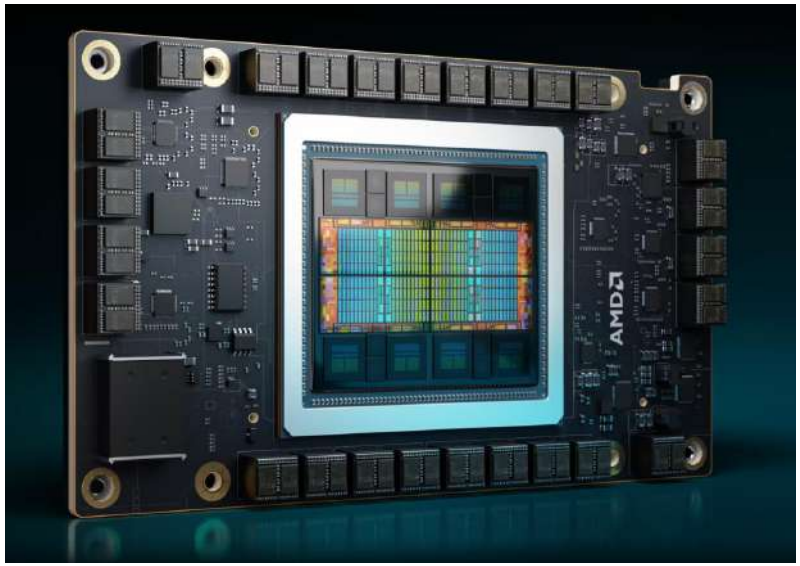
Property			Units	Test Method	Condition	Typical Value R-5785(GE) E glass	Typical Value R-5785(GN) Low-Dk glass
THERMAL	Glass Transition Temp (Tg)		C	DSC	As received	200	200
				TMA	As received	190	190
				DMA	As received	210	210
	Thermal Decomposition Temp (Td)		C	TGA	As received	400	400
	Time to Delam (T288)	Without Cu	Min	IPC TM-650 2.4.24.1	As received	> 120	> 120
		With Cu	Min	IPC TM-650 2.4.24.1	As received	> 120	> 120
	CTE : α1	X – axis	ppm / C	IPC TM-650 2.4.24	< Tg	14 - 16	14 - 16
		Y – axis	ppm / C	IPC TM-650 2.4.24	< Tg	14 - 16	14 - 16
		Z – axis	ppm / C	IPC TM-650 2.4.24	< Tg	42	42
	CTE : α2	Z – axis	ppm / C	IPC TM-650 2.4.24	> Tg	280	280
ELECTRICAL	Volume Resistivity		MΩ - cm	IPC TM-650 2.5.17.1	C-96/35/90	1 x 10^9	1 x 10^9
	Surface Resistivity		MΩ	IPC TM-650 2.5.17.1	C-96/35/90	1 x 10^8	1 x 10^8
	Dielectric Constant (Dk)	@ 1GHz	-	IPC TM-650 2.5.5.9	C-24/23/50	3.63	3.37
		@ 13, 14GHz	-	*Note 1	C-24/23/50	3.60 @13GHz	3.31 @14GHz
	Dissipation Factor (Df)	@ 1GHz	-	IPC TM-650 2.5.5.9	C-24/23/50	0.002	0.001
		@ 13, 14GHz	-	*Note 1	C-24/23/50	0.0034 @13GHz	0.0023 @14GHz
PHYSICAL	Water Absorption		%	IPC TM-650 2.6.2.1	D-24/23	0.06	0.06
	Peel Strength	1oz (H-VLP2)	kN / m	IPC TM-650 2.4.8	As received	0.8	0.8
	Flammability		-	UL	C-48/23/50	94V-0	94V-0

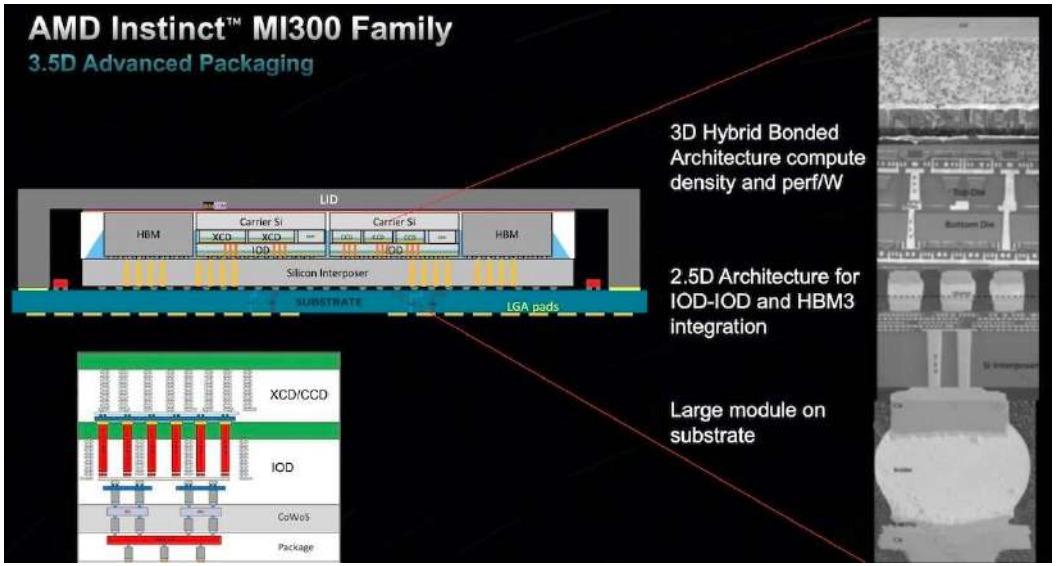
1. Advanced Silicon/Package/PCB SPGTI Design 기술동향

Packaging Issue : Package 불량으로 인한 손실비용

- HBM 등 packaging 부품 증가로 기판 크기 증가 → Warpage 문제 발생
- package 내부에 단위 소자 불량 시 손실 비용 막대해 PCB level에서 부품 실장 희망 → SI 해석 중요
- 미국 선진사의 경우 System level simulation을 통해 설계 최적화 후 제품 제작

구분	설명
2D packaging	단일 기판 위에 chip 평면 배치
2.5D packaging	Silicon interposer 위에 여러 chiplet 배치
3D packaging	TSV(Through-Silicon Via) 기술로 Die들을 수직 적층
3.5D packaging	2.5D + 3D Hybrid. 일부는 수직 적층, 일부는 평면 상 연결

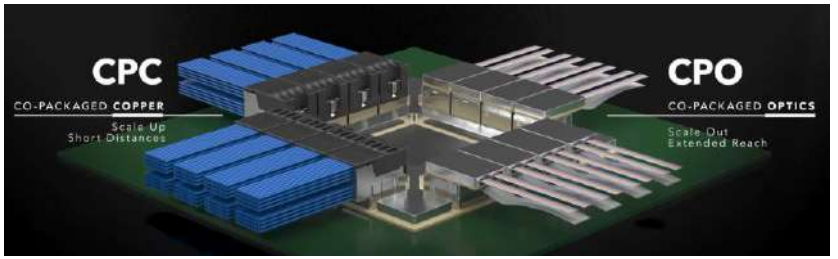


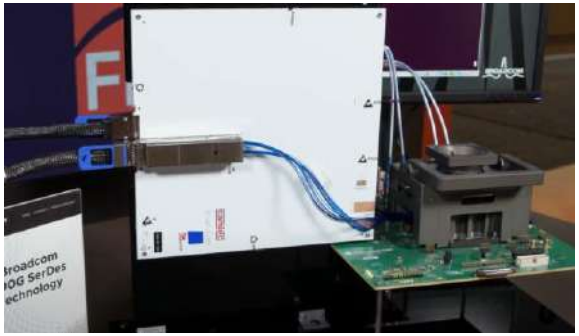


1. Advanced Silicon/Package/PCB SPGTI Design 기술동향

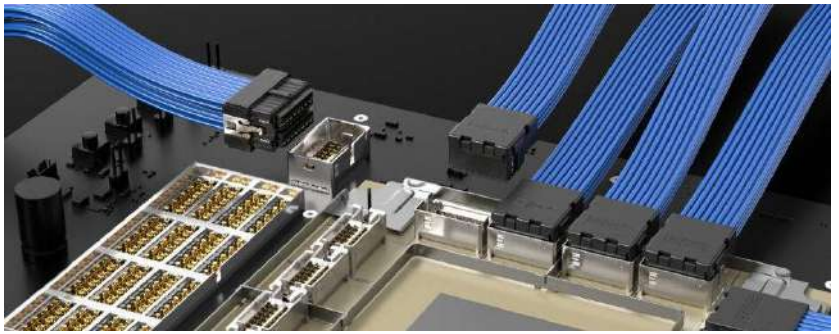
Interconnection issue

- Co-Packaged copper channel(CPC) : PCB Trace 최소화하여, 패키지에서 직접 케이블을 연결하는 방식
- A사 제품 출시해 N사 공급, 타사 시제품 출시 중
- ~110GHz 대역 low loss 특성 요구
- Twinax cable + GSSG 구조 pin 배열 사용 (SI 해석 필요)
- Twinax cable skew 제어도 중요 → 제조 정밀도 중요

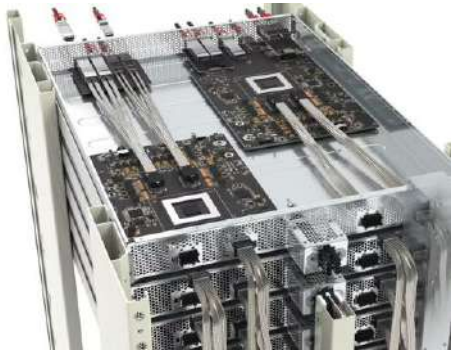




[S사 200 Gbps Co-packaged Copper channel 시연 예]



[S사 CPC 구조도]

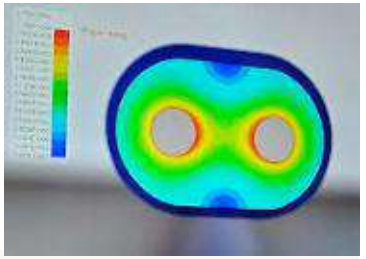


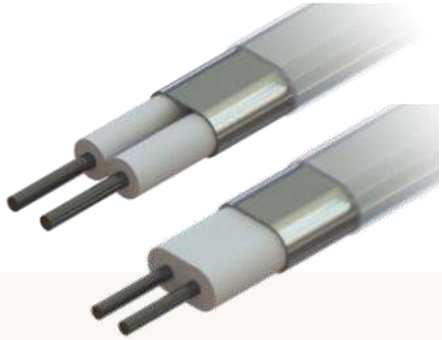
[M사 224G architecture, near ASIC cable, board-to-board connector, backplane cable 예시]

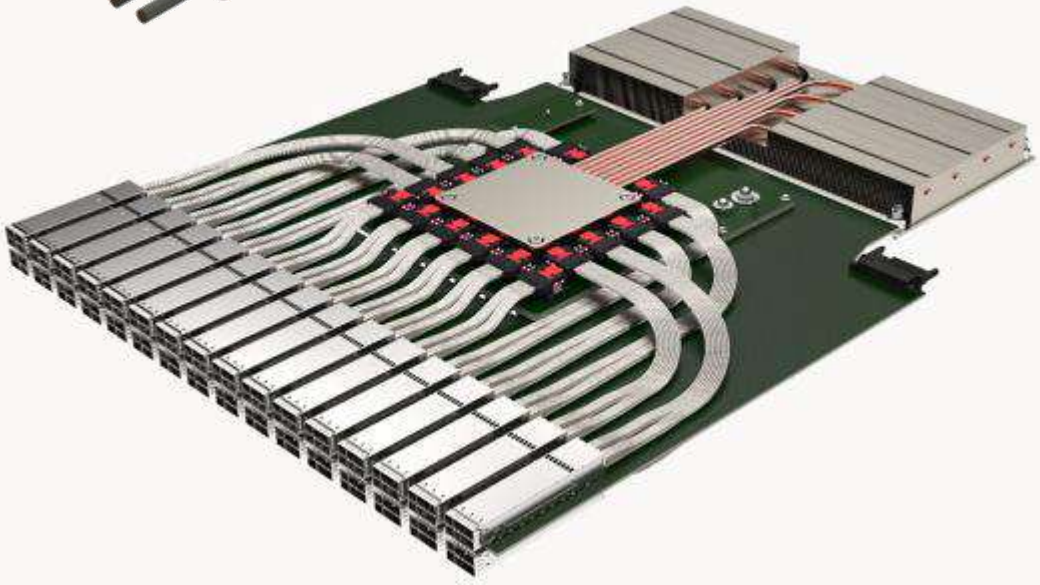
1. Advanced Silicon/Package/PCB SPGTI Design 기술동향

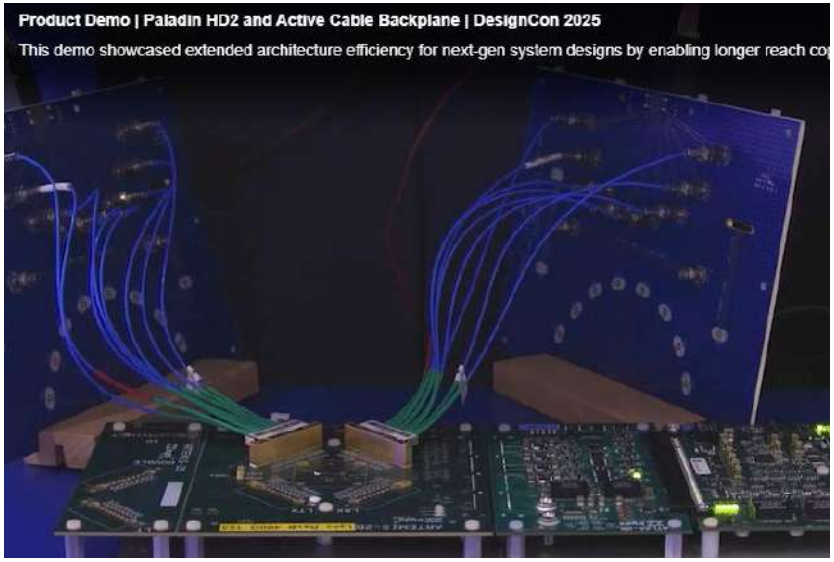
Interconnection issue

- Mear Package Connector
- 0.8mm connector (145 GHz)
- 1mm connector (110 GHz)









Paladin HD2 and Active Cable Backplane : 224Gbps

1. Advanced Silicon/Package/PCB SPGTI Design 기술동향

Interconnection issue : 224G Long-Reach SerDes for UALink

UALink Overview :

- UALink: Ultra Accelerator Link
- Industry consortium: AMD, Intel, Broadcom, Microsoft, Meta, Cisco, HPE, Google 등
- Purpose: 고속 AI 가속기 간 인터커넥트 표준화
- 경쟁 기술: NVLink, CCIX, CXL, PCIe
- 224G SerDes는 차세대 AI 시스템 연결의 핵심
- UALink의 고속/저지연/확장성 구현을 위한 필수 기술
- 전력/신호무결성/모듈화 기술과 함께 발전 중

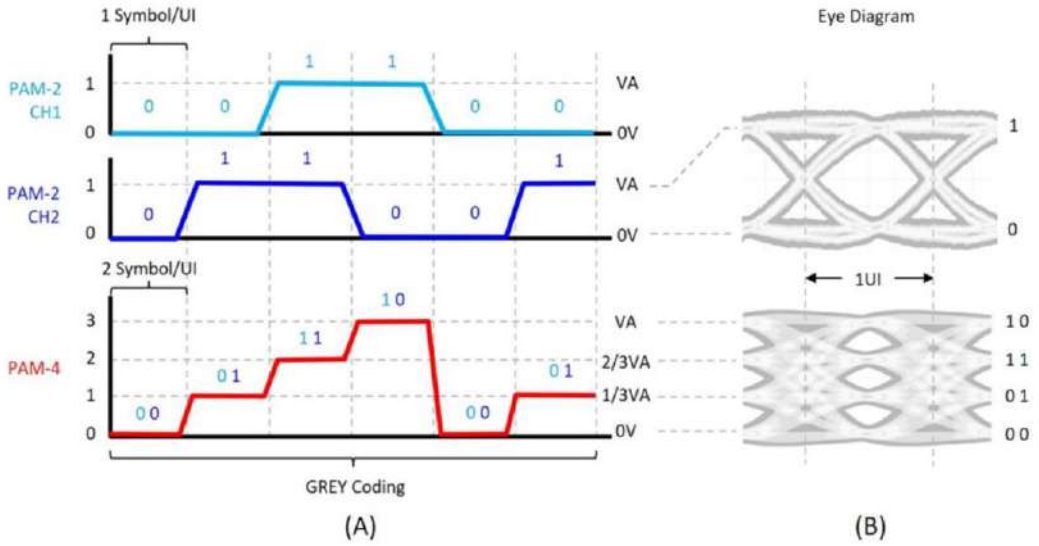
기술 구성 요소 :

- Modulation: PAM4 (2bit/symbol)
- Equalization: FFE, DFE, ML-based
- FEC: BER 1e-13 이하 보장
- Channel 설계: Trace, Via, Connector, Packaging
- Power Efficiency: 고속 인터페이스의 과제

1. Advanced Silicon/Package/PCB SPGTI Design 기술동향

Interconnection issue : PAM4

- 25Gbps에서 50Gbps 링크 속도로 전환하면서 신호 형식은 NRZ에서 PAM4로 변환됨
- PAM2는 2개의 전압 레벨만 사용하는 NRZ(Non-Return-to_Zero) 방식으로, 각 심볼이 1비트를 전달함
- PAM4는 4개의 전압 레벨을 사용하여 하나의 심볼로 2비트를 전달하지만, SNR이 낮아지고 오류율이 증가함



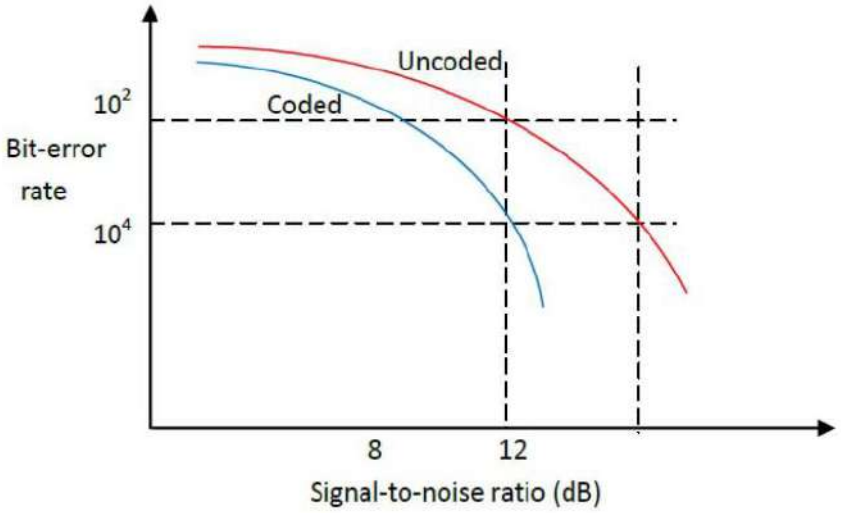
[PAM-2 / PAM-4 encoding 및 eye diagram 비교]

	PAM2 (NRZ)	PAM4
신호 레벨 수	2 (0,1)	4 (00,01,10,11)
비트당 심볼 수	1 bit /symbol	2 bits/symbol
보드율 대비 데이터율	동일	기존 대비 2배
적용 분야	PCIe Gen 3~5	100G

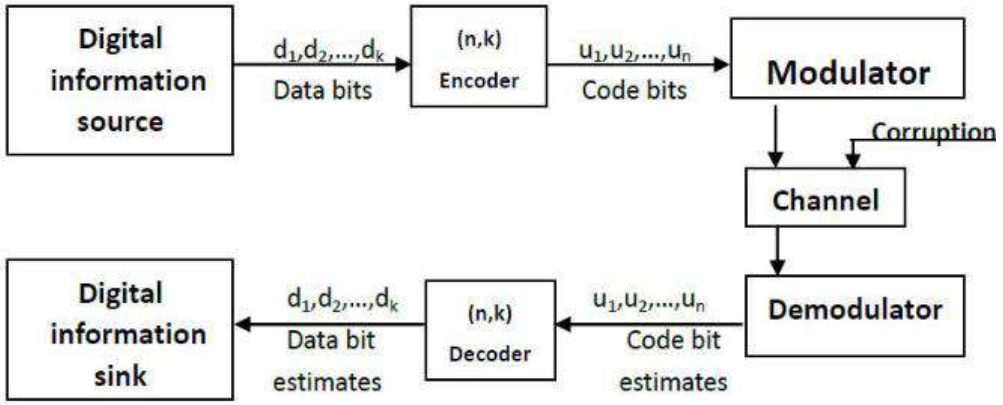
1. Advanced Silicon/Package/PCB SPGTI Design 기술동향

Interconnection issue : FEC

- FEC는 송신 데이터에 추가 정보를 더하여 전송하는 데이터 전송 시스템으로, 수신 측에서 재전송 없이 오류 감지 및 수정할 수 있게 해주는 기술을 의미함
- 시스템의 오류율은 SNR(Signal to noise ratio)이 감소함에 따라 점차 증가하며, FEC 코딩이 적용되면 더 낮은 비트 오류율은 가지게 됨
- 송신측에서 원본데이터에 체크 비트를 추가하여 인코딩된 코드워드를 전송하면, 수신측에서는 수신된 코드워드를 디코딩하여 오류 복구



[SNR of systems with and without FEC]



[How FEC Works]

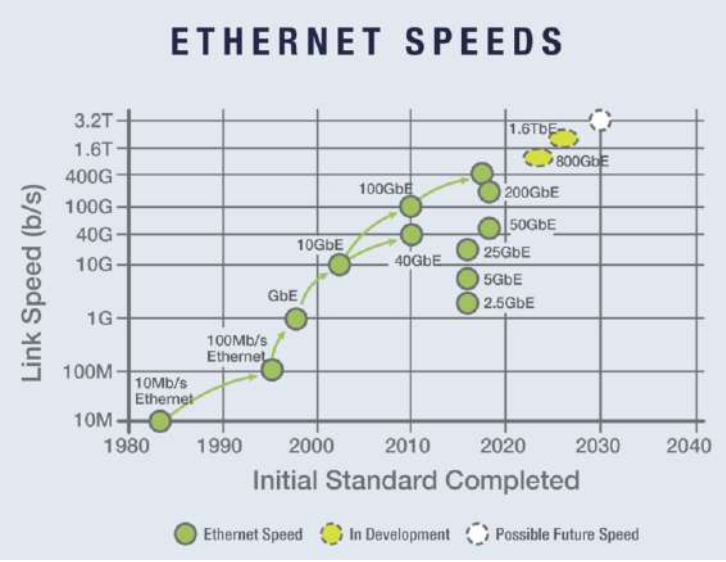
1. Advanced Silicon/Package/PCB SPGTI Design 기술동향

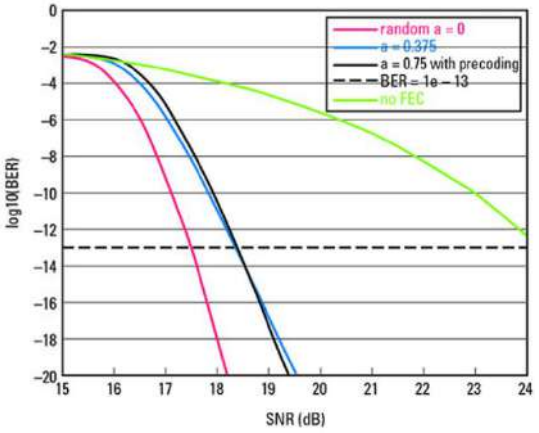
Interconnection issue : FEC for 200+ Gbps Ethernet

- 5G/6G 네트워크 및 AI/ML application의 성장으로, 큰 bandwidth, high speed communication의 요구로 serial lin data 속도는 지속적으로 증가하고 있음

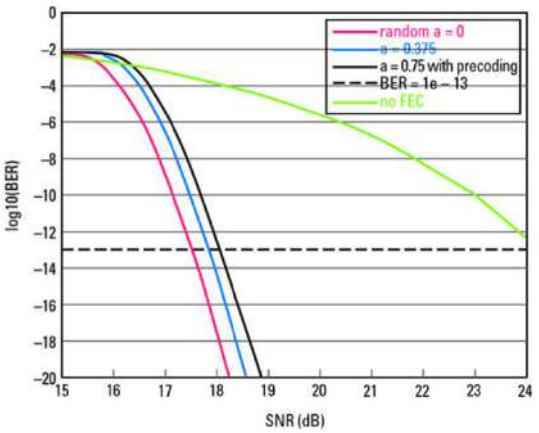
- IEEE 802.3은 200 Gbps, 400 Gbps, 800 Gbps 및 1.6 Tbps 이더넷을 위한 task force를 구성하였고, 목표는 lane 당 200Gbps 전송 속도 확보임

- 200 Gbps 이상 이더넷 시스템에서는 낮은 SNR 환경에서 안정적인 전송을 위해 FEC(Forward Error Rate)가 필수적





2-way 코드워드 인터리빙



4-way 코드워드 인터리빙

[Post-FEC BER 성능 비교]

Ref) https://iebmedia.com/technology/industrial-ethernet/ethernet-celebrates-50-years-with-2023-roadmap-and-demo

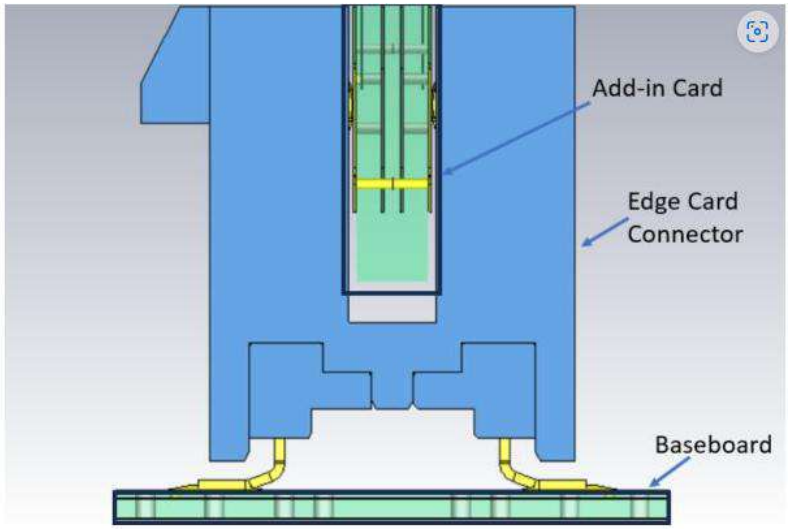
1. Advanced Silicon/Package/PCB SPGTI Design 기술동향

PCIe Gen7 설계 주요 변화

- PCIe Gen6 → PCIe Gen7 (PAM4, 128Gbps)

Pad to Pad Channel loss budget : 32dB @16GHz → 36dB @32GHz

- 대역폭 증가로 인해 spec은 엄격해지고 Add in card(AIC) 부터 Baseboard components 까지 설계 개선이 필요함
- Signal Integrity, Ground-mode resonance, Balance signal performance and mechanical reliability



[Figure 1 The architecture of the PCIe CEM connector]

- PCIe CEM Connector 성능 평가 범위

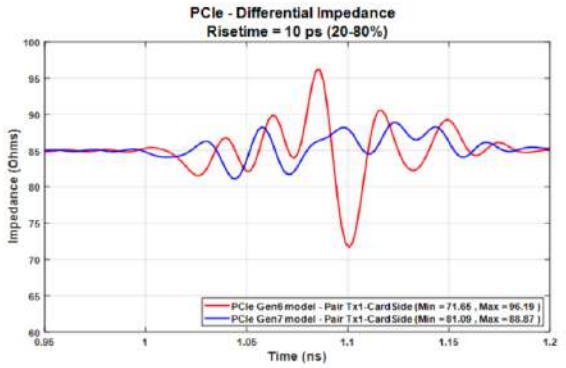
AIC trace 50mils(1.27mm)
+
AIC Connector 결합 부 pad
+
Connector 자체
+
Baseboard의 Connector 결합 부 pad
+
Baseboard trace 50mils(1.27mm)

1. Advanced Silicon/Package/PCB SPGTI Design 기술동향

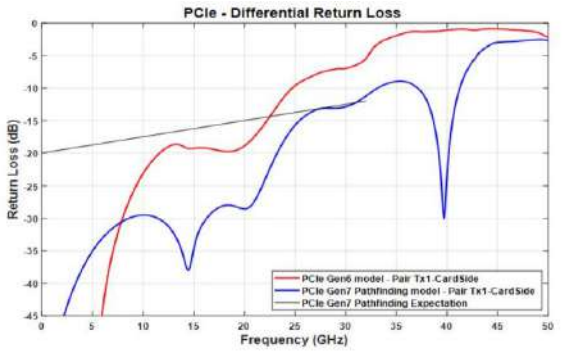
PCIe Gen6 and Gen7 connectors의 시뮬레이션 결과 비교

- CEM(Card Electromechanical) Connector 의 임피던스 guideline : 85ohm ± 10% (76.5~93.5 ohm)

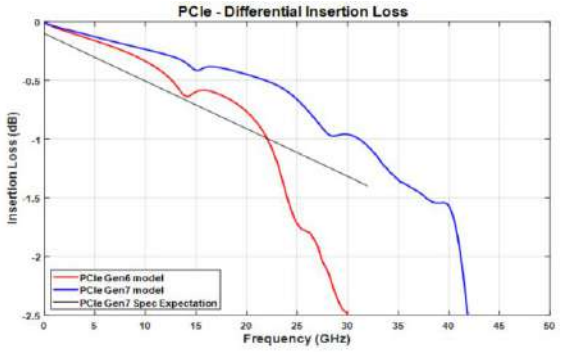
– Gen6 connector : rise time 10ps 조건에서의 TDR 임피던스 72 ~ 96 ohm 수준을 나타냄, Gen7 기준 미달
– Gen7 connector : 81 ~ 89 ohm 을 보이며, Gen6 connector에 비해 IL, RL 특성 우수
→ 데이터 속도 증가함에 따라 정교한 임피던스 제어 필요성 증가



[Figure 2 Impedance comparison of Amphenol's PCIe Gen6 connector vs. Gen7 connector]

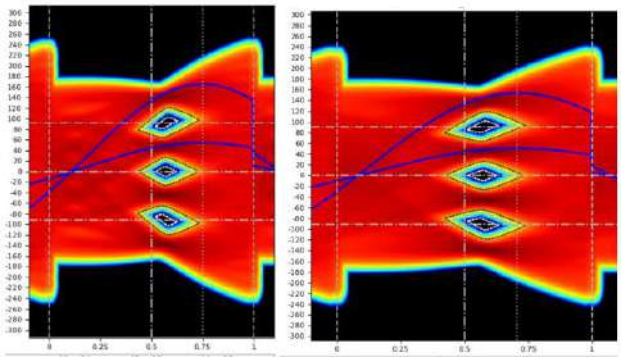


[Figure 3 Return loss comparison of Amphenol's PCIe Gen6 connector vs. connector]



[Figure 4 Insertion loss comparison of Amphenol's PCIe Gen6 connector vs. connector]

	Gen6			Gen7		
BER	1e-04	1e-06	1e-12	1e-04	1e-06	1e-12
eye height top	53.49mV	**41.54mV**	16.69mV	54.37mV	**43.17mV**	19.67mV
eye height mid	52.85mV	41.88mV	19.00mV	52.98mV	42.27mV	19.79mV
eye width top	0.235UI	**0.180UI**	0.070UI	0.270UI	**0.205UI**	0.095UI
eye width mid	0.292UI	0.222UI	0.101UI	0.306UI	0.237UI	0.113UI
pkeh off	0.070UI	0.070UI	0.070UI	0.075UI	0.075UI	0.075UI
vref top	92.2mV	92.4mV	92.2mV	91.3mV	91.1mV	91.5mV



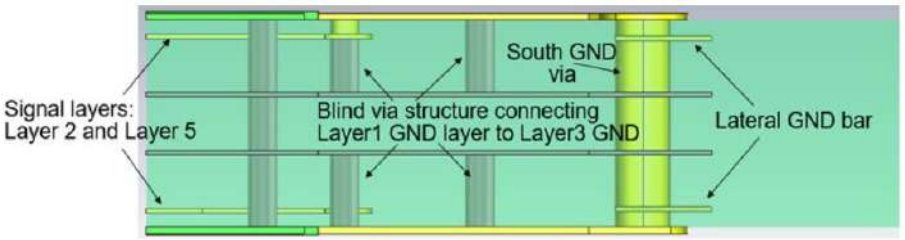
[Figure 5 Seasim result comparing Gen6(left) and Gen7(right)]

1. Advanced Silicon/Package/PCB SPGTI Design 기술동향

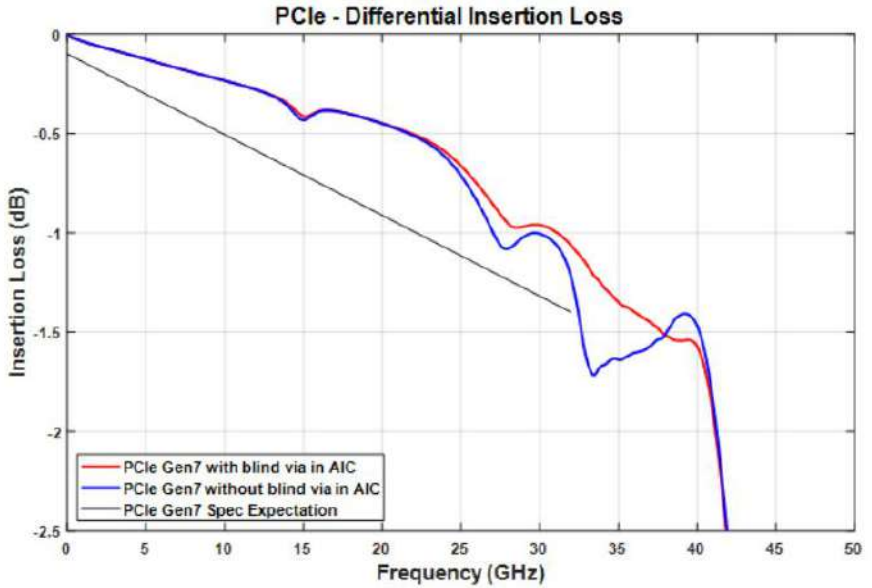
PCIe Gen7 Add in Card Design

- Gen7 AIC 설계의 주요 변화

(1) Gen6의 핵심 구성은 Gen7에서도 유지(GND plane for shield, fingertip south via, lateral ground bar 등)
(2) Blind via를 이용한 top layer의 GND와 가장 안쪽 layer GND와 연결 → 25GHz 이후 IL 성능 개선



[Figure 6. AIC design of PCIe Gen7 CEM connector]



[Figure 7. Insertion loss performance with and without blind via in AIC]

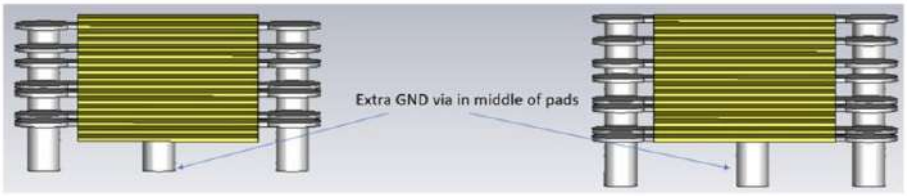
1. Advanced Silicon/Package/PCB SPGTI Design 기술동향

PCIe Gen7 Baseboard Design

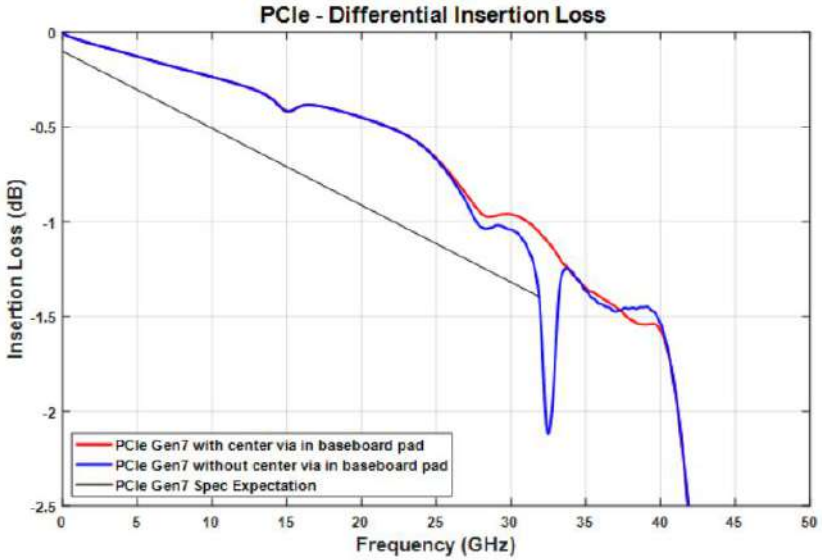
- Gen7 Baseboard/Motherboard 설계의 주요 변화

(1) Gen7은 Gen6 footprint 유지하면서 고주파에 성능 향상 필요
(2) GND pad 양 끝단에만 있는 via 외에 pad 중앙에도 GND via를 추가
→ Return path의 Inductance 감소, Ground mode Resonance 감소 효과
→ 25GHz 이상 대역에서 IL 성능 개선

* Loss, TDR 검증위해 정확한 Field solver 중요 => ANSYS HFSS



[Figure 8. Addition of extra GND via in baseboard]



[Figure 9. Insertion loss performance with and without center GND via in baseboard]

목차

2. 시뮬레이션 통한 SPGTI 설계 :

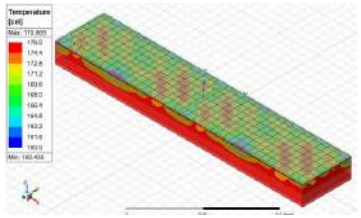
Next Generation Advanced Ch. Trends :

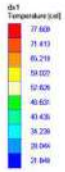
Signal :

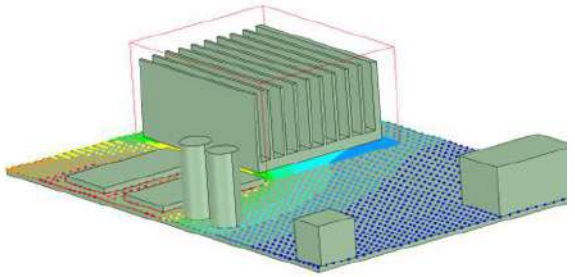
Power :

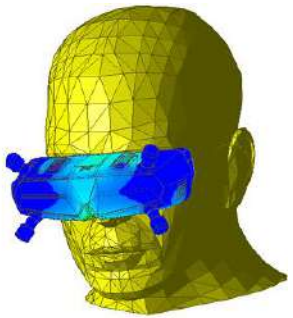
Ground :

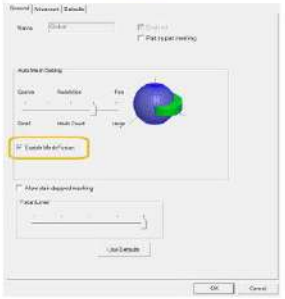
Thermal :







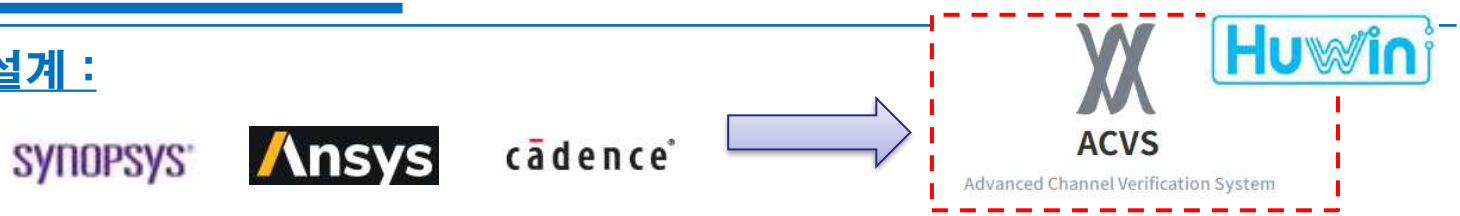




ANSYS Electronics 개발 방향 :

- Icepak : workflow, Meshing, Enhanced Physics 개선
- Icepak : System Level Thermal Integrity Solutions and Workflow => Chip to system thermal (RHSC-ET, Mechanical FEM, HFSS , ROM/CTM workflow)
- Icepak-Slwave : Package on PCB and PCB Assemblies => PCB/PKG Thermal
- Mechanical in AEDT : Thermal & Structural (Enabling easy-to-use conduction-only thermal and linear steady-state structural analysis)

2. 시뮬레이션 통한 SPGTI 설계 :



"Energy Efficient Computing Systems: Architectures, Abstractions, and Modeling(시뮬레이션) to Techniques(검증,기법,방법) and Standards"

1.Architectural Trends: The evolution from single-core to multi-core and domain-specific architectures, driven by the end of Dennard scaling and the limits of Moore's Law.

2.Energy Efficiency Techniques: dynamic voltage and frequency scaling (DVFS), power gating, and thermal management across CPUs, GPUs, memory, and AI accelerators.

3.Modeling and Simulation: Reviews tools and frameworks used for power, performance, and thermal modeling, essential for optimizing future computing systems.

4.Verification and Standards: importance of standards like IEEE 1801 (Unified Power Format) for specifying power intent in design, and the need for holistic approaches encompassing hardware and software. the complexity and multi-disciplinary nature of designing energy-efficient systems, stressing the importance of cross-layer optimizations and industry collaboration in addressing future challenges in computing systems' energy efficiency.

* Source : Energy Efficient Computing Systems: Architectures, Abstractions and Modeling to Techniques and Standards

2. 시뮬레이션 통한 SPGTI 설계 :

Technology Scale 에 따른 R(f),L(f),C(f),G(f) ?

Next Generation Advanced Ch. Trends :

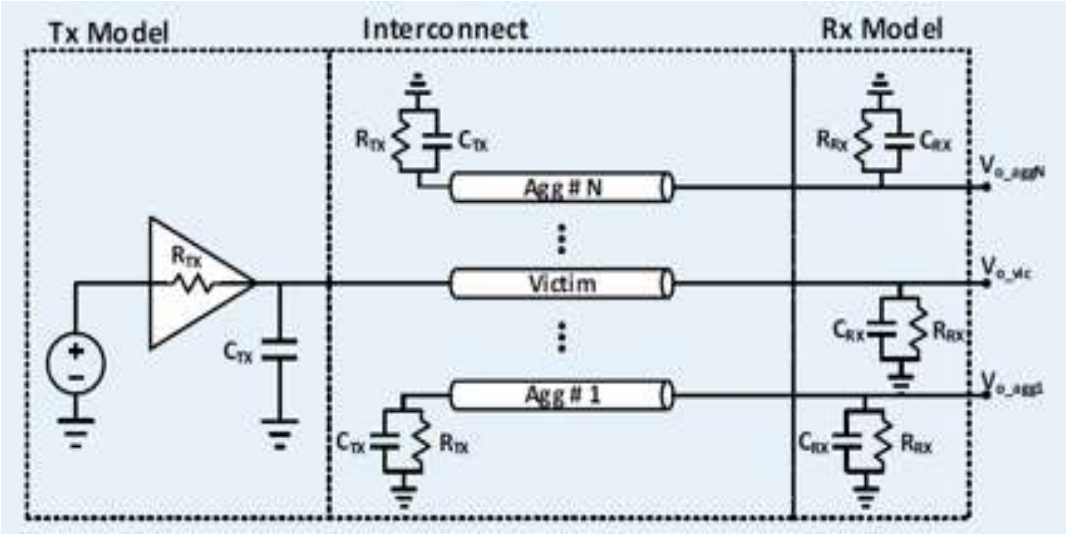
< 2um width, space

Signal : VTF loss, XTALKS

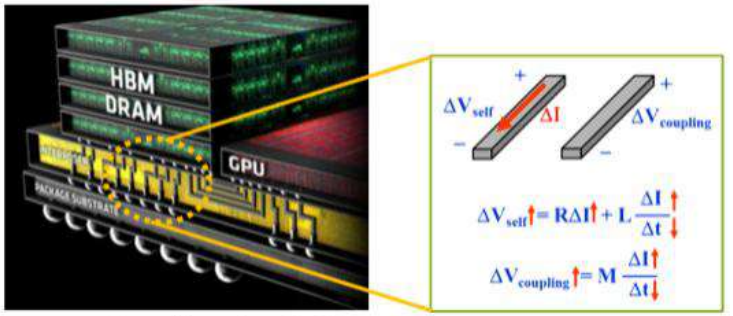
Power : Effective Imp.

Ground : Common GND Interference

Thermal : Reliability



$$Z_0 = \frac{V_0^+}{I_0^+} = \frac{-(R+jwL)}{-\gamma} = \frac{(R+jwL)}{\sqrt{(R+jwL)(G+jwC)}} = \sqrt{\frac{(R+jwL)}{(G+jwC)}}$$

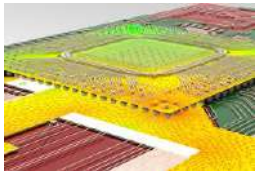


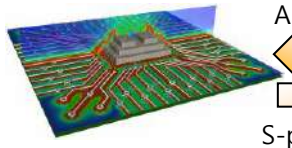
- Smaller size & Narrower space

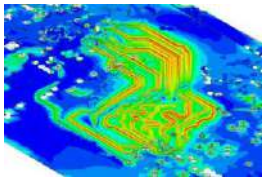
2. 시뮬레이션 통한 SPGTI 설계 : ACVS

High-Precision, High-Speed, and Reliable SI/PI Analysis

EM simulation







➢ ANSYS SIwave, HFSS, etc.

Automation

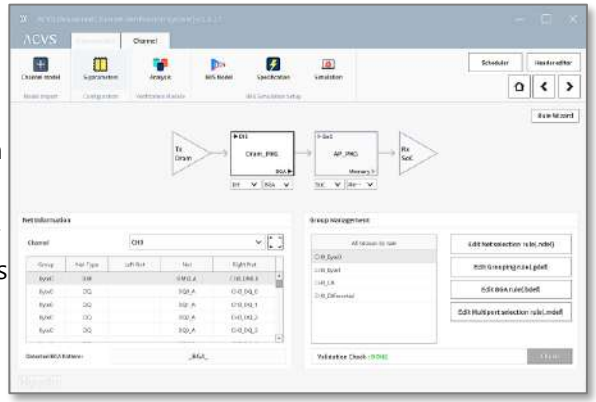
S-parameters

ACVS: Channel simulation/reporting

SAMSUNG SK hynix LG KAIST

GAONCHIPS Qualitas Telechips

StepSystem CoCoLink meritech SEMI FIVE

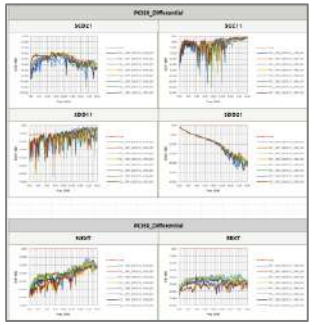


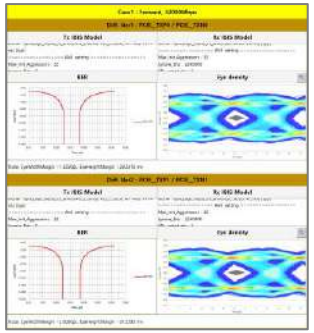
➢ Automation of system simulation with SimNX® engine.
➢ Reporting: charts and measurement.
➢ Applications: DDR4/5~, HBM3+, PCIe, UCIe, C-PHY, etc.

S-parameters with 1000+ ports, 100GB+ file size

Reporting

Report

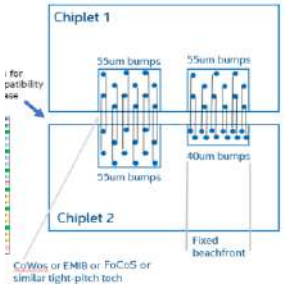




➢ Customized report

Expanding **automation coverage** for recent applications

2. 시뮬레이션 통한 SPGTI 설계 :



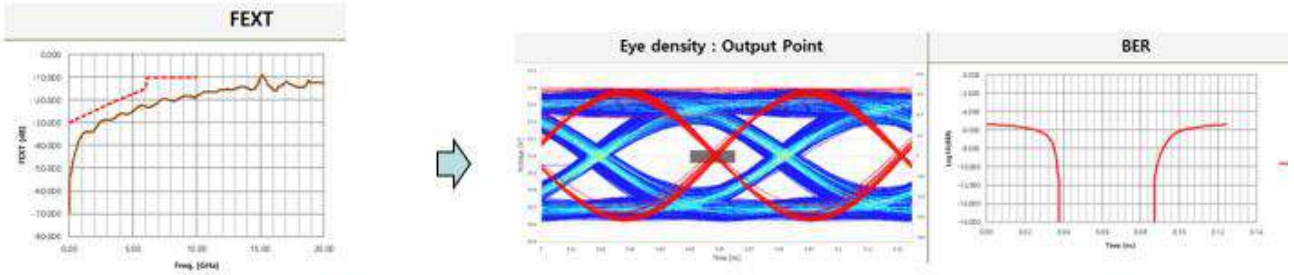
Tech. Issues and Why ACVS ?

Tech. Issues :

- Adv. Pkg/PCB/Interconnects
- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDR/TDT
- IL
- Skin Effects
- PAM4
- Full Ch. Auto verification

ACVS
Advanced Channel Verification System

➢ Huwin ACVS Basic SI (FEXT) and Eye/BER report results correlation example for Jitter analysis



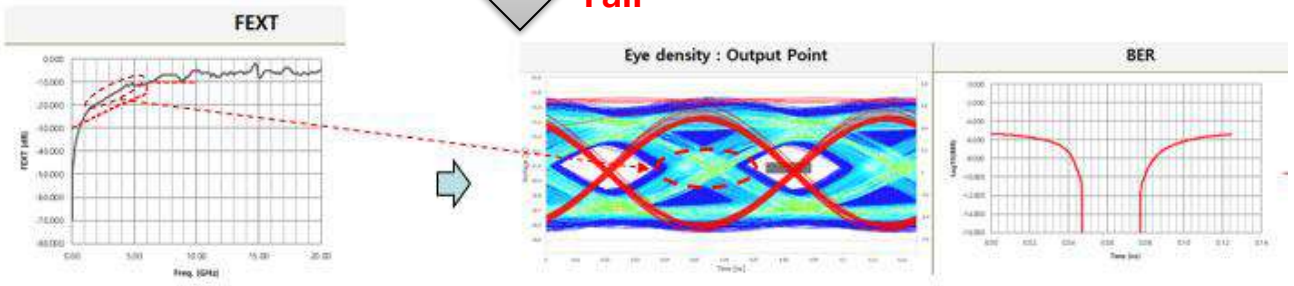
ACVS Basic report example of Good ch, Satisfy the FEXT limit (far end cross-talk summation)

ACVS EYE/BER report example of Good ch, With less Jitter noise

One click

Pass

Fail



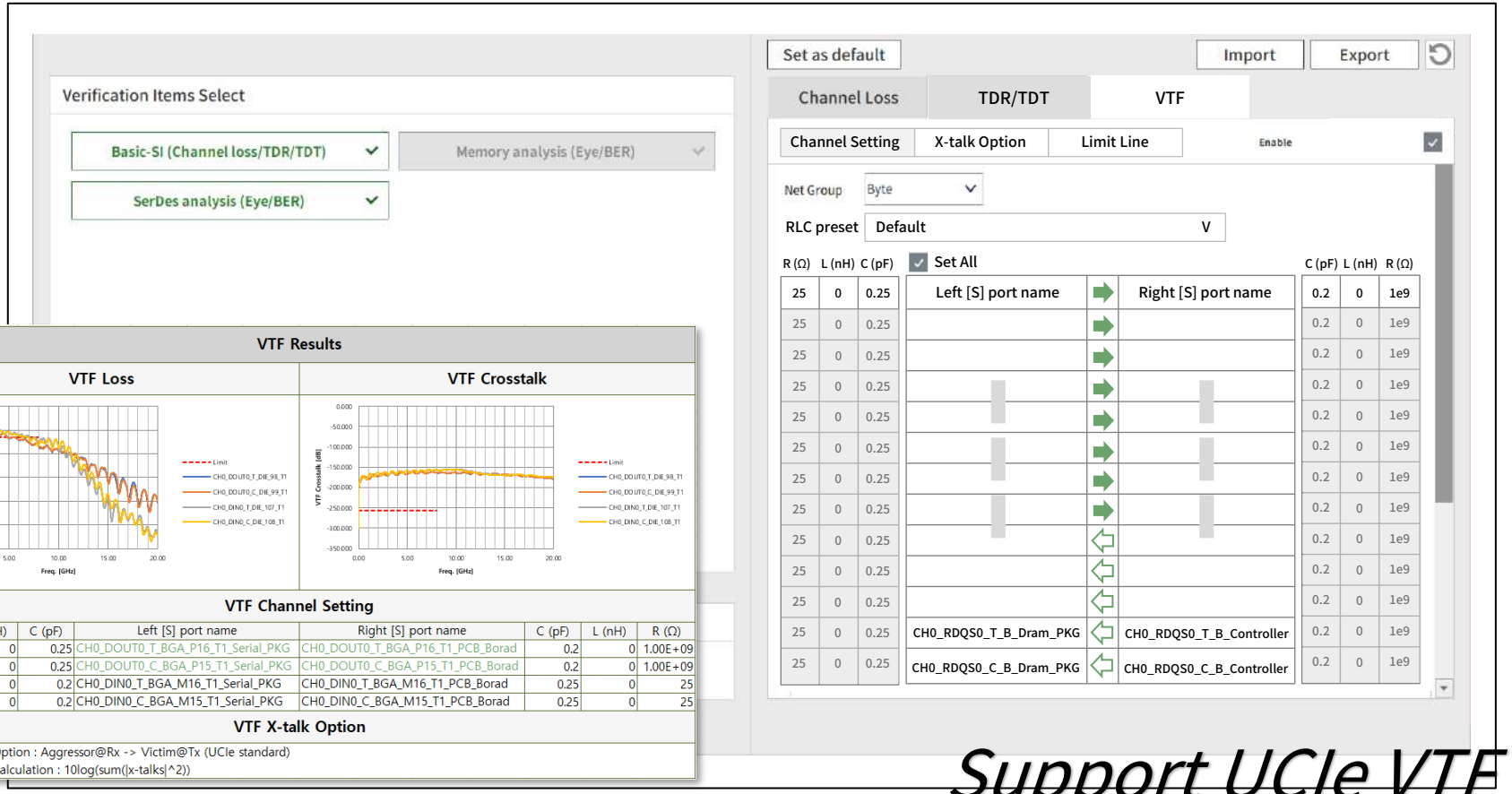
CVS Basic report example of Bad ch, Over e FEXT limit (far end cross-talk summation)

ACVS EYE/BER report example of Bad ch, With more Jitter noise caused by FEXT

2. 시뮬레이션 통한 SPGTI 설계 :

ACVS : UCIe VTF 분석을 위한 모든 설정 환경 제공

- 양방향 분석 설정 제공
- UCIe 표준 Tx/Rx RLC Termination 조건 및 Limit line 측정 설정 제공
- Report 자동 생성 기능 제공

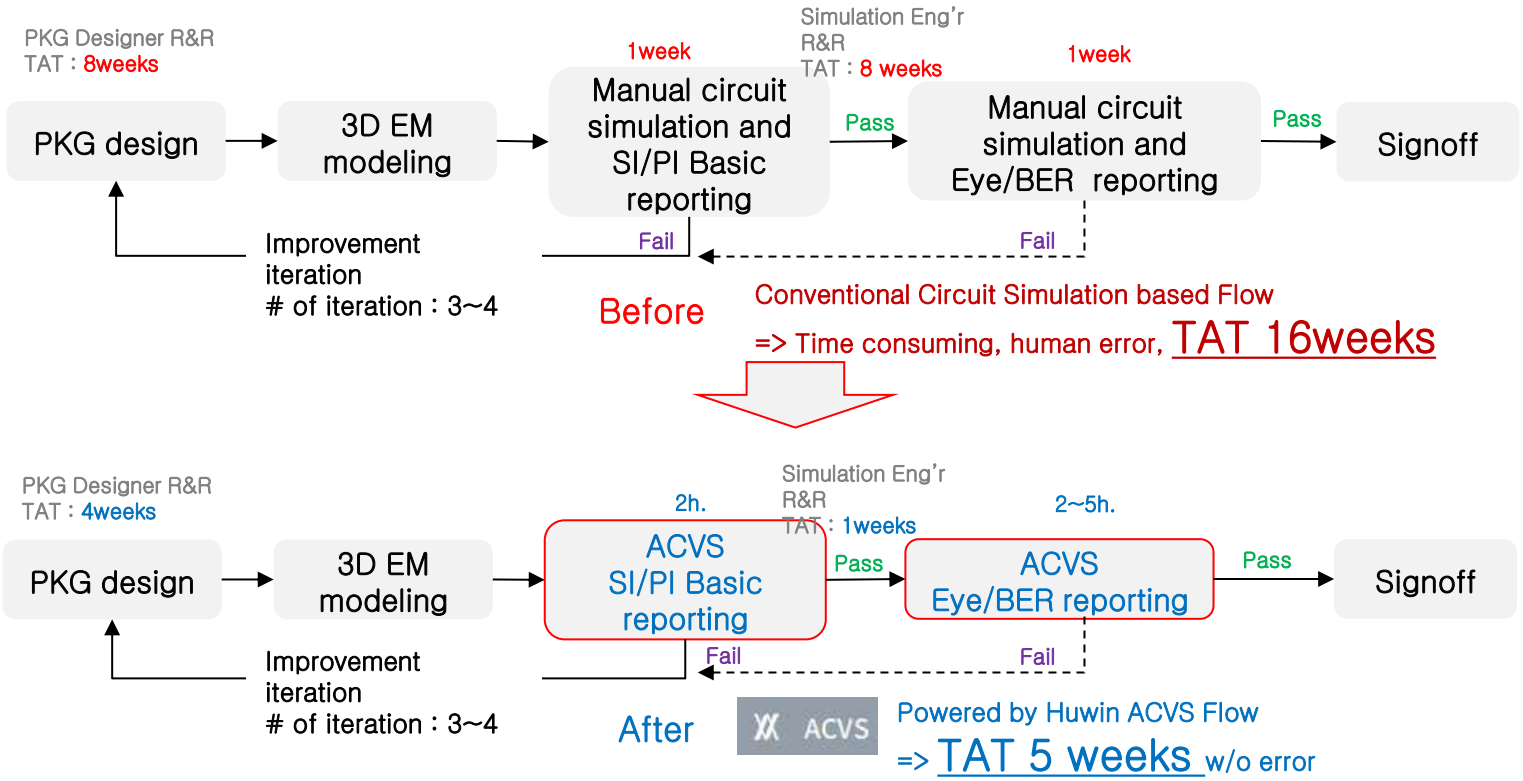


Support UCIe VTF

2. 시뮬레이션 통한 SPGTI 설계 :

History & Success Story : ACVS flow

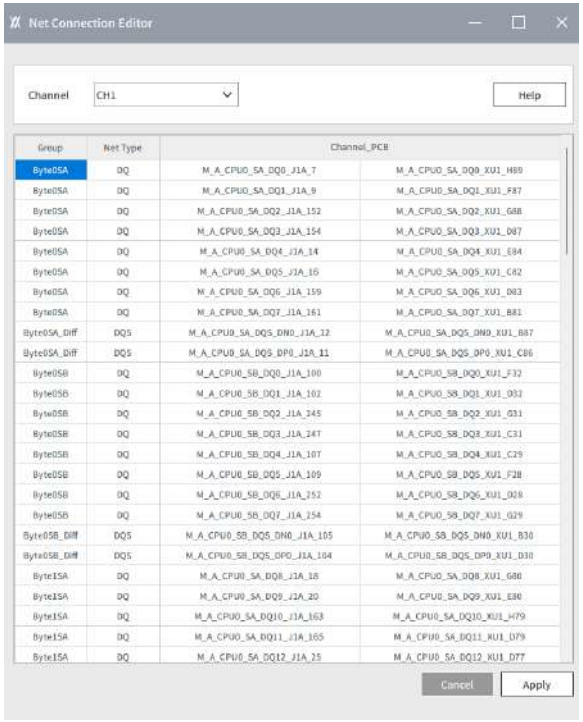
- Over 10 years, delivering the finest SI/PI solutions, ensuring trust and satisfaction among our clients.
- ACVS provides the capacity for handling of large-size S-parameters (HBM) and efficiency by new developed SimNX solver
- Compared to conventional circuit simulators, ACVS flow provides fast and fully automated analysis and reporting

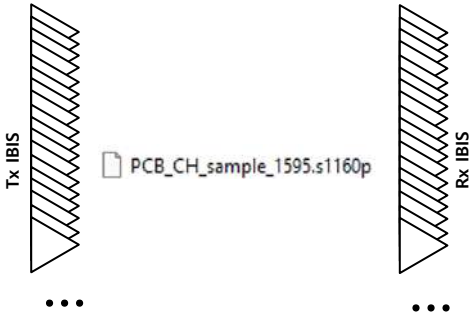


2. 시뮬레이션 통한 SPGTI 설계 :

Cases study: LPDDR5x (Transient simulation) 1160-ports Ch. model

- ✓ 6.4Gbps, step->UI/32, sim. Hawk-eye Fast option setting
- ✓ Tx/Rx IBIS models: Non-linear model (Rising/falling waveform, pull-up/pull-down I/V data)
- ✓ Simulation environment: AMD Ryzen 32-Cores, 512GB RAM





1160ports S-parameters

LPDDR5x CH1/2/3/4 (s1160p)
(File Size : 111.5GB)

Solution type	Conditions	Analysis time
Conventional solver	Can not handle the large Ch. model	NA
ACVS	-auto setting -auto reporting	Basic SI: 6h Memory IBIS : 2h. 2m.

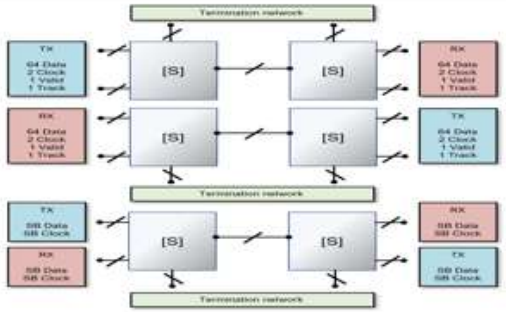
Transient simulation comparison

2. 시뮬레이션 통한 SPGTI 설계 :

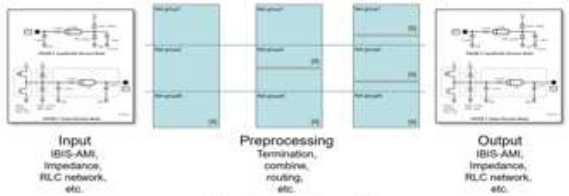
미세 배선 성능 분석을 위한 SI/PI 시뮬레이터 기술 개발

미세 배선 채널 구성 및 전처리 기술 개발

- ✓ 향상된 사용성 및 효율성의 채널 구성 모듈 개발
- ✓ S-parameter 채널 전처리 기능 개발



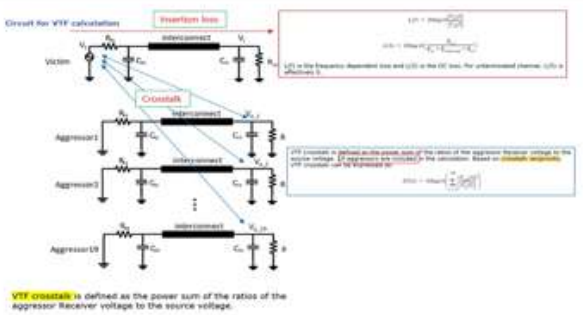
미세 배선 채널 구성 모듈(+GUI) 개발



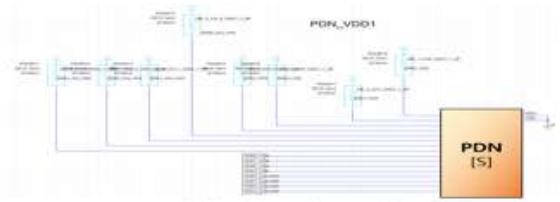
채널 전처리 기능 개발

SI/PI 핵심 성능 분석 기술 개발

- ✓ IL/RL/X-talk, TDR, VTF등 SI 핵심 성능 분석 모듈
- ✓ |Z|, 등가 R/L/C 추출 등 PI 핵심 성능 분석 모듈



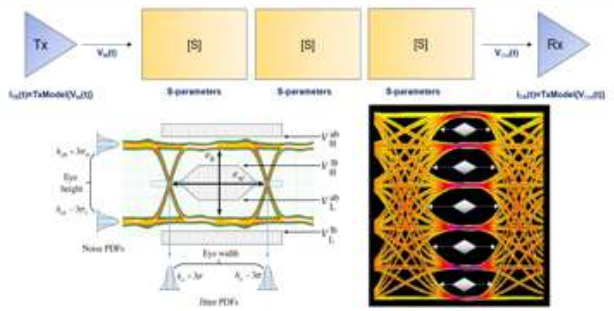
SI 핵심 성능 분석 모듈 개발



PI 핵심 성능 분석 모듈 개발

PAM-n 분석 및 측정 기술 개발

- ✓ PAM-n Eye-diagram 시뮬레이션 및 측정 모듈 개발
- ✓ Chart 생성 및 측정 결과 Reporting 모듈 개발



PAM-n Eye 시뮬레이션 및 측정 모듈 개발

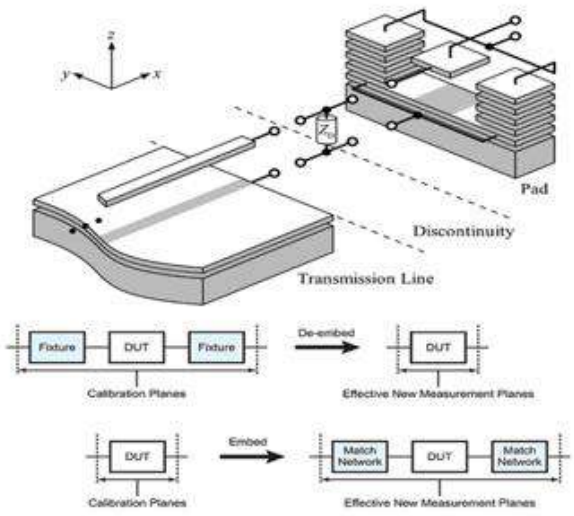
분석 결과 Chart 및 Report 생성 모듈 개발

2. 시뮬레이션 통한 SPGTI 설계 :

미세 배선 측정을 위한 광대역 측정 및 De-embedding 기술 개발

최대 80GHz 대역 De-embedding(DE) 기술 개발

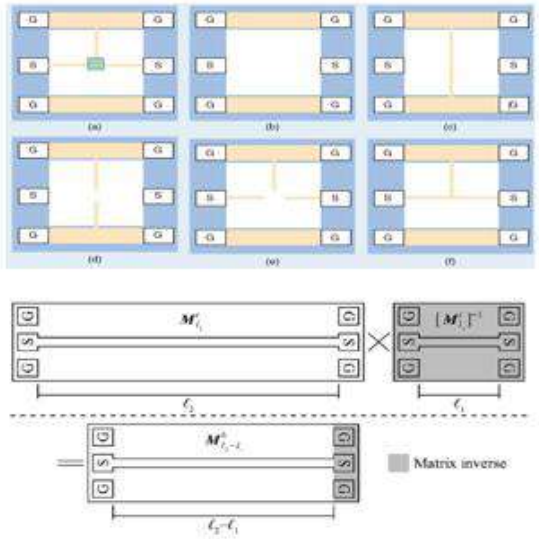
- ✓ 미세 배선 성능 평가를 위한 종래 기법 검토
- ✓ 미세 구조 및 80GHz 대역 측정용 DE 기술 개발



80GHz 대역급 De-embedding 기술 개발

um급 미세 배선 측정을 위한 Text fixture 개발

- ✓ 개발된 DE 기법 적용을 위한 Test fixture 필요
- ✓ 광대역 측정 편차를 최소화하기 위한 신규 구조 개발



2~5um 미세 배선 측정용 고정밀 Test fixture 구조 개발

80GHz대역 성능 평가를 위한 110GHz 측정 환경 구축

- ✓ 80GHz DE 안정성 확보를 위한 대역 마진 필요
- ✓ 110GHz 대역급 초광대역 Diff. pair 측정 환경 구축

종래 50GHz 대역으로 부터 110GHz 대역 확장 측정 환경 구축

최대 80GHz 대역의 성능 평가를 위한 110GHz 측정 환경 구축

2. 시뮬레이션 통한 SPGTI 설계 :

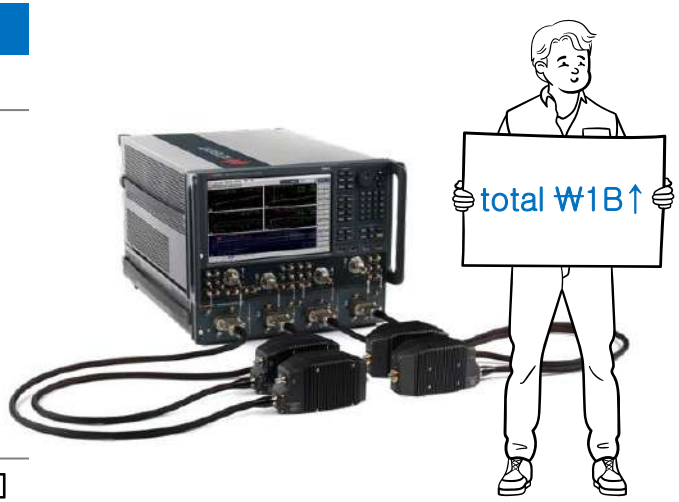
미세 배선 측정을 위한 광대역 측정 및 De-embedding 기술 개발
110 GHz Measurement Setup: Instruments and Accessories

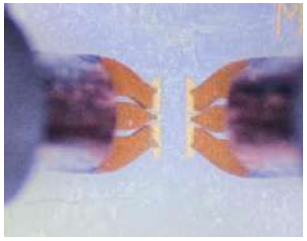
Instruments

[Keysight N5225B (900Hz~50GHz)]

[N5292A (4-port Milimeter wave test set controller)]

[N5293AX02 (Milimeter-wave frequency extender)]





Accessories

[DC to 110GHz 1.0mm calibration kit]

[1.0mm 110GHz cables & connectors]

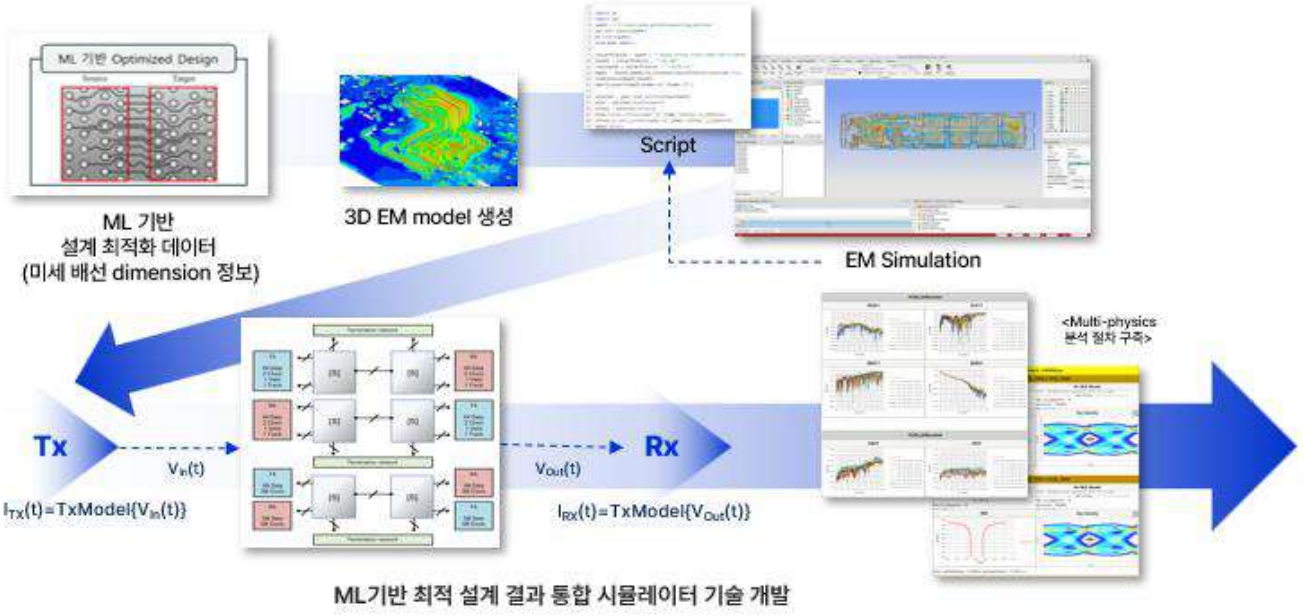
[110GHz Probe & calibration substrate]

2. 시뮬레이션 통한 SPGTI 설계 :

ML기반 최적 설계 결과 통합 시뮬레이터 기술 개발 및 Multi-physics 분석 절차 구축

ML기반 최적 설계 결과를 연동하는 통합형 시뮬레이터 개발

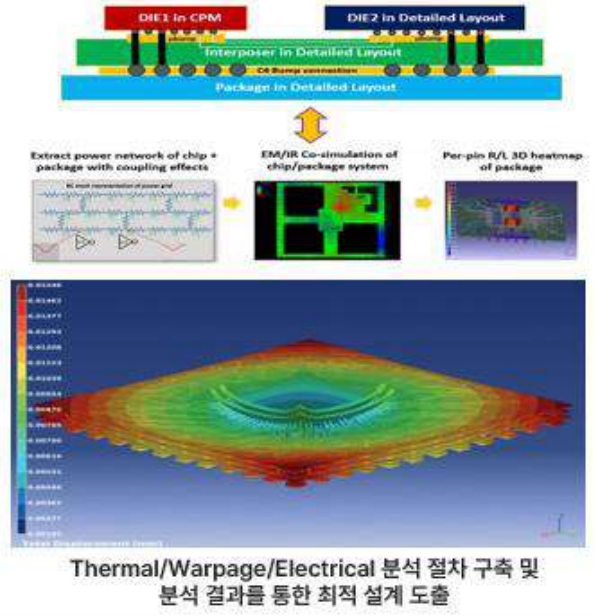
- ✓ 최적 설계 결과로 부터 EM model 생성 및 S-parameters 추출 기술 개발
- ✓ 미세 배선 채널 시스템 구성/분석/Reporting 절차 통합 자동화 기술 개발



ML기반 최적 설계 결과 통합 시뮬레이터 기술 개발

Multi-physics 분석 절차 및 최적 설계 방법론 구축

- ✓ Thermal/Warpage/Electrical 분석 절차 구축
- ✓ Multi-physics 성능을 반영한 최적 설계 방법론 구축



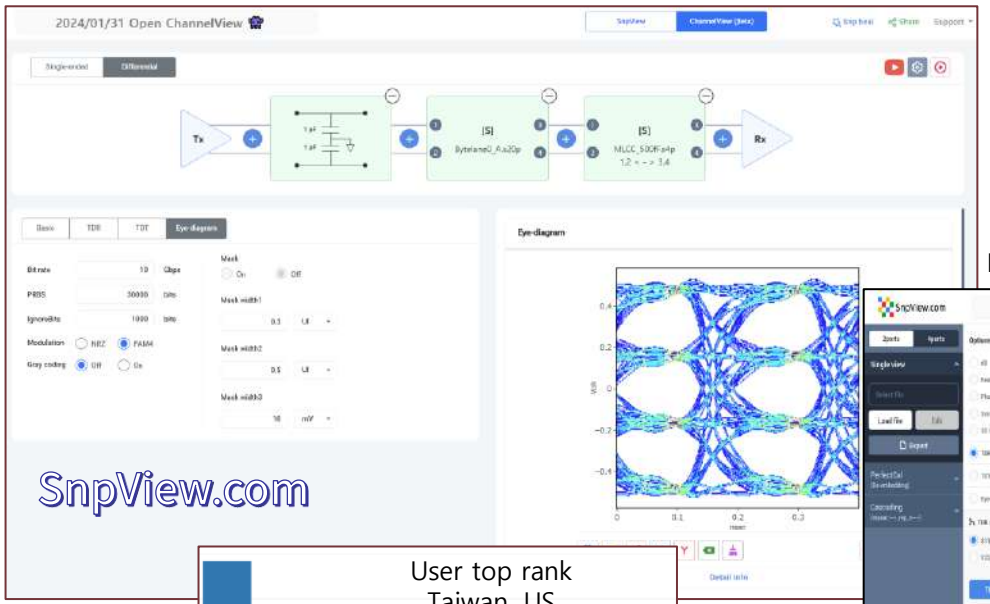
Thermal/Warpage/Electrical 분석 절차 구축 및
분석 결과를 통한 최적 설계 도출

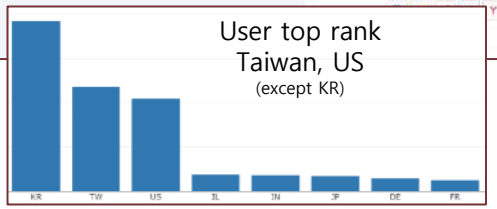
2. 시뮬레이션 통한 SPGTI 설계 :

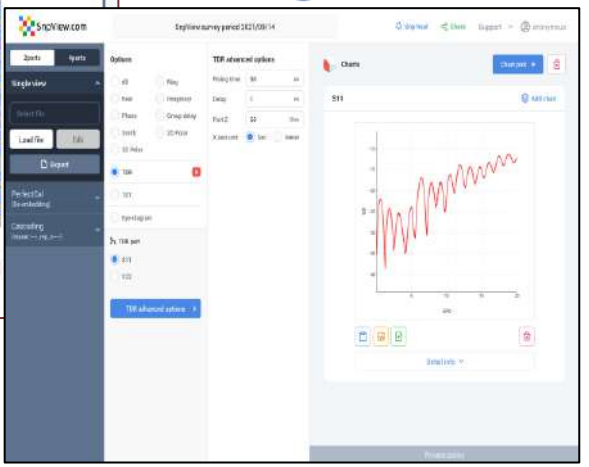
SnpView.com

A High-Value, Professional Signal Integrity Simulator—Free to Use Online

- Basic charts: dB/phase, real/img, smith chart, group delay, passivity
- Advanced charts: **TDR, TDT, Eye-diagram (w. EQ, Jitter, Noise)**
- Advanced functions: **PerfectCal®** (lite), Snp Heal
- Powered by **SimNX**





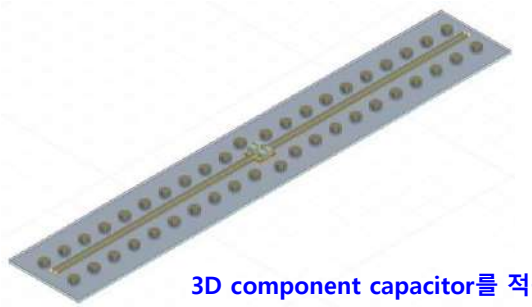


Visitors
✓ **500~1000/**day

Powered by SimNX

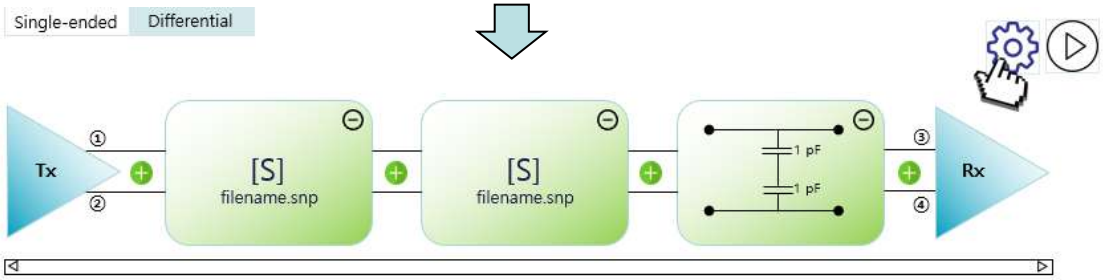
2. 시뮬레이션 통한 SPGTI 설계 :

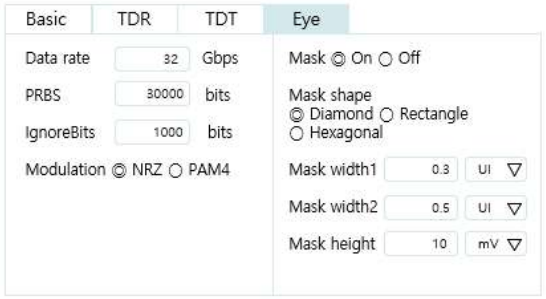
SnpView.com/CV => Channel View

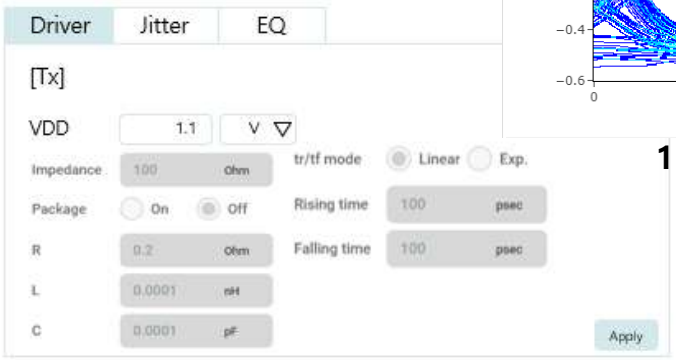


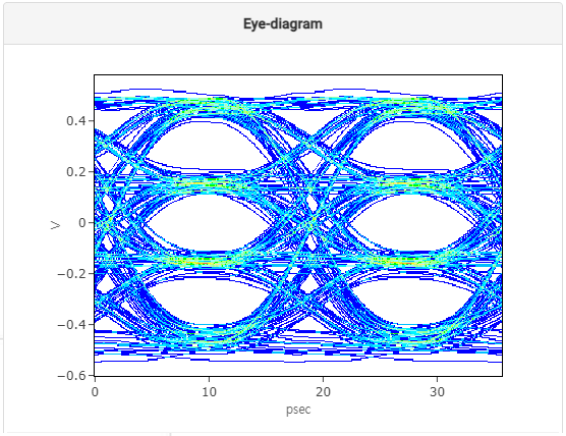
3D component capacitor를 적용한 HFSS

- **연산 기능**
  - ➢ Lumped component 생성 및 연결
  - ➢ MLCC 및 기타 S-parameter 연결
  - ➢ 전체 채널 시스템의 IL/RL, TDR, TDT 연산
  - ➢ 전체 채널 시스템의 Eye-diagram 연산
  - ➢ RLC 패키지 값 적용, Tx/Rx Driver model, Jitter, EQ







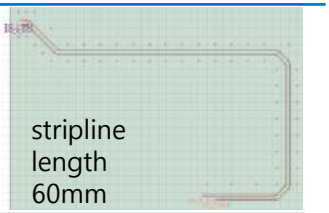


112Gbps PAM4 Eye

2. 시뮬레이션 통한 SPGTI 설계 :

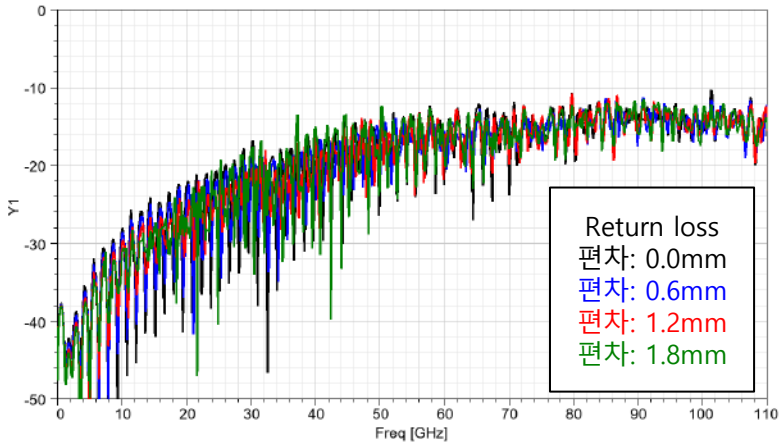
Skew 에 의한 SI 영향 분석

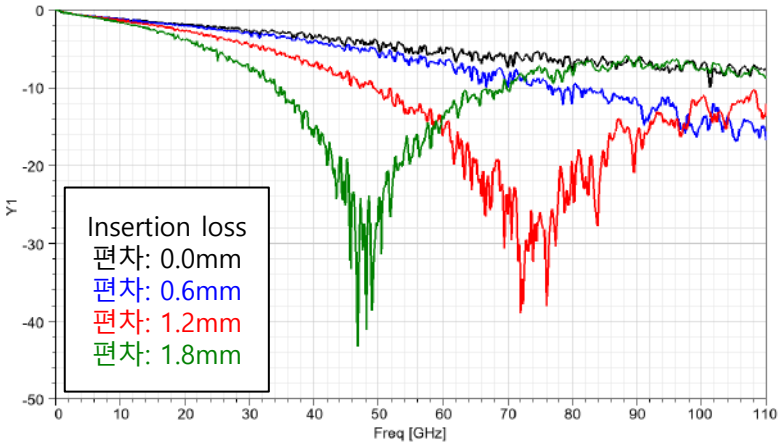
❖ 해석 조건
- ➢ 주파수: ~110GHz
- ➢ P/N 길이 편차: 0mm, 0.6mm, 1.2mm, 1.8mm



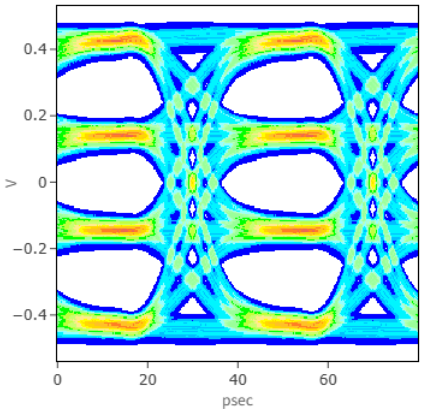
Name	Type	Thickness (m...	M..	Conductivity (...	Dielectric...	Loss tangent
L1	METAL	0,035	ODB,..	5,95901E+07	O.. 2,99	0,0044
dielectric1	DIELECTRIC	0,105	ODB,..	0	2,99	0,0044
L2	METAL	0,018	ODB,..	5,95901E+07	O.. 2,99	0,0044
dielectric2	DIELECTRIC	0,105	ODB,..	0	2,99	0,0044
L3	METAL	0,035	ODB,..	5,95901E+07	O.. 2,99	0,0044

❖ 길이 60mm인 strip line의 P/N 길이 편차에 따른 특성
- ➢ Return loss 특성은 같음(동일한 임피던스)
- ➢ Insertion loss는 편차가 클수록 낮은 주파수에서 공진 발생

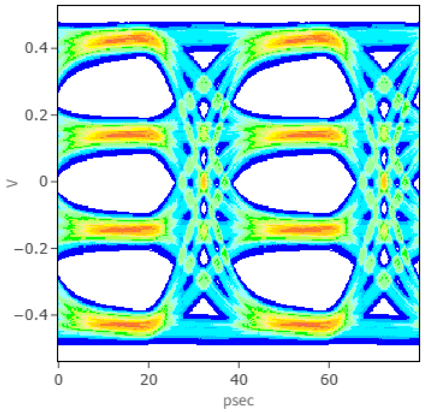




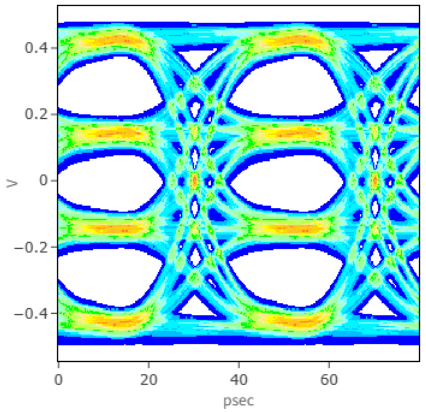
50Gbps(0.0mm)



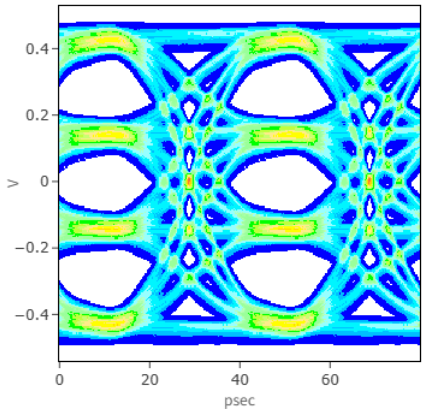
50Gbps(0.6mm)



50Gbps(1.2mm)



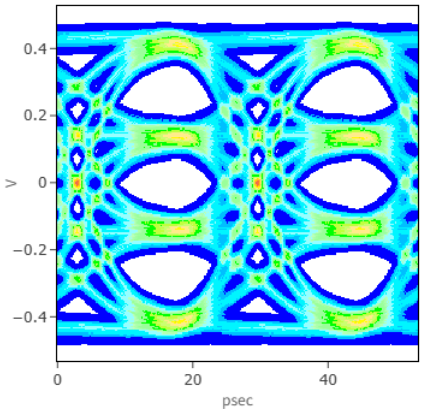
50Gbps(1.8mm)



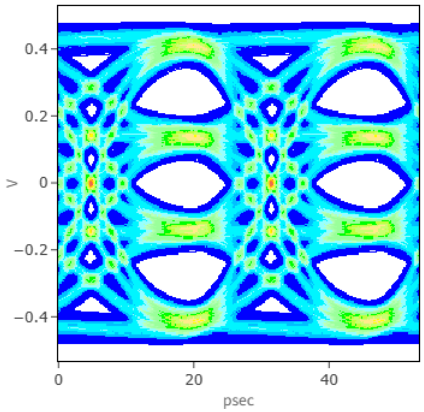
2. 시뮬레이션 통한 SPGTI 설계 :

Skew 에 의한 SI 영향 분석

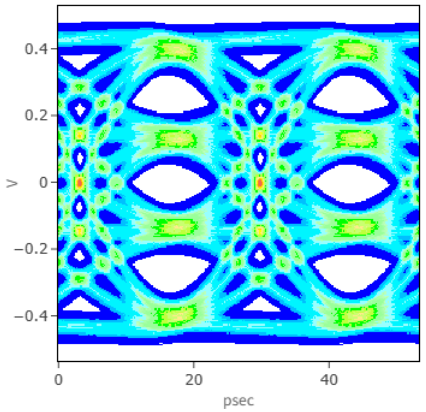
75Gbps(0.0mm)



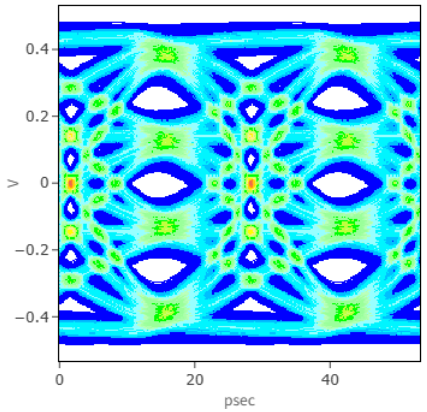
75Gbps(0.6mm)



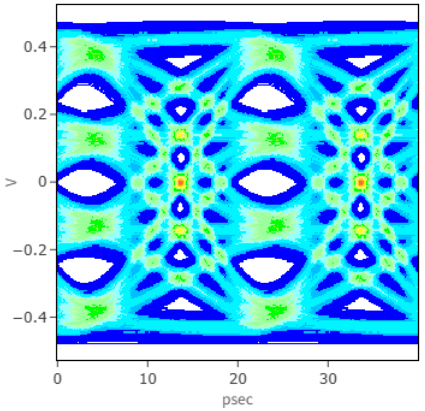
75Gbps(1.2mm)



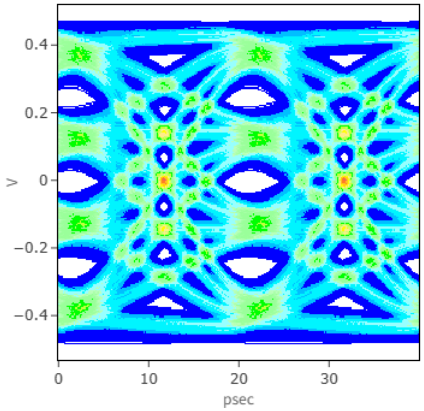
75Gbps(1.8mm)



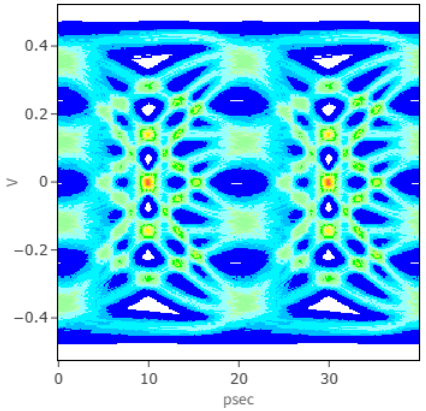
100Gbps(0.0mm)



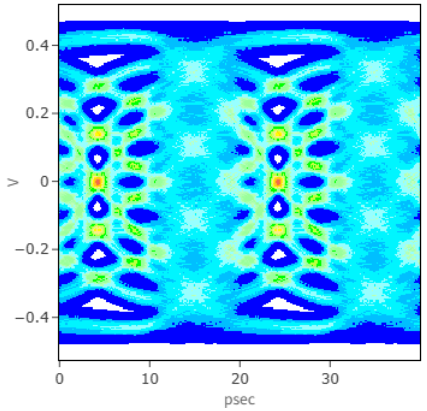
100Gbps(0.6mm)



100Gbps(1.2mm)



100Gbps(1.8mm)

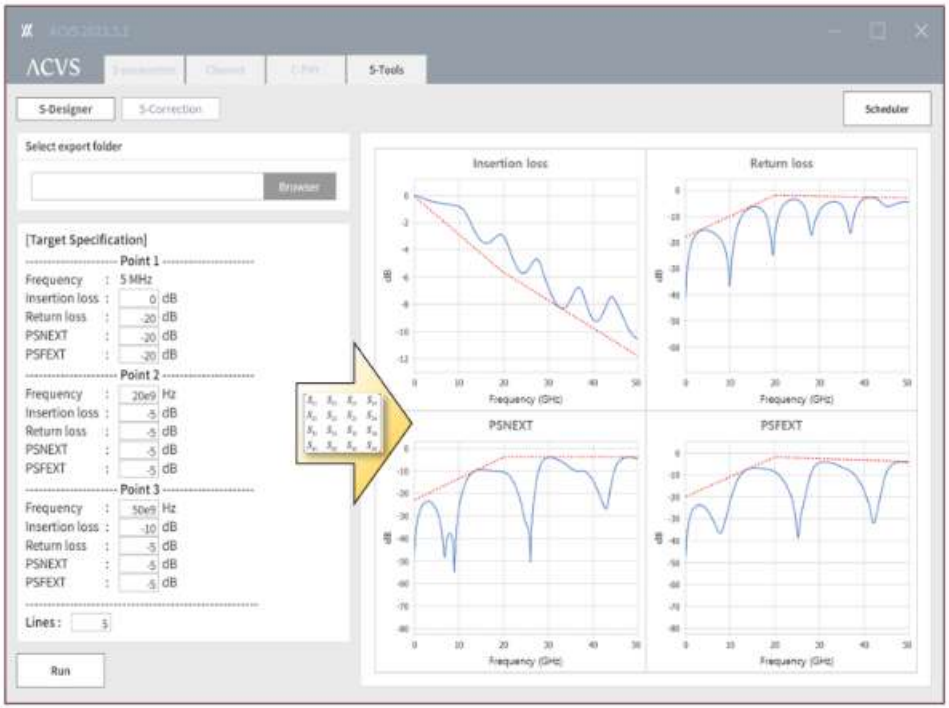


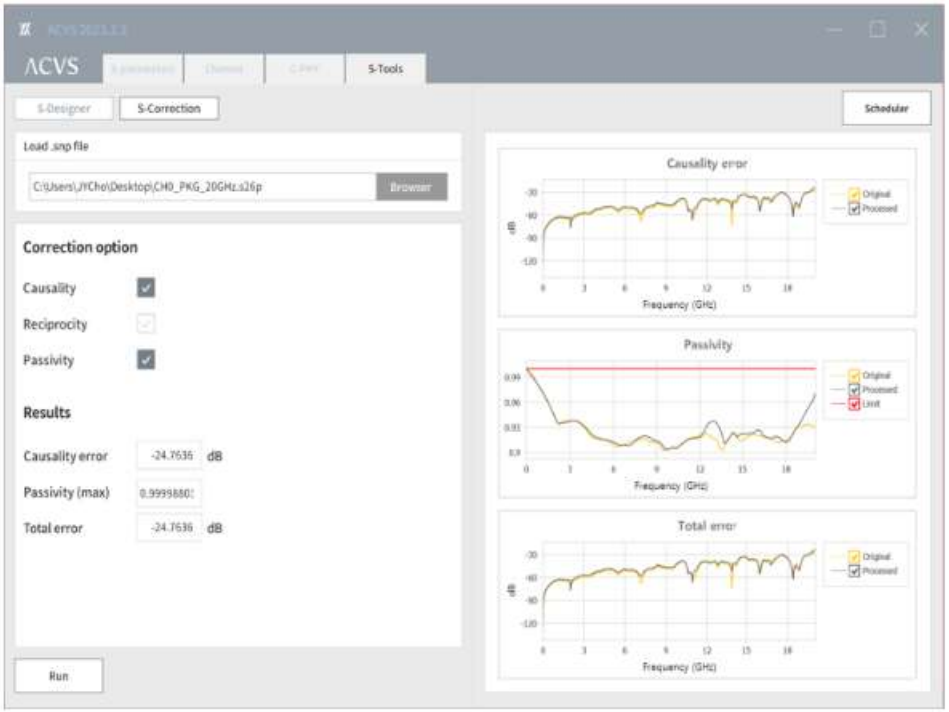
2. 시뮬레이션 통한 SPGTI 설계 :

Xtalk test: ACVS S-Tools => S-Designer, S-Correction

- S-Designer: 사용자가 원하는 Insertion loss, Return loss, Xtalk 규격의 S-parameter 생성
  - 설계/제조를 위한 고속 채널 시스템의 성능을 예측

- S-Correction: EM 해석 또는 측정에서 발생하는 Causality / Passivity 보정
  - 채널 시스템 분석의 안정성 확보

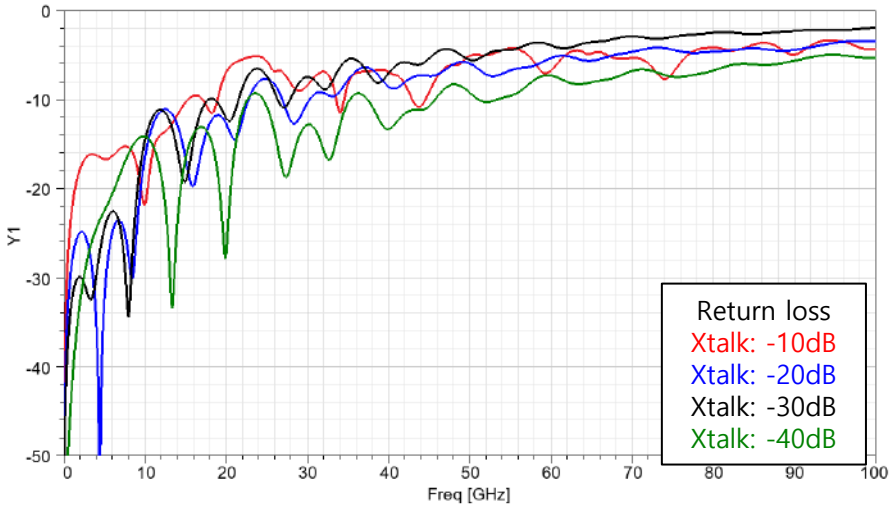


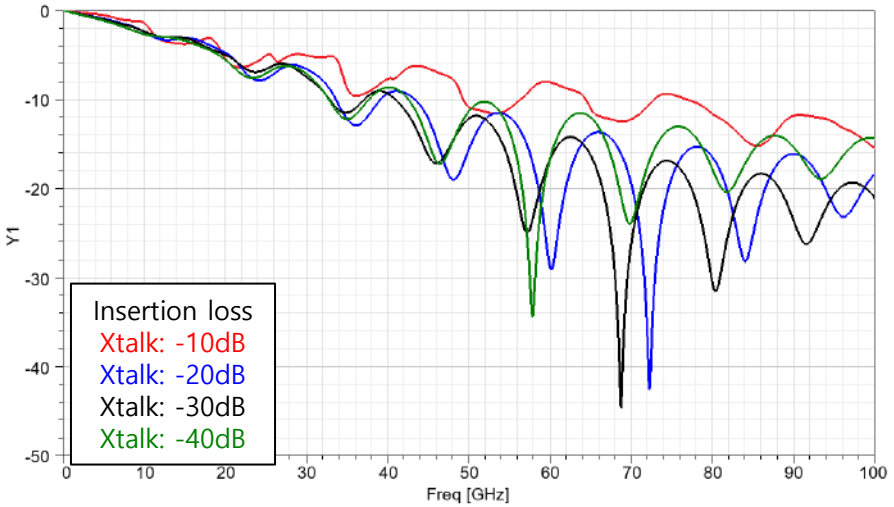


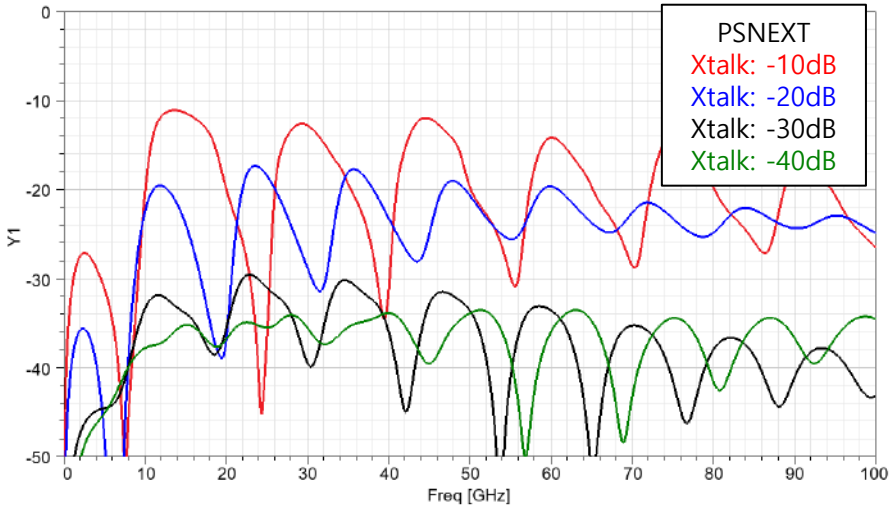
2. 시뮬레이션 통한 SPGTI 설계 :

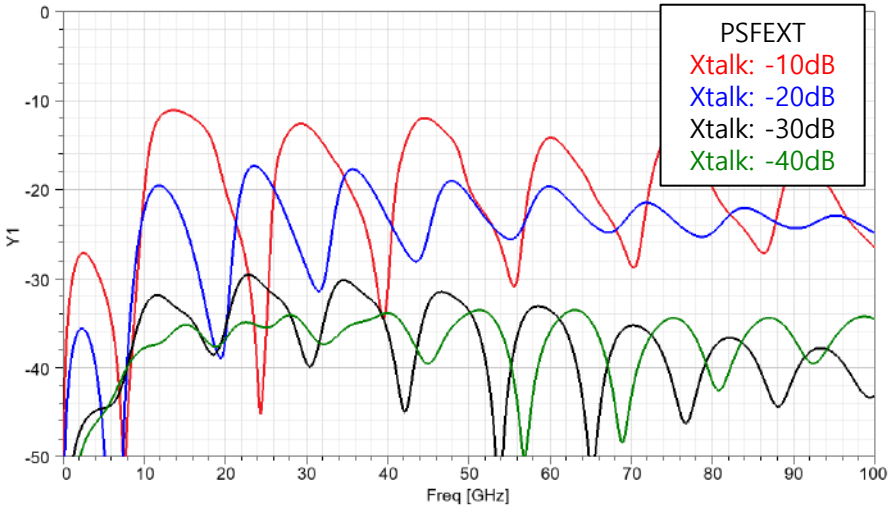
Xtalk test: ACVS S-Tools => S-Designer, S-Correction

❖ S-Designer로 생성된 S-parameter 결과 비교(PSNEXT와 PSFEXT를 각각 -10dB, -20dB, -30dB, -40dB 이하로 설정)





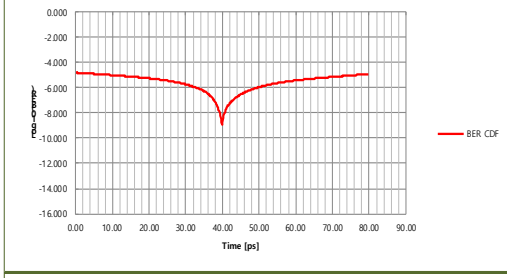
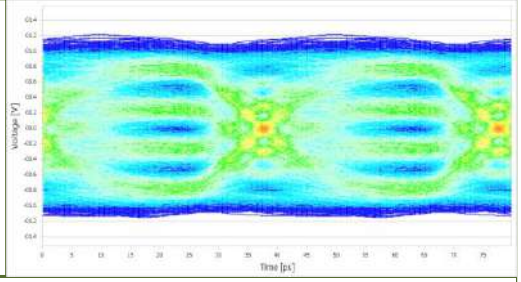




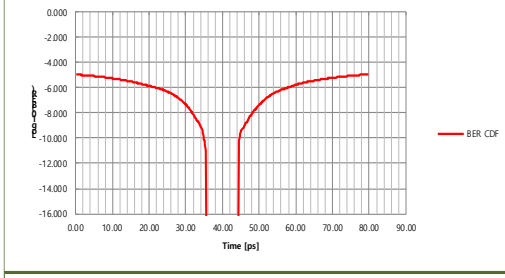
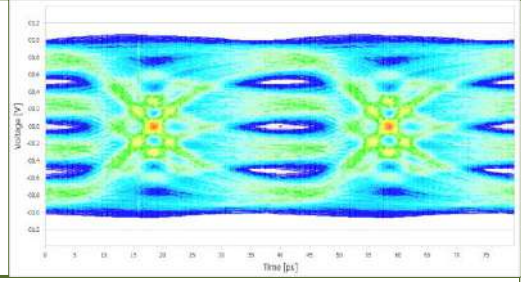
2. 시뮬레이션 통한 SPGTI 설계 :

Xtalk test: ACVS S-Tools => S-Designer, S-Correction

❖ PSNEXT와 PSFEXT가 -10dB 이하일때 eye 해석 결과

Case1 : Forward / 2^15 / X-talk On / New Spec #1 / 32 / General	
Diff. Net1 : Out1_P_10dB / Out1_N_10dB	
Tx IBIS Model	**Rx IBIS Model**
Undefined : PAM4_tx_v1@[PU_Z:50.00, PD_Z:50.00, RT:--ns, FT:--ns] [typ] [Internal 1V] ========== AMI setting ==========	Undefined : pam4_rx@[GC:Inf, PC:Inf] [typ] [Internal 1V]
BER	**Eye density**
	
[User Mask] Width:0.00 ps (+0.00 ps), Height:5.19 mV (+0.00 mV), Result: Fail [Point mask] Width:0.0ps, Height:5.2 mv	

Xtalk를 반영한 eye 결과

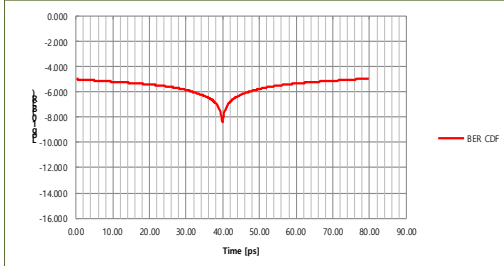
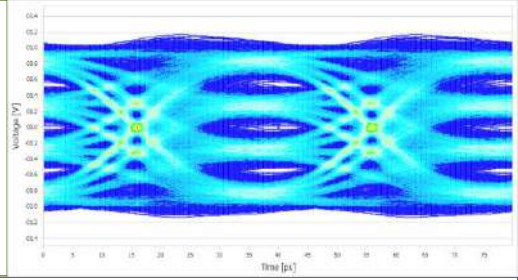
Case1 : Forward / 2^15 / X-talk Off / New Spec #1 @Profile / 32 / General	
Diff. Net1 : Out1_P_10dB / Out1_N_10dB	
Tx IBIS Model	**Rx IBIS Model**
Undefined : PAM4_tx_v1@[PU_Z:50.00, PD_Z:50.00, RT:--ns, FT:--ns] [typ] [Internal 1V] ========== AMI setting ==========	Undefined : pam4_rx@[GC:Inf, PC:Inf] [typ] [Internal 1V]
BER	**Eye density**
	
[User Mask] Width:8.00 ps (+3.84 ps), Height:65.19 mV (+25.74 mV), Result: Pass [Point mask] Width:8.0ps, Height:65.2 mv	

Xtalk를 반영하지 않은 eye 결과

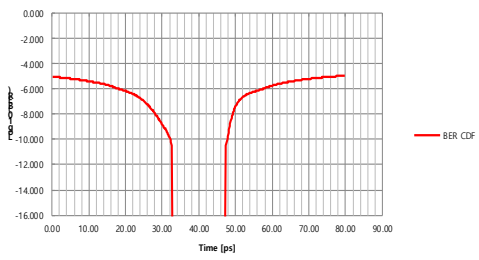
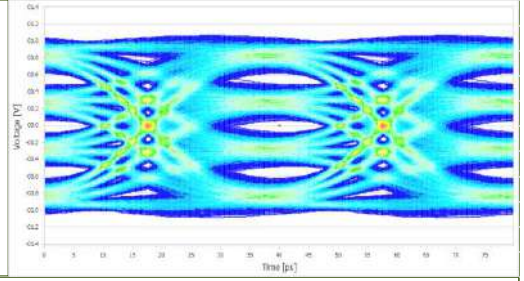
2. 시뮬레이션 통한 SPGTI 설계 :

Xtalk test: ACVS S-Tools => S-Designer, S-Correction

❖ PSNEXT와 PSFEXT가 -20dB 이하일때 eye 해석 결과

Case1 : Forward / 2^15 / X-talk On / New Spec #1 / 32 / General	
Diff. Net1 : Out1_P_20dB / Out1_N_20dB	
Tx IBIS Model	**Rx IBIS Model**
Undefined : PAM4_tx_v1@[PU_Z:50.00, PD_Z:50.00, RT:--ns, FT:--ns] [typ] [Internal 1V] ========== AMI setting ==========	Undefined : pam4_rx@[GC:Inf, PC:Inf] [typ] [Internal 1V]
BER	**Eye density**
	
[User Mask] Width:7.20 ps (+3.36 ps), Height:40.43 mV (+13.92 mV), Result: Pass [Point mask] Width:7.2ps, Height:40.4 mv	

Xtalk를 반영한 eye 결과

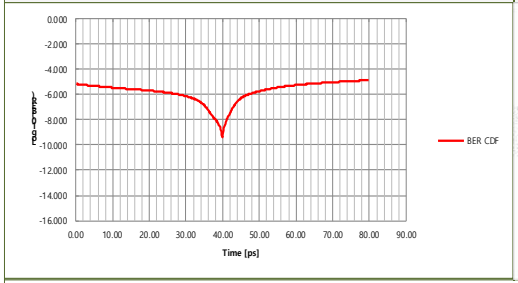
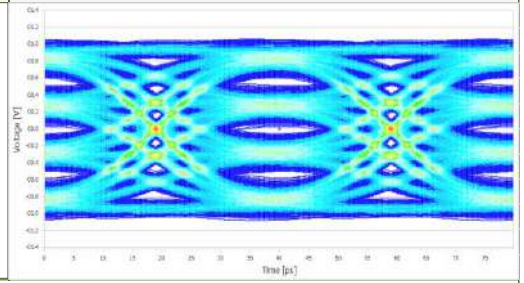
Case1 : Forward / 2^15 / X-talk Off / New Spec #1 @Profile / 32 / General	
Diff. Net1 : Out1_P_20dB / Out1_N_20dB	
Tx IBIS Model	**Rx IBIS Model**
Undefined : PAM4_tx_v1@[PU_Z:50.00, PD_Z:50.00, RT:--ns, FT:--ns] [typ] [Internal 1V] ========== AMI setting ==========	Undefined : pam4_rx@[GC:Inf, PC:Inf] [typ] [Internal 1V]
BER	**Eye density**
	
[User Mask] Width:14.56 ps (+7.04 ps), Height:137.10 mV (+55.88 mV), Result: Pass [Point mask] Width:14.6ps, Height:137.1 mv	

Xtalk를 반영하지 않은 eye 결과

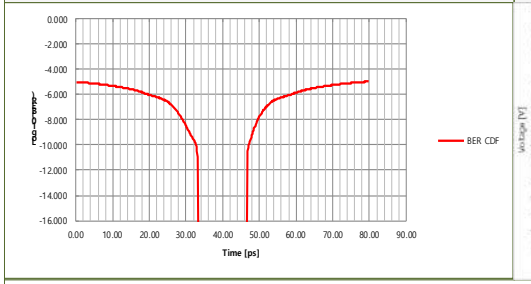
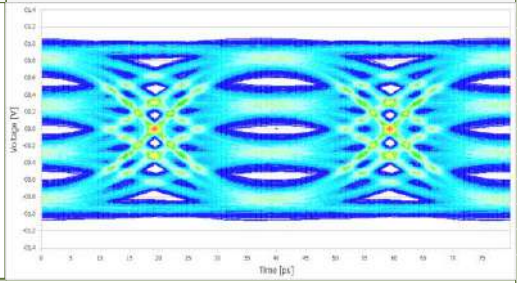
2. 시뮬레이션 통한 SPGTI 설계 :

Xtalk test: ACVS S-Tools => S-Designer, S-Correction

❖ PSNEXT와 PSFEXT가 -30dB 이하일때 eye 해석 결과

Case1 : Forward / 2^15 / X-talk On / New Spec #1 / 32 / General	
Diff. Net1 : Out1_P_30dB / Out1_N_30dB	
Tx IBIS Model	**Rx IBIS Model**
Undefined : PAM4_tx_v1@[PU_Z:50.00, PD_Z:50.00, RT:--ns, FT:--ns] [typ] [Internal 1V] ========== AMI setting ==========	Undefined : pam4_rx@[GC:Inf, PC:Inf] [typ] [Internal 1V]
BER	**Eye density**
	
[User Mask] Width:10.88 ps (+5.28 ps), Height:80.06 mV (+22.13 mV), Result: Pass [Point mask] Width:10.9ps, Height:80.1 mv	

Xtalk를 반영한 eye 결과

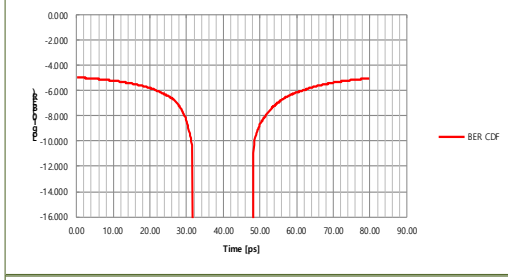
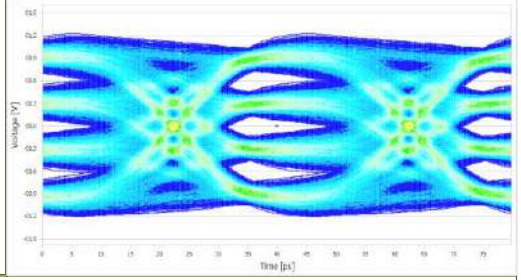
Case1 : Forward / 2^15 / X-talk Off / New Spec #1 @Profile / 32 / General	
Diff. Net1 : Out1_P_30dB / Out1_N_30dB	
Tx IBIS Model	**Rx IBIS Model**
Undefined : PAM4_tx_v1@[PU_Z:50.00, PD_Z:50.00, RT:--ns, FT:--ns] [typ] [Internal 1V] ========== AMI setting ==========	Undefined : pam4_rx@[GC:Inf, PC:Inf] [typ] [Internal 1V]
BER	**Eye density**
	
[User Mask] Width:12.64 ps (+6.08 ps), Height:103.59 mV (+34.42 mV), Result: Pass [Point mask] Width:12.6ps, Height:103.6 mv	

Xtalk를 반영하지 않은 eye 결과

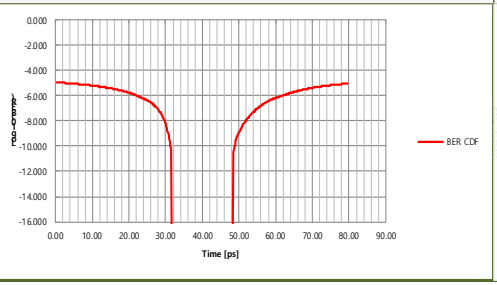
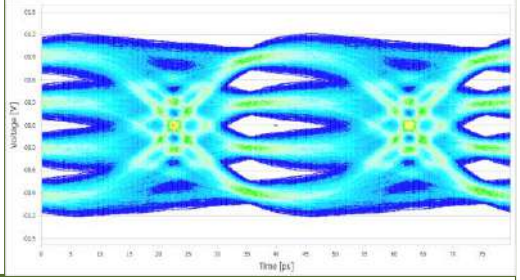
2. 시뮬레이션 통한 SPGTI 설계 :

Xtalk test: ACVS S-Tools => S-Designer, S-Correction

❖ PSNEXT와 PSFEXT가 -40dB 이하일때 eye 해석 결과

Case1 : Forward / 2^15 / X-talk On / New Spec #1 / 32 / General	
Diff. Net1 : Out1_P_40dB / Out1_N_40dB	
Tx IBIS Model	**Rx IBIS Model**
Undefined : PAM4_tx_v1@[PU_Z:50.00, PD_Z:50.00, RT:--ns, FT:--ns] [typ] [Internal 1V] ========== AMI setting ==========	Undefined : pam4_rx@[GC:Inf, PC:Inf] [typ] [Internal 1V]
BER	**Eye density**
	
[User Mask] Width:16.16 ps (+7.84 ps), Height:175.73 mV (+76.94 mV), Result: Pass [Point mask] Width:16.2ps, Height:175.7 mv	

Xtalk를 반영한 eye 결과

Case1 : Forward / 2^15 / X-talk Off / New Spec #1 @Profile / 32 / General	
Diff. Net1 : Out1_P_40dB / Out1_N_40dB	
Tx IBIS Model	**Rx IBIS Model**
Undefined : PAM4_tx_v1@[PU_Z:50.00, PD_Z:50.00, RT:--ns, FT:--ns] [typ] [Internal 1V] ========== AMI setting ==========	Undefined : pam4_rx@[GC:Inf, PC:Inf] [typ] [Internal 1V]
BER	**Eye density**
	
[User Mask] Width:16.16 ps (+7.84 ps), Height:180.72 mV (+82.01 mV), Result: Pass [Point mask] Width:16.2ps, Height:180.7 mv	

Xtalk를 반영하지 않은 eye 결과

2. 시뮬레이션 통한 SPGTI 설계 :

Next Generation Advanced Ch. Trends :

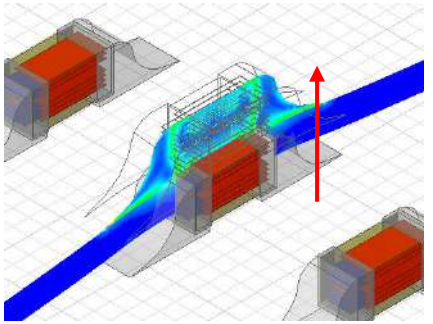
Signal :

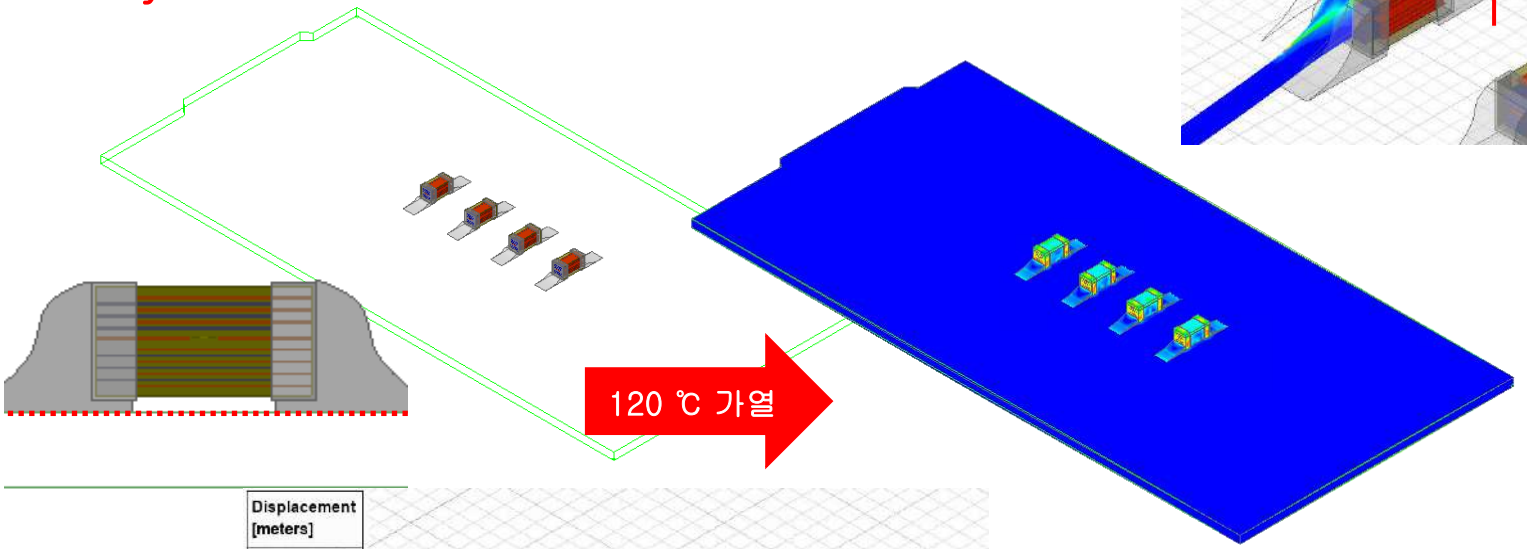
Power :

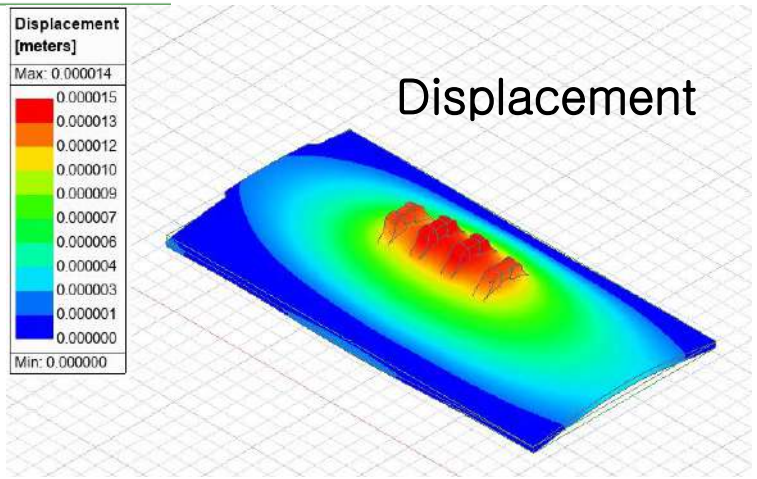
Ground :

Thermal :

Ansys AEDT Electro-Thermal-Mechanical

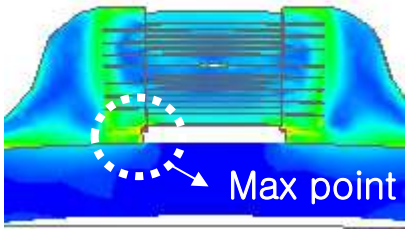






Displacement

Equivalent Stress



2. 시뮬레이션 통한 SPGTI 설계 :

How to Simulate Low Voltage, High Power 2000 Amps to a Dynamic Digital Load

$$Z_{Target} = \frac{\Delta V_{Max\ Ripple}}{\Delta I_{Max\ Transient\ Load}}$$

기존 Targe impedance

$$P = V_{in} \times I_{in} = DV_{in} \times \frac{1}{D} I_{in}$$

the ideal DC-DC converter equation

$$Z_{Target} = \frac{D \times V_{in} \times 5\%}{\frac{1}{D} \times I_{in\_max} \times 50\%}$$

$$= D^2 \frac{V_{in}}{I_{in\_max}} \times 10\%$$

$$= \frac{(D \times V_{in})^2}{P_{max}} \times 10\%$$

D(the duty cycle of the DC-DC regulator)
고려한 Targe impedance

- 고성능 Power Integrity (PI) 설계를 위해 Power Delivery Network (PDN)의 Electromagnetic (EM) simulation이 필수
- 전류가 수백A에서 수천A로 설계가 발전함에 따라 전통적인 rules-of-thumb과 data sheet examples만으로는 더 이상 충분하지 않음
- 2000 A의 전류가 100μΩ의 PCB PDN을 통과하면 100 mV의 IR drop과 100 Watts (W)의 전력 손실이 발생
- 2000A transient load stepper의 열 폭주를 방지하기 위해 수 냉각(water cooling)을 하지 않을 경우 최대 766 도 까지 상승 (자연 대류 조건)
- ET 시뮬레이션 통한 고 전류 설계에서 적절한 cooling solutions을 결정하고 다양한 thermal management strategies의 효과의 평가가 필수

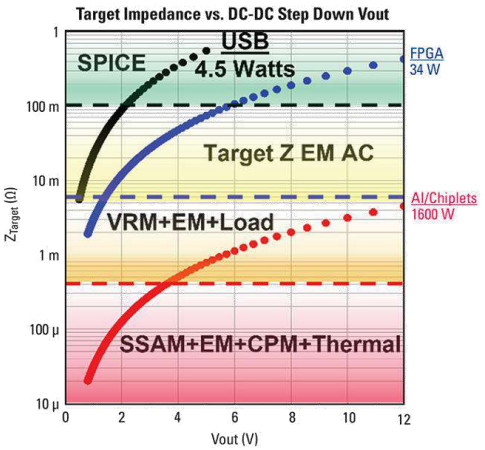


Figure 2. A plot showing how target impedance decreases with the output voltage of a DC-DC regulator for a given application where the power is held constant. As the output voltage drops the current increases proportionally, but target impedance decreases exponentially.

2. 시뮬레이션 통한 SPGTI 설계 :

PCB Layout and Thermal Design for High Density Modular Power Systems

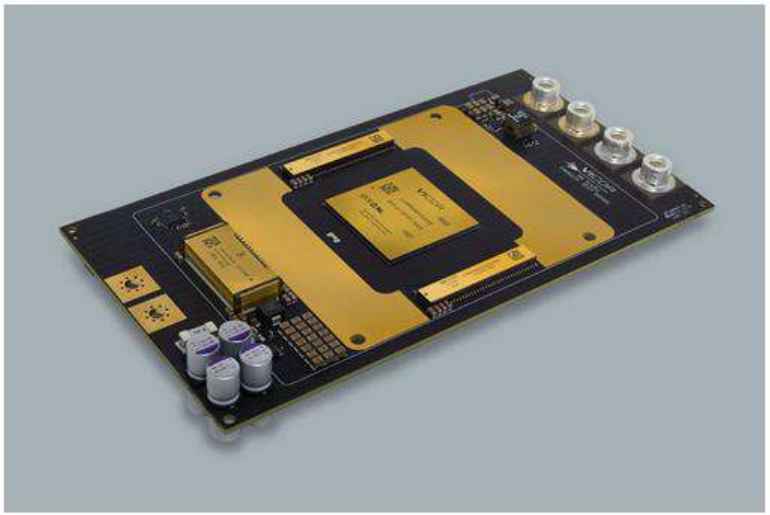


Figure 1: In this test board from Vicor, a PRM™ regulator and two VTM™ current multipliers mounted on a high-density PCB supply power to a load module that simulates a high-performance computing processor. In operation, a cold plate or heat sink would be mounted over the VTMs and load module, and another heat sink would be mounted on the PRM.

- 전통적으로 PCB는 부품 실장 및 배선 평면으로 취급되었으나, 고성능 컴퓨팅과 AI 프로세서와 같은 고밀도 부하에서는 PCB 레이아웃이 전력 성능에 미치는 영향이 매우 큼
- Voltage-regulation 요구 사항과 매우 빠른 transient slew rates로 인해 시스템 내의 모든 전압 강하 및 전력 손실은 성능에 부정적인 영향을 미침

2. 시뮬레이션 통한 SPGTI 설계 :

PCB Layout and Thermal Design for High Density Modular Power Systems

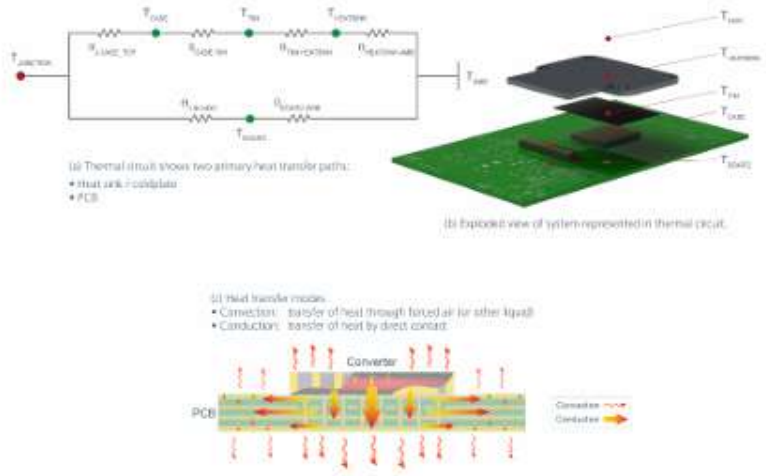


Figure 2. Conduction to and through the PCB is an important part of high-density thermal management, and requires the use of equivalent circuits to determine the most effective thermal paths (a), (b). Good thermal design optimizes both conduction and convection heat transfer modes (c).

- 전력 시스템 설계에서 열 관리의 목표는 열 발생 접점에서 주변 공기로 효율적으로 열을 전달하는 것
- 고밀도 시스템에서는 PCB 자체를 효율적인 열 전도체로 활용하기 위해 설계 초기 단계부터 PCB에 대한 상세한 열 전달 분석이 필수적임
- Thermal model은 부품 내부 접점에서 열을 방출하는 가장 낮은 impedance paths를 식별하며, 이를 통해 설계 시 구리 면적 확장 및 Thermal via를 사용하여 열 방출 잠재력을 최대화할 수 있음

2. 시뮬레이션 통한 SPGTI 설계 :

PCB Layout and Thermal Design for High Density Modular Power Systems

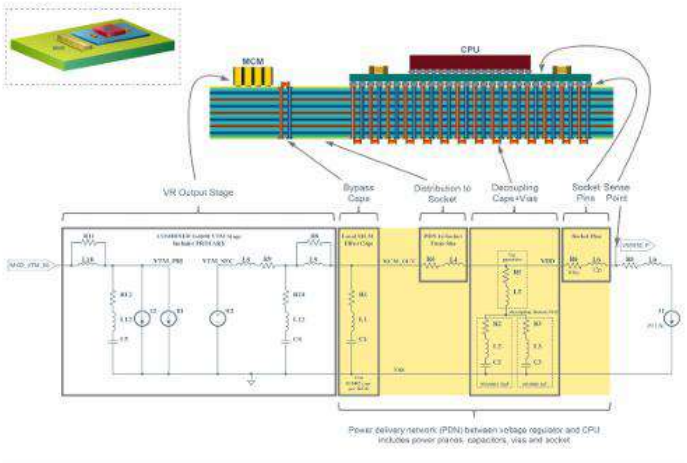
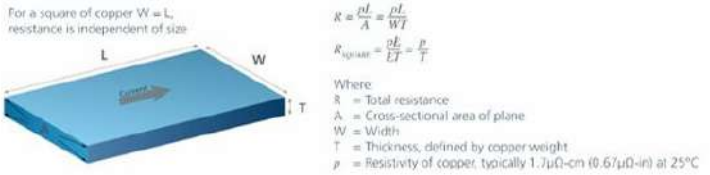
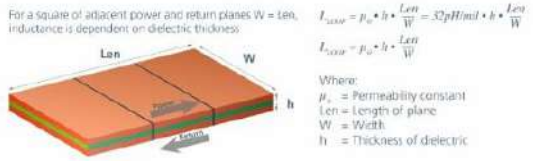


Figure 3. Impedances in the discrete components of the PDN between a voltage regulator and the CPU load, particularly at high frequencies and large load steps, can seriously impact the effectiveness of a power design.



Copper weight in ounces	Thickness in mm [mils]	mΩ/square at 25°C
0.5	0.02 [0.7]	1.0
1	0.04 [1.4]	0.5
2	0.07 [2.8]	0.25



pH/mil	Dielectric thickness in mils	Inductance
32	3.1	100pH

Figure 4. The squares methods of estimating power plane resistance and inductance.

- 고밀도 컴퓨팅 전력 시스템에서 PCB 내의 PDN 임피던스는 매우 중요한 초점 영역
- 고성능 컴퓨팅 시스템에서 PDN은 Voltage-regulation 출력과 CPU 내부의 센스 지점 사이에 여러 요소로 구성
- 1000A 이상의 고 전류 프로세서를 설계할 때는 layer 수, Power 및 GND layer 할당, 구리 두께 등을 포함한 PCB stackup and floor plan을 사전에 정의하는 것이 중요

2. 시뮬레이션 통한 SPGTI 설계 :

PCB Layout and Thermal Design for High Density Modular Power Systems

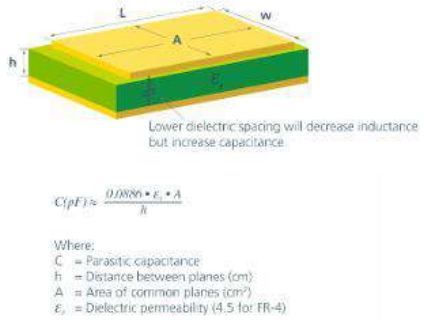


Figure 6. Parasitic capacitance in a PCB is a function of the area shared by two planes, the distance between those planes and the nominal dielectric constant of the material.

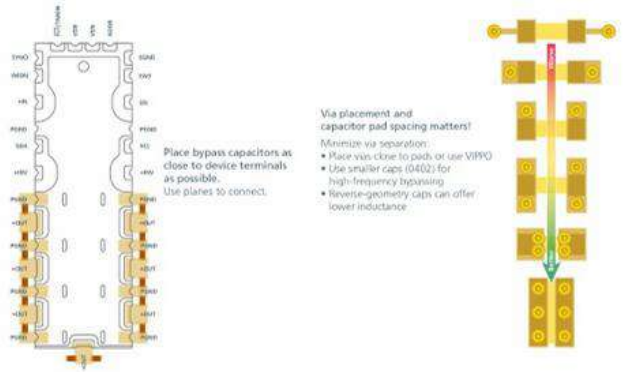


Figure 7. Capacitor selection and via placement are critical for achieving low-impedance filtering of high-frequency switching noise.

- 고밀도 전력 시스템은 고주파 Switching noise를 필터링하기 위해 신중하게 선택된 Decoupling capacitor가 필요
- 낮은 ESR 및 적절히 높은 self-resonant frequency를 갖는 capacitor가 중요하며, capacitor 값 자체보다 이러한 특성이 더 중요할 수 있음
- 낮은 ESR 및 ESL을 달성하기 위해 소형 inductor 및 역기하학적 capacitor를 고려하고, 부품 및 비아의 신중한 배치를 통해 loop inductance를 최소화해야 함

2. 시뮬레이션 통한 SPGTI 설계 :

PCB Layout and Thermal Design for High Density Modular Power Systems

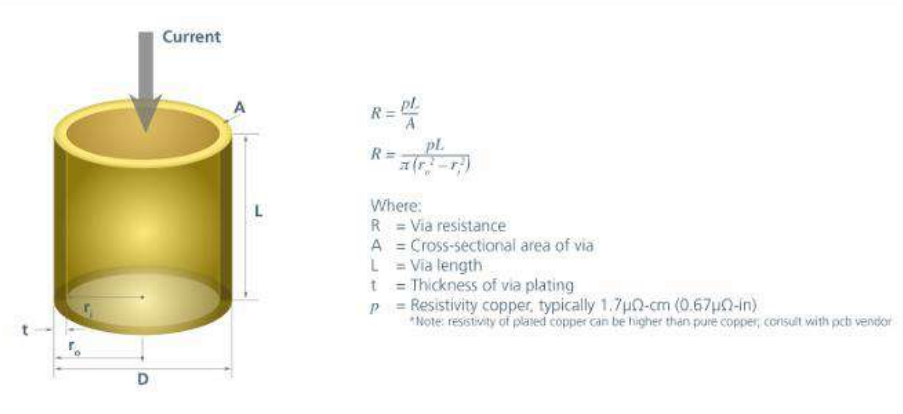


Figure 5. Via resistance can be estimated with simple geometry-based rules-of-thumb.

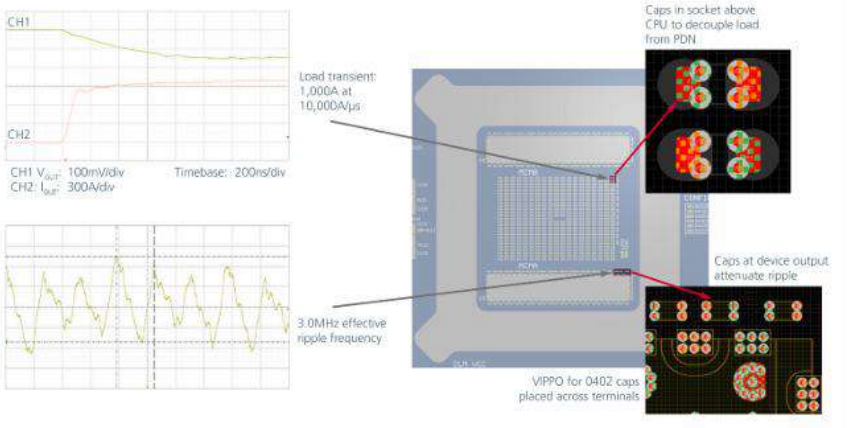
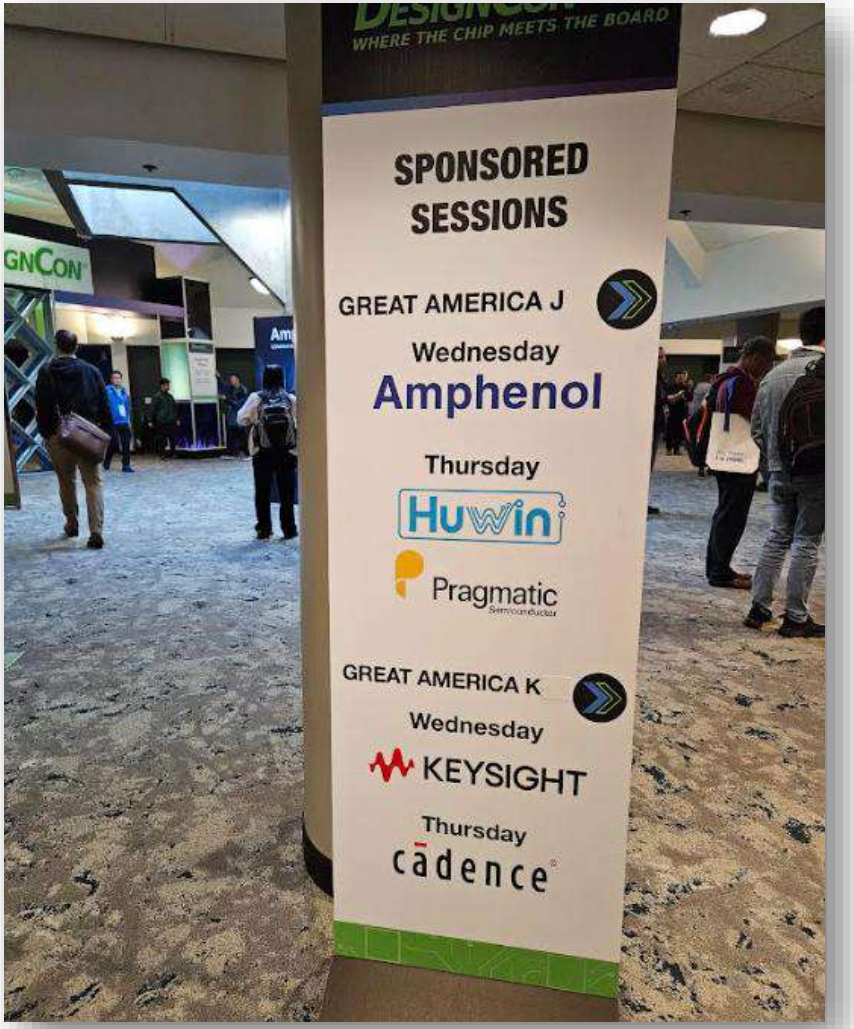


Figure 8. Appropriate capacitor selection and placement using high-performing via arrangement makes 1000A load steps at 10,000A/μs possible.

- 오늘날 advanced processors는 끊임없이 증가하는 전류 수준 및 전압 정확도 요구 사항으로 인해 고성능 컴퓨팅 및 AI용 PDN 설계는 복잡한 과제임
- 열 및 PDN 설계를 위한 최신 모델링 및 추정 기술, 고급 부품 선택 및 배치 기준이 필수적임
- 소켓 근처에 배치된 Decoupling capacitor는 ripple을 감소시키고, 다른 capacitor 는 부하를 PDN으로부터 Decoupling 함

목차

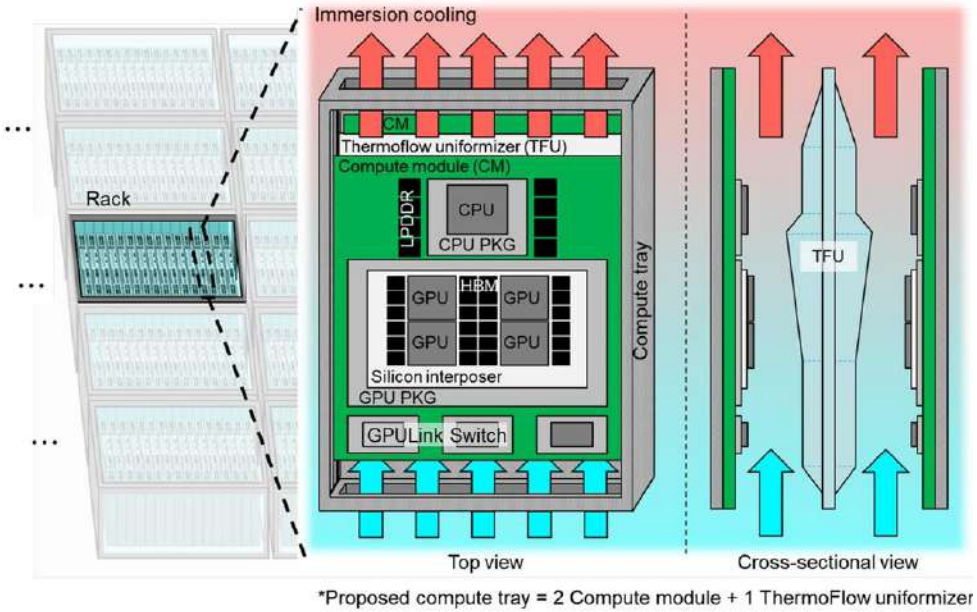


3. DesignCon 2025 자료 소개

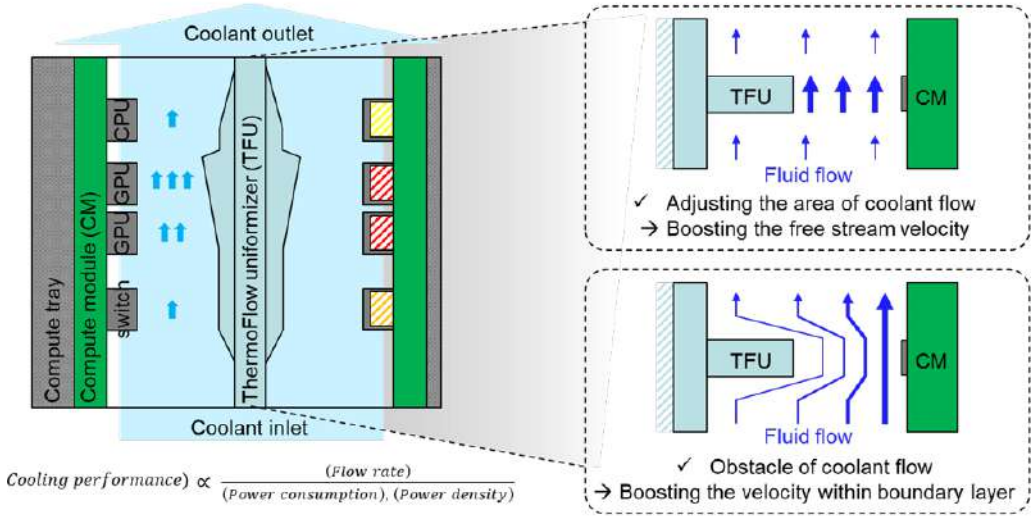
3-1 : A Novel ThermoFlow Uniformizer Applied Immersion Cooling System (TFU-ICS) for Highly-Dense Multi-GPU-HBM Based Compute Module for AI Supercomputer

❖ AI 슈퍼컴퓨터는 수천 개의 GPU로 구성되며, AI 연산량의 증가로 전력 소비 증가와 냉각 요구가 심화됨

❖ TFU(ThermoFlow Uniformizer) 구조물로 유체 유속 조절하여 냉각을 강화하고, 양면 냉각 구조와 Silicon Interposer 위에 GPU/HMB을 적층할 수 있는 고밀도 냉각구조인 TFU-ICS 제안



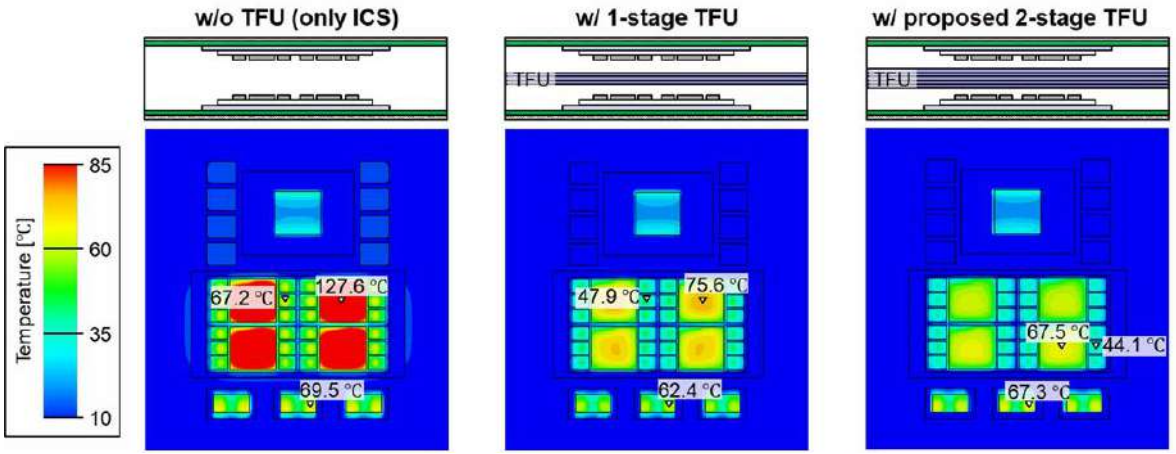
[TFU-ICS AI supercomputer 구조]



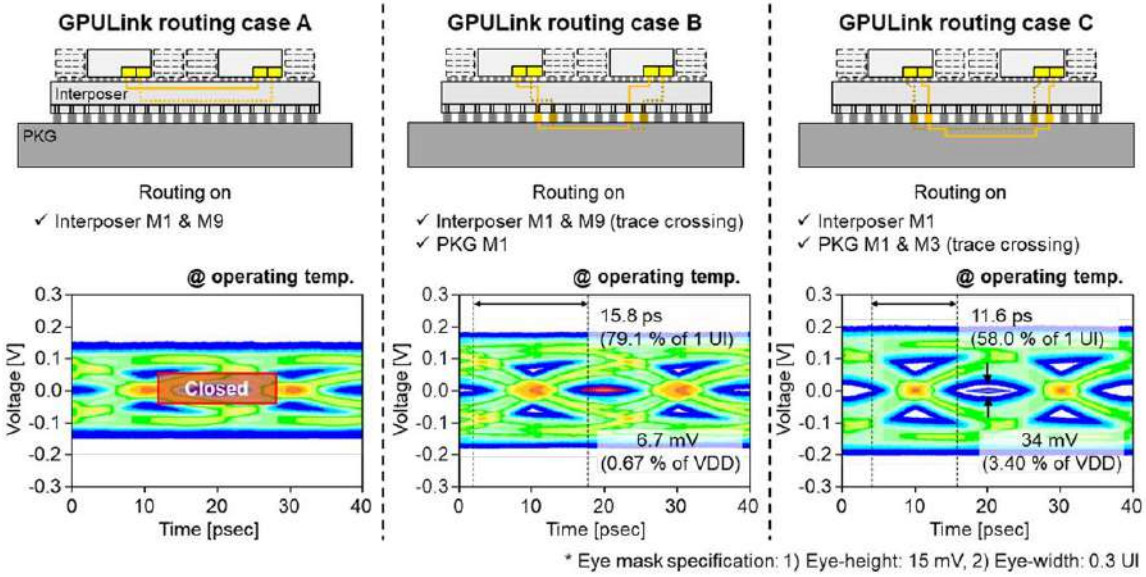
[유체 유속 제어 방법]

3. DesignCon 2025 자료 소개

3-1 : A Novel ThermoFlow Uniformizer Applied Immersion Cooling System (TFU-ICS) for Highly-Dense Multi-GPU-HBM Based Compute Module for AI Supercomputer



TFU 적용시 훨씬 낮은 열 분포 확보 가능하며, 고밀도 적층 구조에서도 안정적으로 열 저감 가능



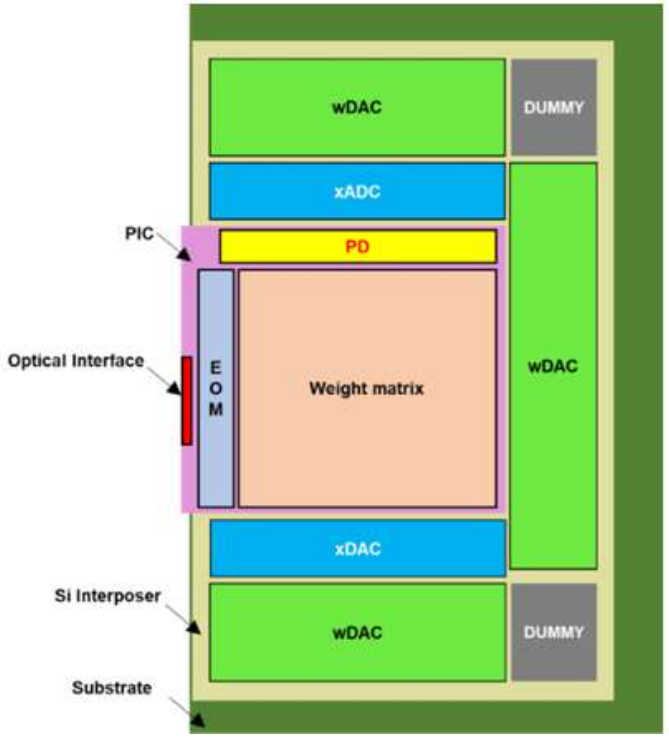
Equalization 없이도 안정적인 Eye 확보를 통해 전력 절감 가능

3. DesignCon 2025 자료 소개

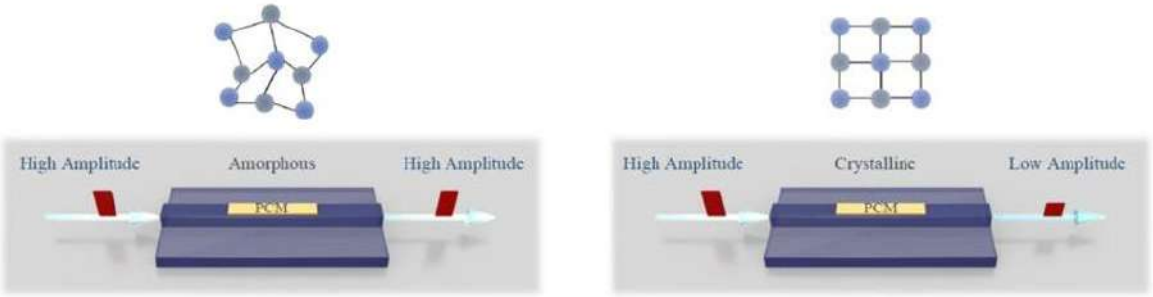
3-2 : Fast Design and Simulation of Photonic Computing Chip with Chiplet based Heterogeneous Integration

❖ AI 모델 연산량은 급증하였지만, 메모리/인터커넥트는 상대적으로 정체되어 병목 현상이 발생함

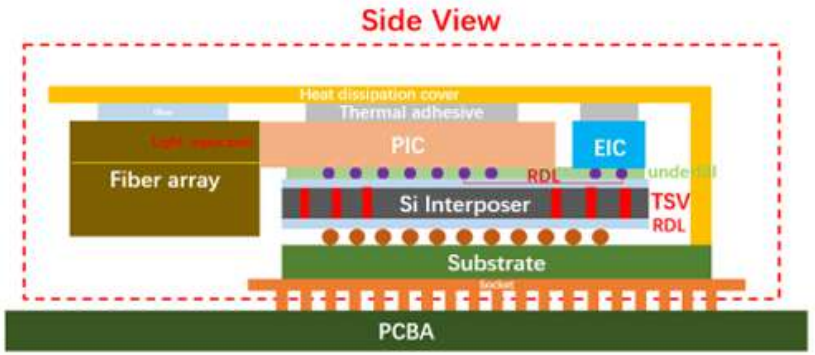
❖ 광 기반 연산 + 칩렛 구조를 활용해 고속, 저전력, 고집적 컴퓨팅 칩을 실현할수있는 Photonics + 2.5D Heterogeneous Integration 구조로 구현하고 이를 위한 시뮬레이션 방법론을 제안함



[아키텍처 시스템 구성도]



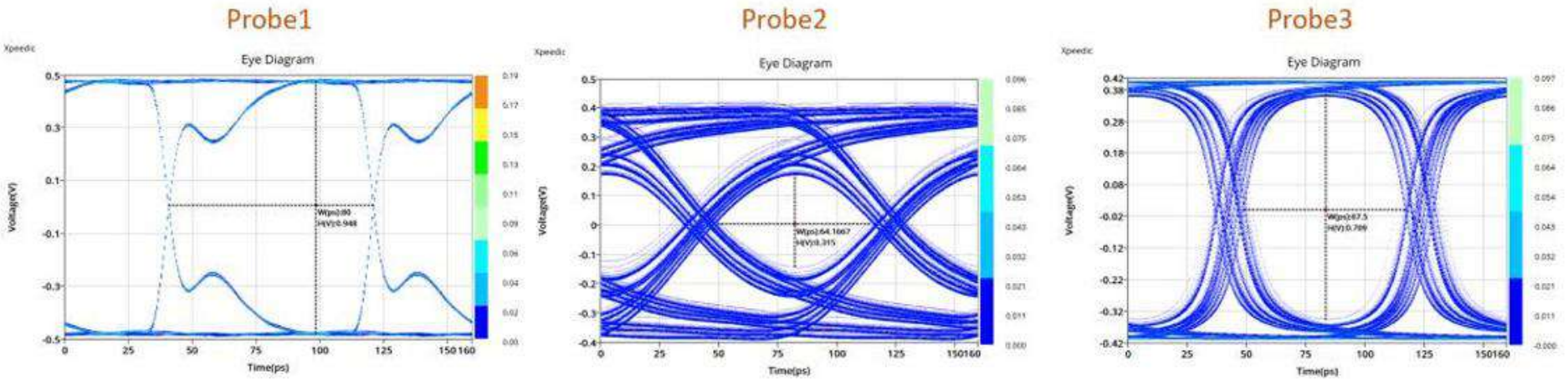
[아키텍처 시스템 구성도]



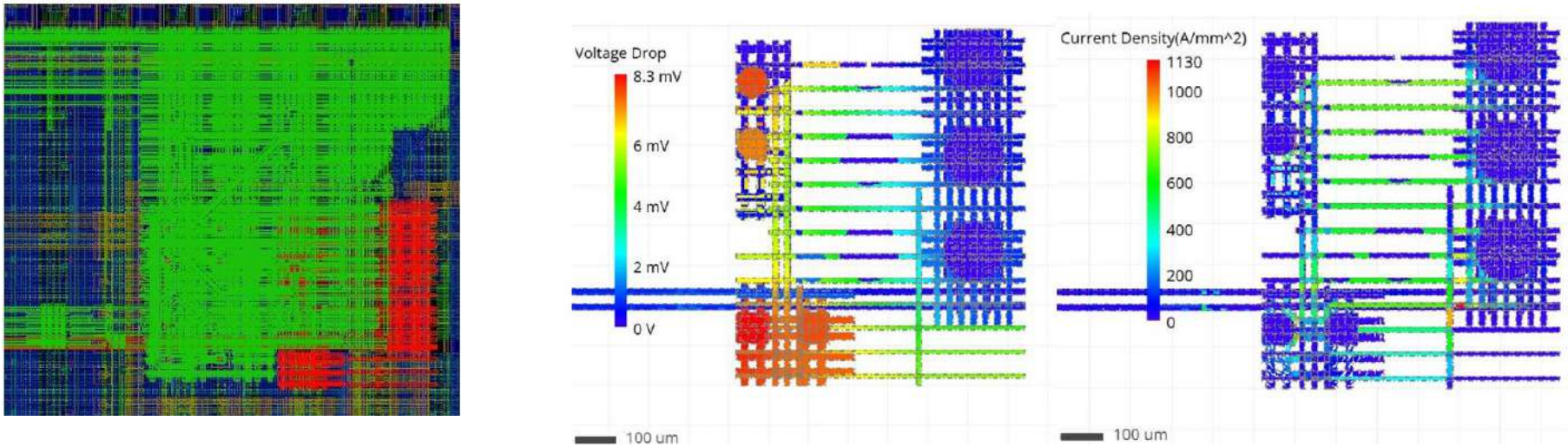
[아키텍처 시스템 구성도]

3. DesignCon 2025 자료 소개

3-2 : Fast Design and Simulation of Photonic Computing Chip with Chiplet based Heterogeneous Integration



[12.5Gbps serdes simulation topology and result]

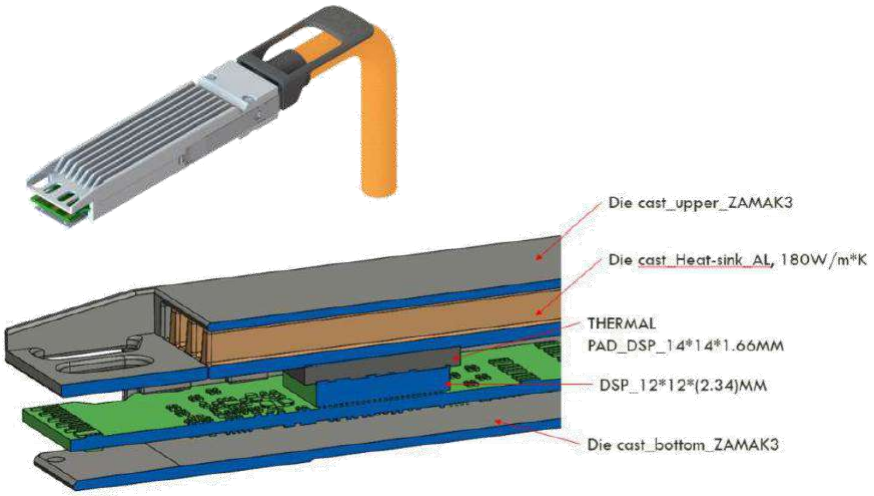


[0.9V Power region and PI-DC simulation result]

3. DesignCon 2025 자료 소개

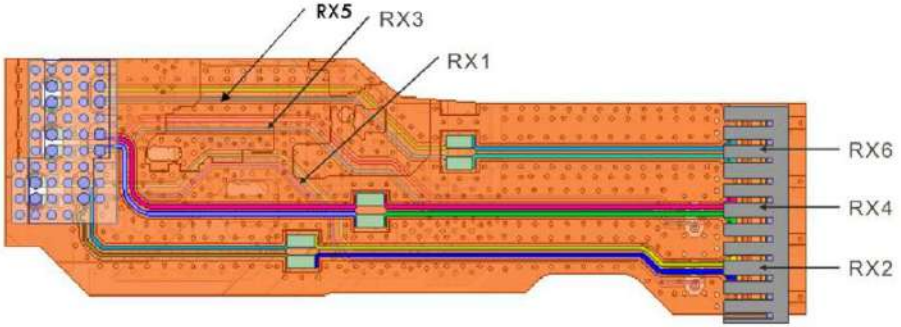
3-3 : Chip-On-Board & Modified-SAP Design for the 100G PAM4 & Beyond Active Cable & Optical Transceivers

- 800G 데이터 전송을 위해 최소한의 시간 지연과 전력 소비 특성을 갖는 케이블링 기술이 필요함
- Package와 interposer가 필요 없도록 die를 사용하여 우수한 SI 특성을 확보하고 히트 싱크를 직접 die에 적용하여 방열 문제를 완화함

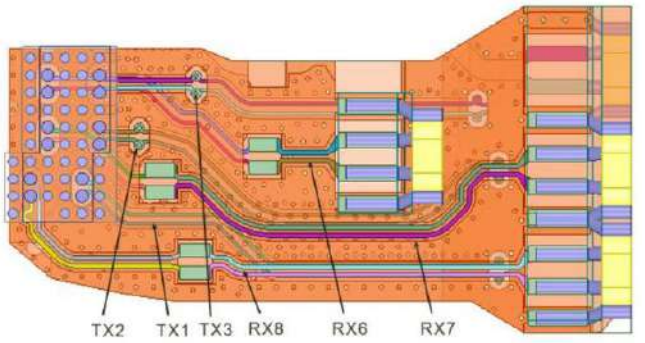


Item	Material	Power/ Thermal conductivity
U2(DC-DC)	Silicon	0.8W
U3(DC-DC)	Silicon	0.03W
U4(DC-DC)	Silicon	0.02W
U13(DC-DC)	Silicon	0.02W
U14(DC-DC)	Silicon	0.01W
U8(DSP)	Silicon	9.7W
U5(MCU)	Silicon	0.5W
Thermal Paste	Prolimatech PK-3	Thermal conductivity 11.2W/(m.k)
HOUSING BASE	ZAMAK3	Thermal conductivity 113.3W/(m.k)
HOUSING COVER	ZAMAK3	Thermal conductivity 113.3W/(m.k)

Host side: RX1-RX6 PCB: Megtron7, Dk:3.3, Df:0.0015@1GHz



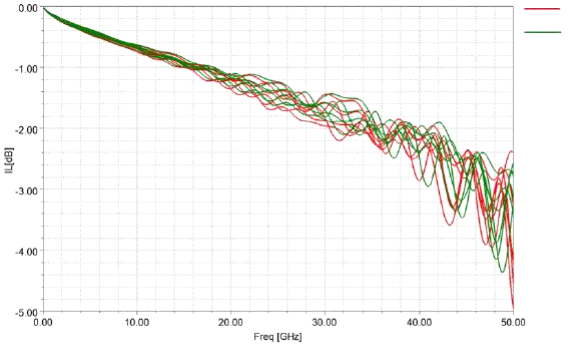
Line Side: TX1-TX3; RX6-RX8



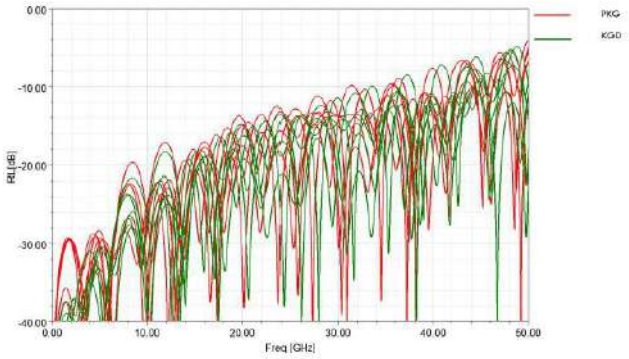
3. DesignCon 2025 자료 소개

3-3 : Chip-On-Board & Modified-SAP Design for the 100G PAM4 & Beyond Active Cable & Optical Transceivers

Simulation KGD vs PKG(Host Side)



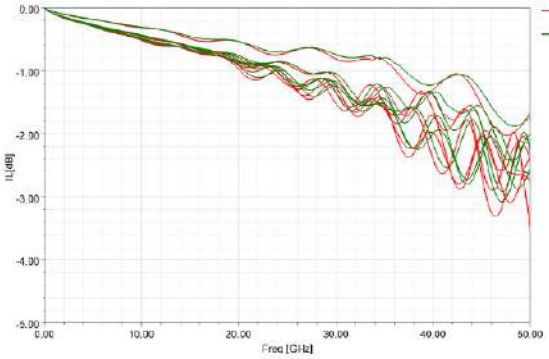
KGD IL vs PKG IL



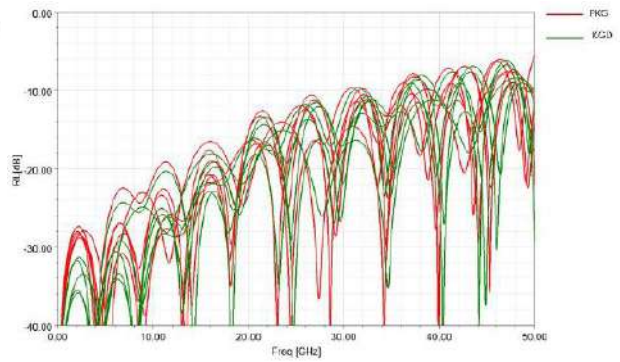
KGD RL vs PKG RL

112G Paddle Card with KGD(Known Good Die) vs PKG

Simulation KGD vs PKG(Line Side)

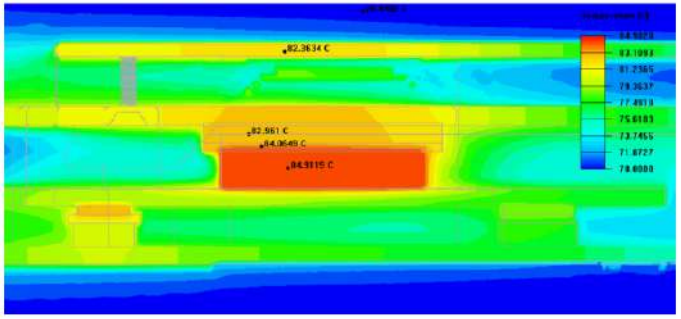


KGD IL vs PKG IL



KGD RL vs PKG RL

With thermal paste and copper plate: Tdsp=84.9℃



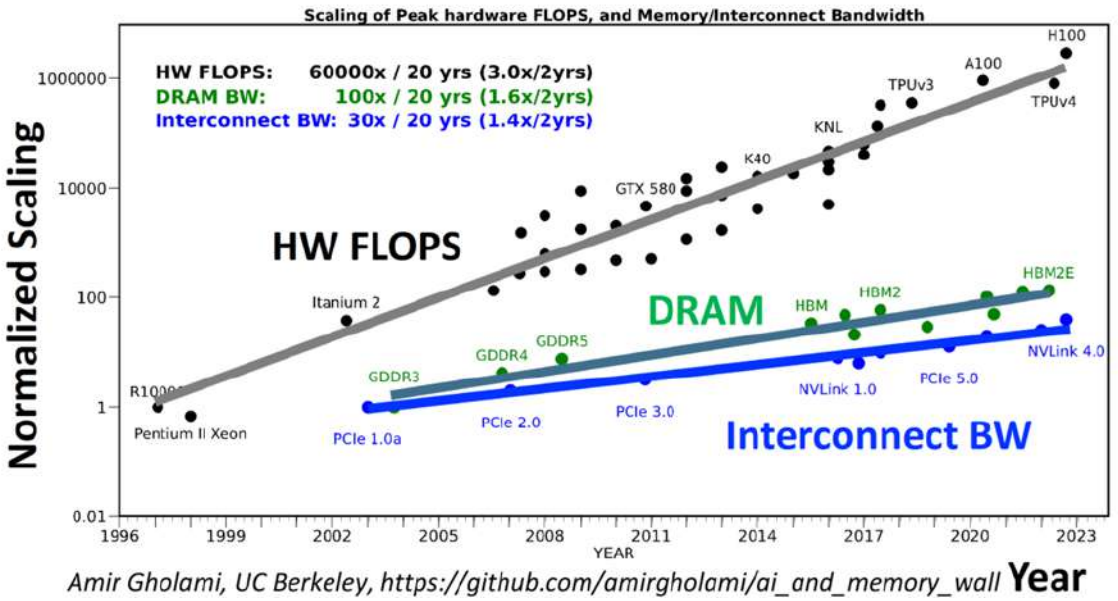
Thermal Dissipation Simulation with Thermal Paste and Copper Plate

3. DesignCon 2025 자료 소개

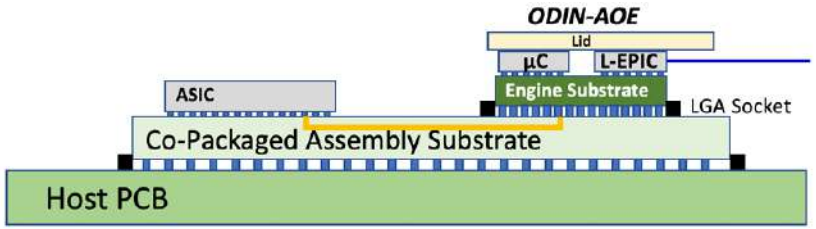
3-4 : Development of a co-packaged Application Specific IC with direct drive optical engine chiplets

❖ AI HW 연산능력(FLOPS)은 향상되고있으나, 메모리 및 인터커넷트 대역폭은 속도를 따라가지 못해서 시스템 아키텍처 전환이 필요함

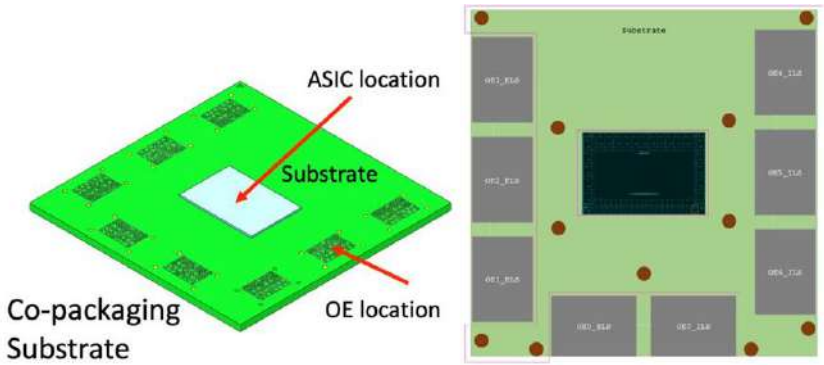
❖ ASIC과 광엔진을 하나의 substrate 위에 Co-packaging하여 SI, Power Efficiency, Latency를 개선하고, AI용 고대역 인터커넥트 구조 실현



[Interconnect bandwidth vs Compute HW FLOPS]



[Typical Optial Enging Copacking Application]

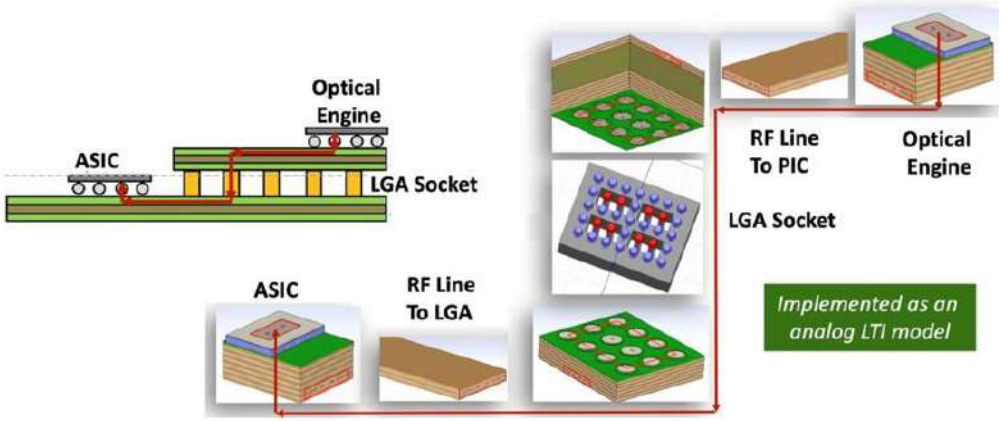


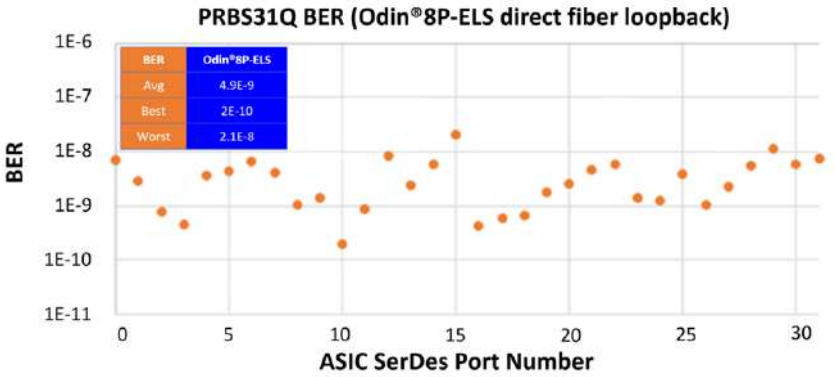
[CPO substrate with 8x OEs]

3. DesignCon 2025 자료 소개

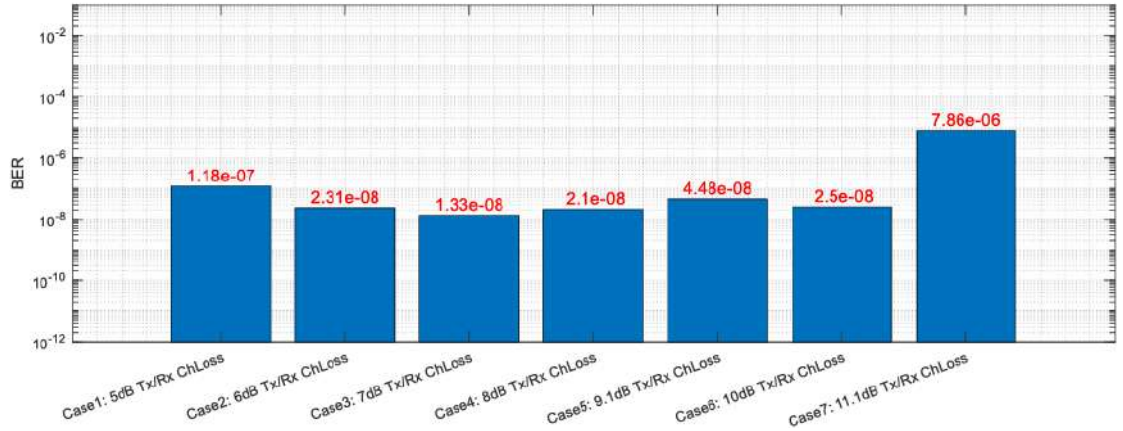
3-4 : Development of a co-packaged Application Specific IC with direct drive optical engine chiplets

❖ Full link simulation을 통해 Retimer 없이도 112G PAM4 전송이 안정적임





[BER Test 결과]



[BER for different electrical channel loss]

	800G Pluggable Module with 5nm DSP Retimer		Odin®8P-ILS Version (this paper)		Odin®8P-ELS Version (this paper)	
Function	Consumption [W]	Efficiency [pJ/bit]	Consumption [W]	Efficiency [pJ/bit]	Consumption [W]	Efficiency [pJ/bit]
Optical Engine			3.6	4.5	2.25	2.81
ELSFP Laser					0.875	1.09
OE + Laser Total					3.125	3.9
Overall	14	17.5	3.6	4.5	3.125	3.9

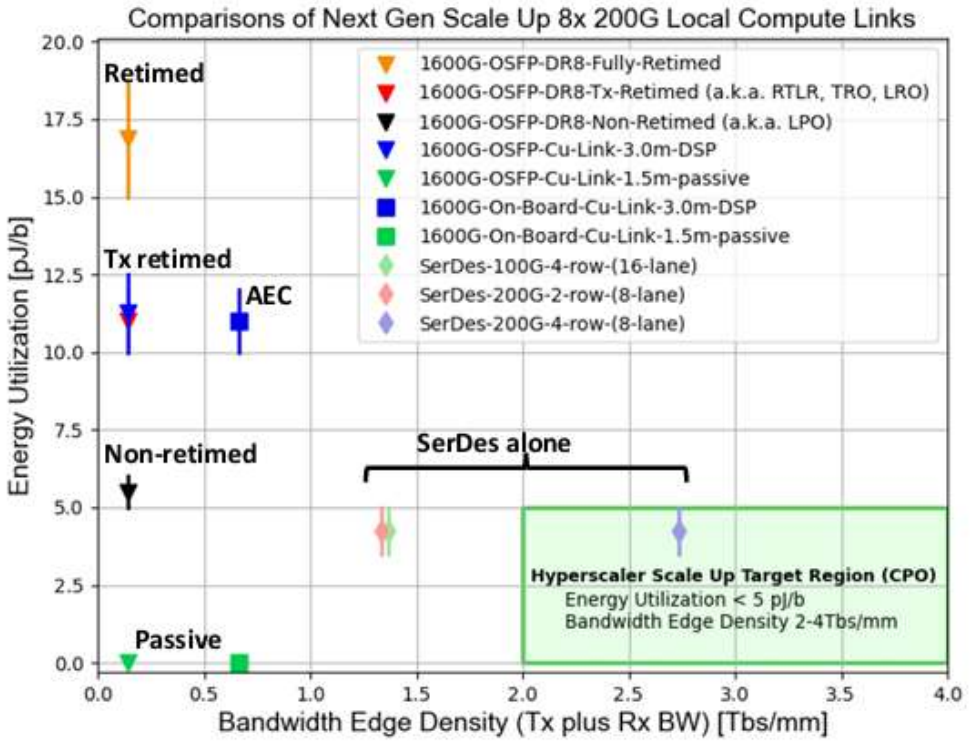
[Power Efficiency Comparison]

3-4 : Development of a co-packaged Application Specific IC with direct drive optical engine chiplets

❖ 200G급 전송 시., SerDes 직결 구조가 가장 에너지 효율적

❖ UCIe (Slow-Wide I/F)는 ASIC 면적 절약에는 유리하나, 지연증가

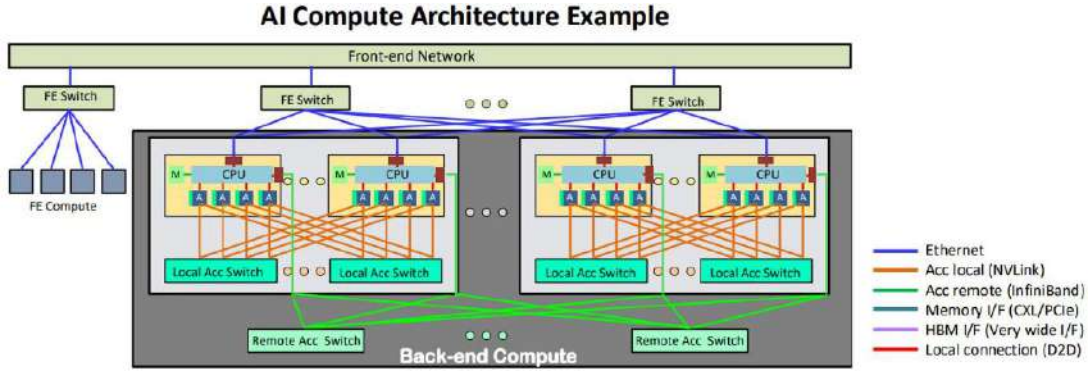
[200G Electrical Interface comparsion]



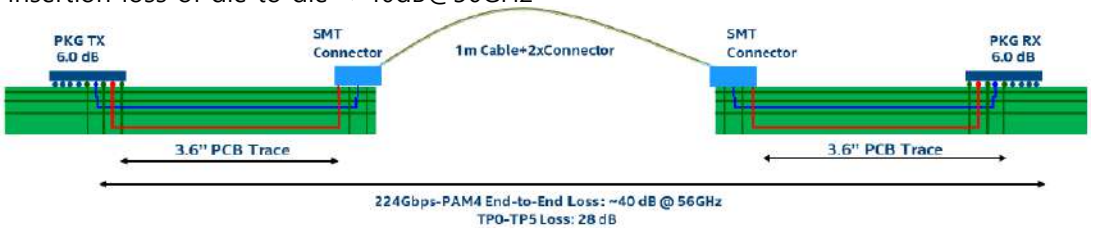
3. DesignCon 2025 자료 소개

3-5 : Modeling and Parameter Extraction of 224G PCB Under Variable Temperature and Research on The Influence of Temperature on SI

- ❖ 최근 급속한 데이터 속도의 발전으로 시스템의 전력 소비가 높아지고 PCB 온도가 점점 높아짐
- ❖ 온도가 높아짐에 따라 PCB 유전율과 손실이 크게 변하며, 이는 전송선로의 임피던스와 손실을 변화시켜 시스템 마진이 감소함

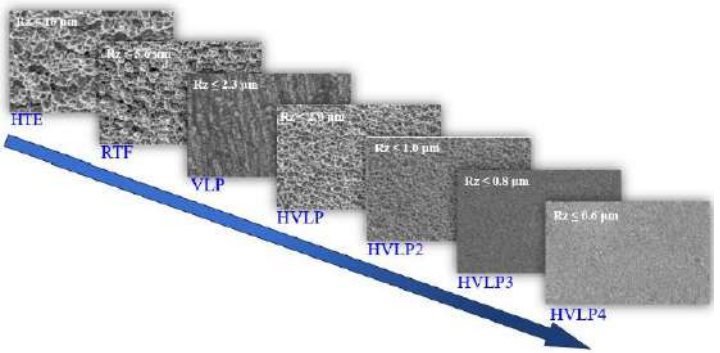


Insertion loss of die to die < 40dB@56GHz

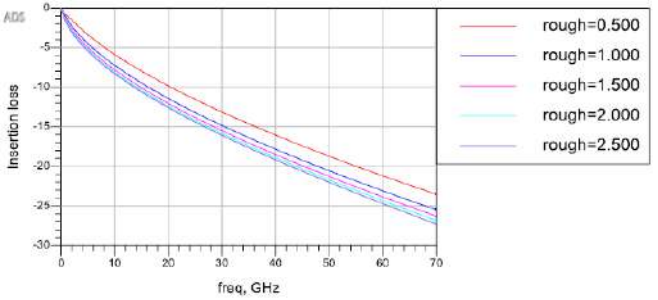


Thermal plate를 이용한 PCB 온도에 따른 영향 측정 환경

Copper foil에 따른 roughness



Copper foil roughness에 따른 insertion loss

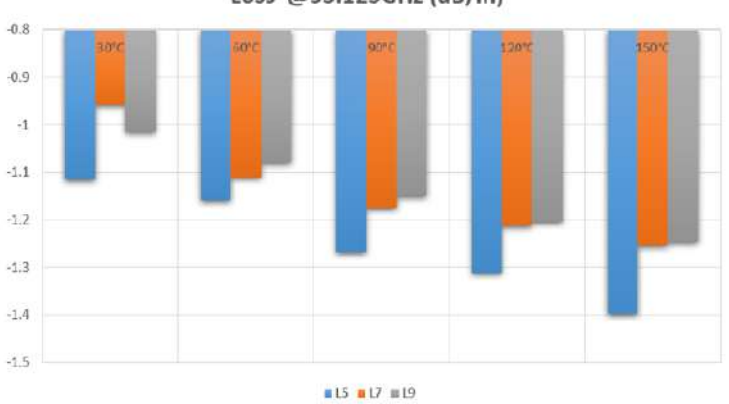


3-5 : Modeling and Parameter Extraction of 224G PCB Under Variable Temperature and Research on The Influence of Temperature on SI

❖ 각 온도의 insertion loss와 phase 측정결과를 이용하여 Dk, Df를 추출함

➢ Megtron9, HVLP4 copper foil, special brown oxide treatment

온도에 따른 각 레이어의 Insertion loss

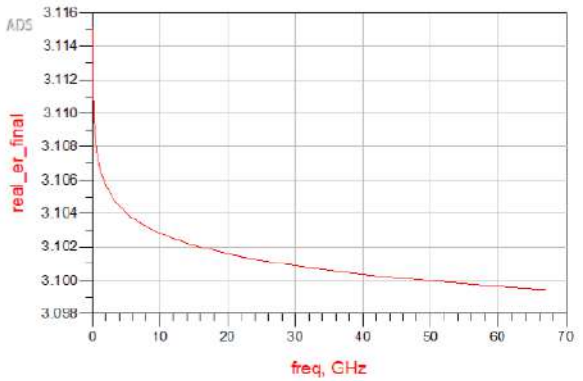


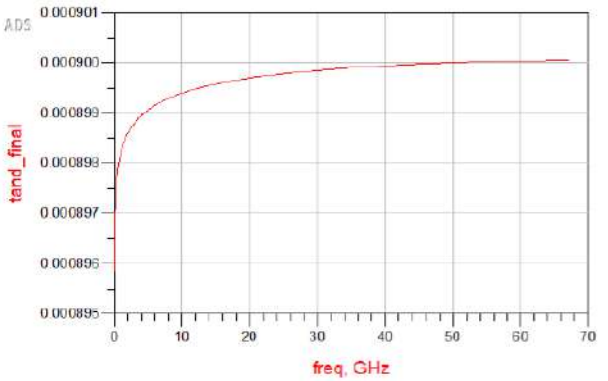
IL (dB/in)	30°C	60°C	90°C	120°C	150°C
L5	-1.116	-1.159	-1.268	-1.311	-1.397
L7	-0.957	-1.11	-1.174	-1.213	-1.254
L9	-1.014	-1.08	-1.149	-1.204	-1.246

온도에 따른 각 레이어의 Skew

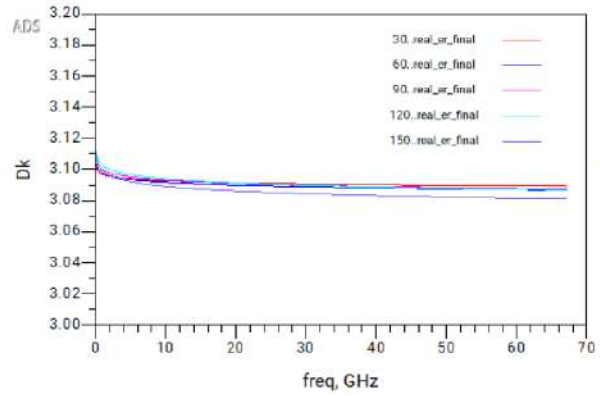
Skew(ps)	30°C	60°C	90°C	120°C	150°C
Layer5	0.4348	0.2628	0.5247	0.5229	0.5112
Layer7	-0.1615	0.2699	0.2745	0.2962	0.2802
Layer9	-0.1566	0.7947	0.7883	0.7871	0.7566

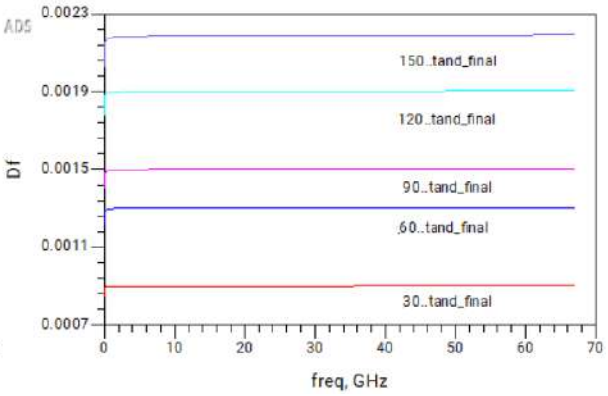
같은 온도에서 주파수에 따른 Dk, Df 변화





30~150℃에서의 Dk, Df 특성





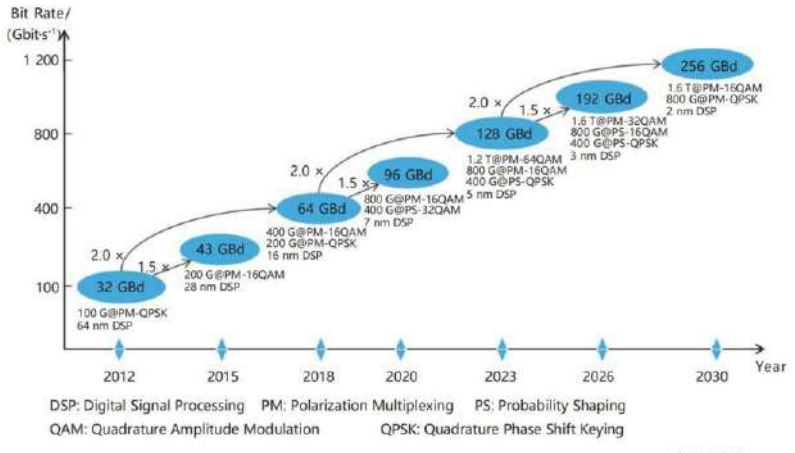
3. DesignCon 2025 자료 소개

3-6 : Study of TDR impedance and loss based on modified Cannonball huray roughness model on a 1.6Tbps optical module PCB

고속 전송선로에서의 TDR 기반 임피던스 분석

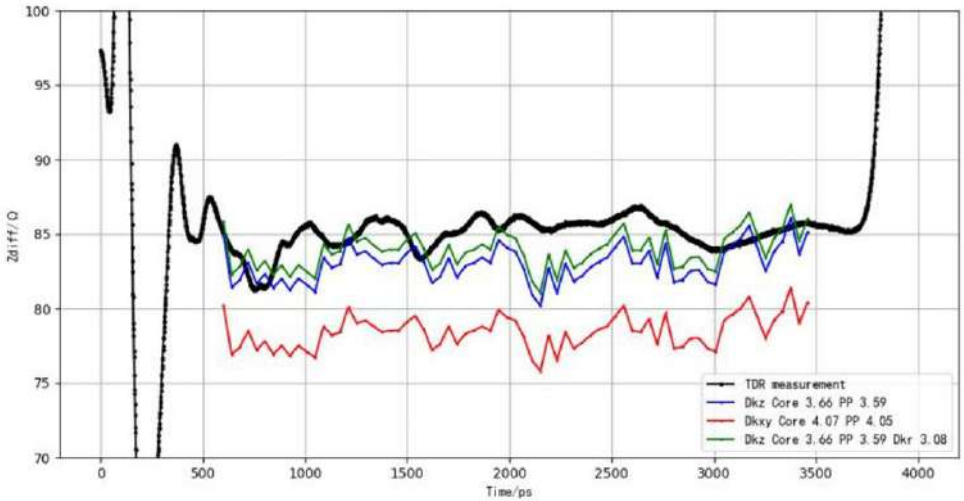
- 1.6T 광모듈 시대, DSP > Optical 경로에서 130 Gbaud/s 이상 필요
  - 3dB Bandwidth > 70~100 GHz 신호 무결성 확보 중요

- 고주파 전송선 모델링
  - TDR 기반 분석을 통해 실제 임피던스 측정 및 시뮬레이션 비교
  >> Dk는 임피던스 오차에 민감 -> Dkz 반영
  - Djordjevic-Sarkar(D-S) 모델 사용
  >>단일 주파수점으로 전체 대역 예측 가능

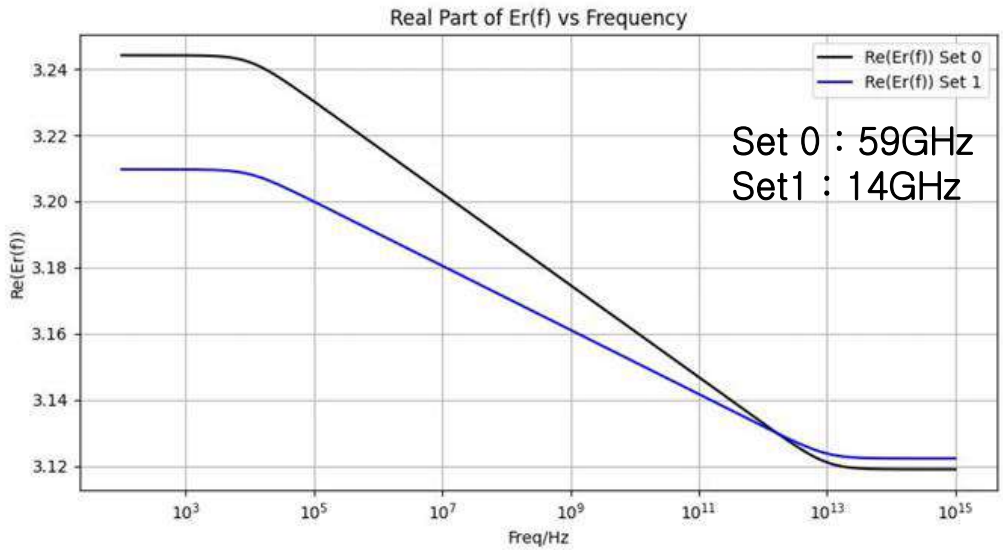


[ZTE.2023]

[Evolution process of DAC/ADC Signal Baud Rate]



[The impedance test curve of a stripline]



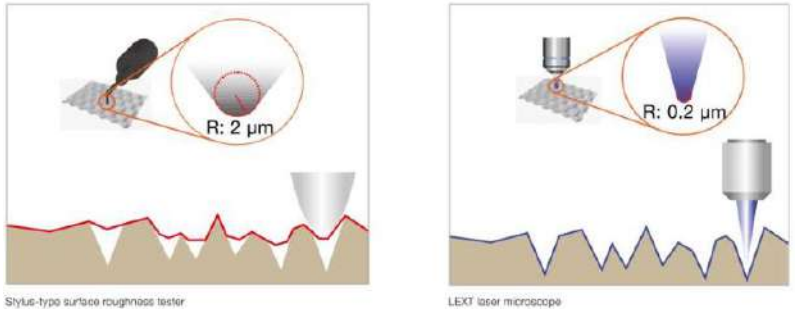
[Simulated D-S models]

3. DesignCon 2025 자료 소개

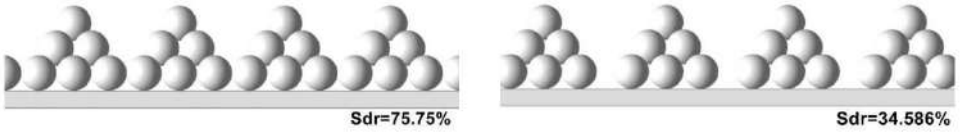
3-6 : Study of TDR impedance and loss based on modified Cannonball huray roughness model on a 1.6Tbps optical module PCB

거칠기 모델 : Cannonball-Huray 개선

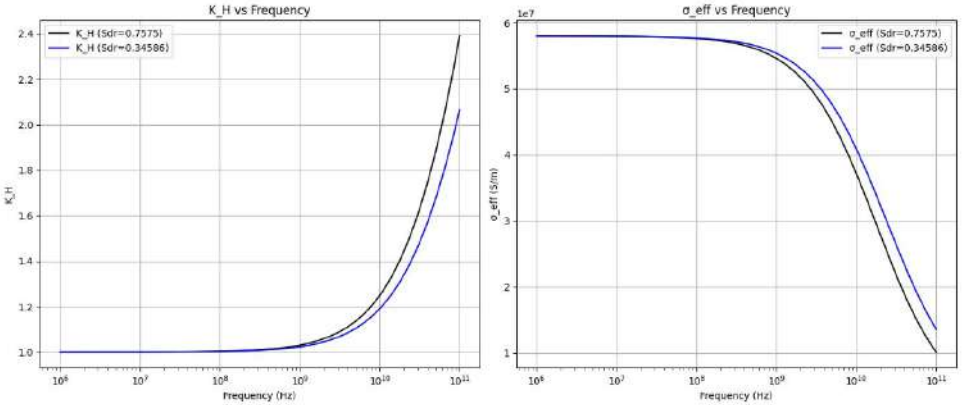
- 전도 손실의 주원인은 표면거칠기(Rz,Sdr)에 의존
- 접촉식 거칠기 측정(Rz)값만으로 도체 손실 예측하기가 어려움
  - Sdr (Developed Interfacial Area Ratio) 측정으로 정밀 반영 가능
- Sdr 기반 보정으로 손실 예측도 증가



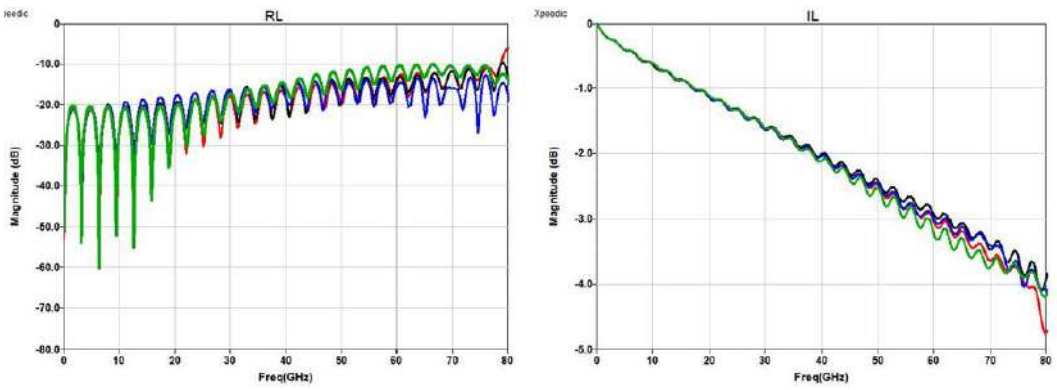
[Contact and non-contact measurements of the roughness Rz parameter]



→ Sdr이 높을수록 표면 거칠기가 증가



[Cannonball model at different Sdr values]



[Surface morphology (magnification factor of 5000X)]

3-7 : The Influence of Copper Crystal Structure on Signal Integrity

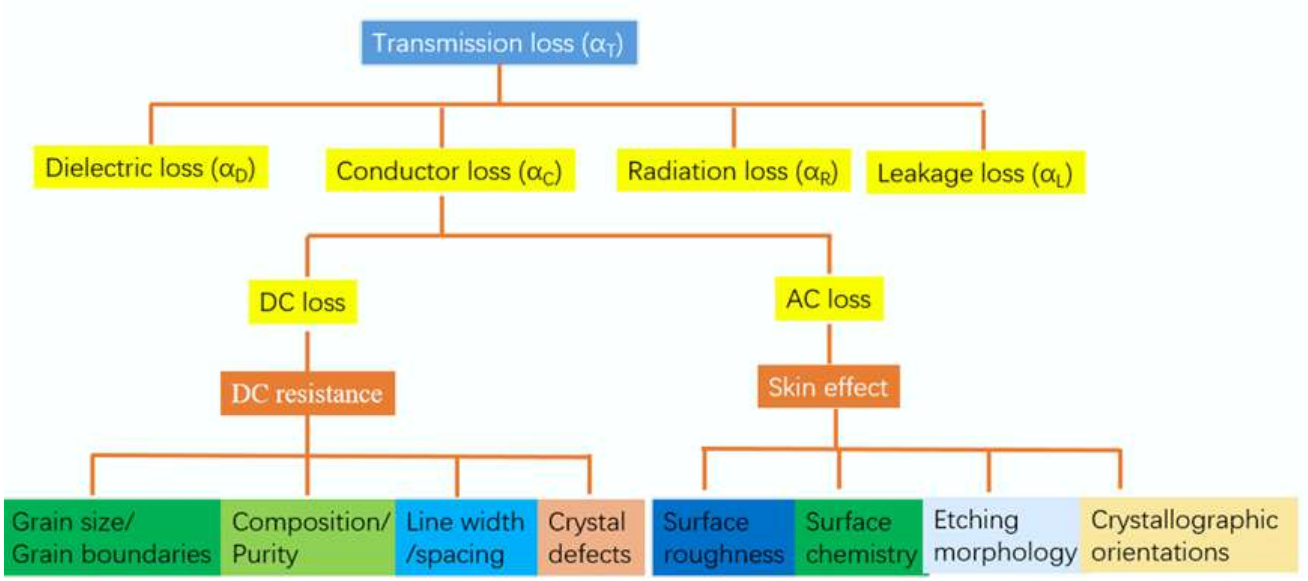
PCB transmission loss

- Total transmssion loss를 줄이기 위해서는 Conductor loss를 줄여야함

- Conductor loss 에는 DC loss와 AC loss로 나뉨
  - DC Loss : 구리 전체 단면적에 따른 손실
  - AC Loss : Skin effect로 인한 손실

$\alpha_T=\alpha_D + \alpha_C + \alpha_R + \alpha_L$

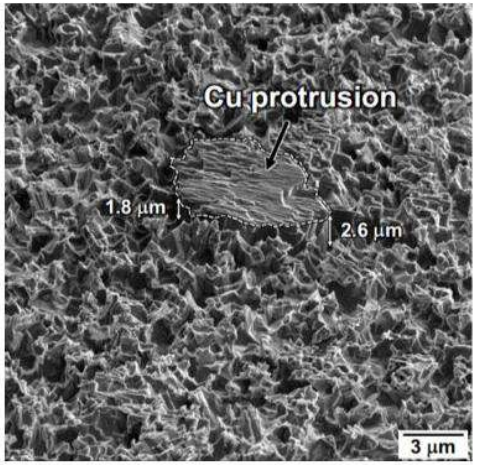
α_T:Transmission loss
α_D: dielectric loss ,
α_C: conductor loss ,
α_R: radiation loss ,
α_L: and leakage loss



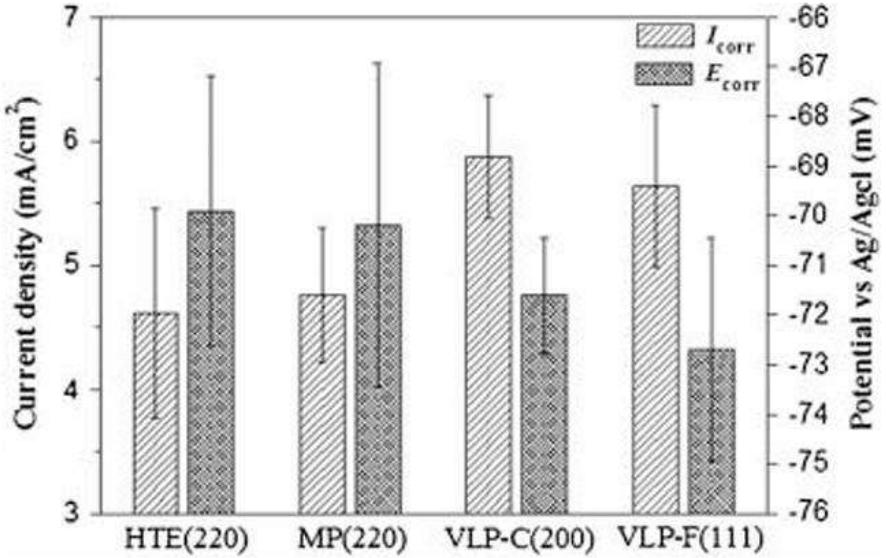
3-7 : The Influence of Copper Crystal Structure on Signal Integrity

결정 구조와 부식 형상

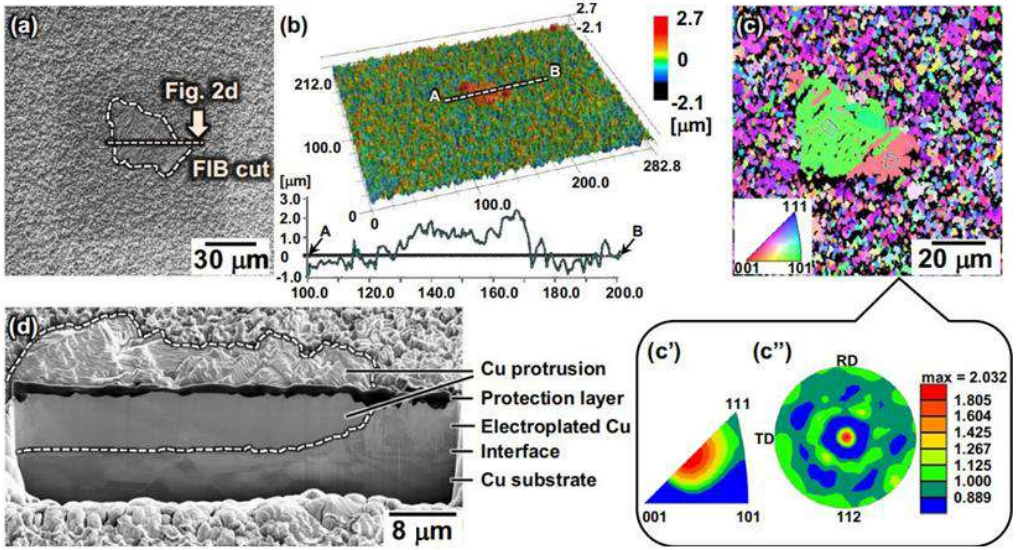
- 구리의 결정방향에 따라 부식속도와 부식 형상이 달라짐
- Etching은 결정 구조에 따라 다르게 진행됨



Effect of crystal structure on etching morphology of copper



Corros. Sci. **2013**, *74*, 223-231.

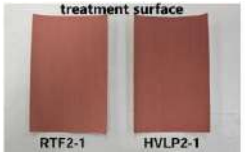


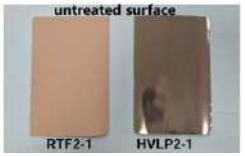
Surf. Coat. Technol. **2020**, *386*, 125471

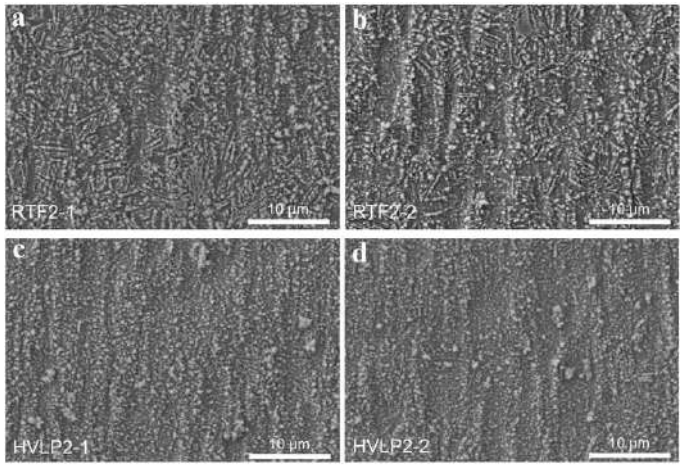
3-7 : The Influence of Copper Crystal Structure on Signal Integrity

결정 구조 및 표면 형상 분석

- SEM 및 거칠기(Sdr, Rz) 분석 결과, Annealing 전후로 거칠기 변화가 없음
  - 결정구조가 변화하더라도 표면 거칠기의 변화는 미미함 -> AC 손실 영향 적음
- 결정 구조 변화에 의한 Insertion Loss 영향은 0-50 GHz에서 제한적
- 50-100 GHz 이상 고주파 대역에서 영향이 커질 가능성이 높음

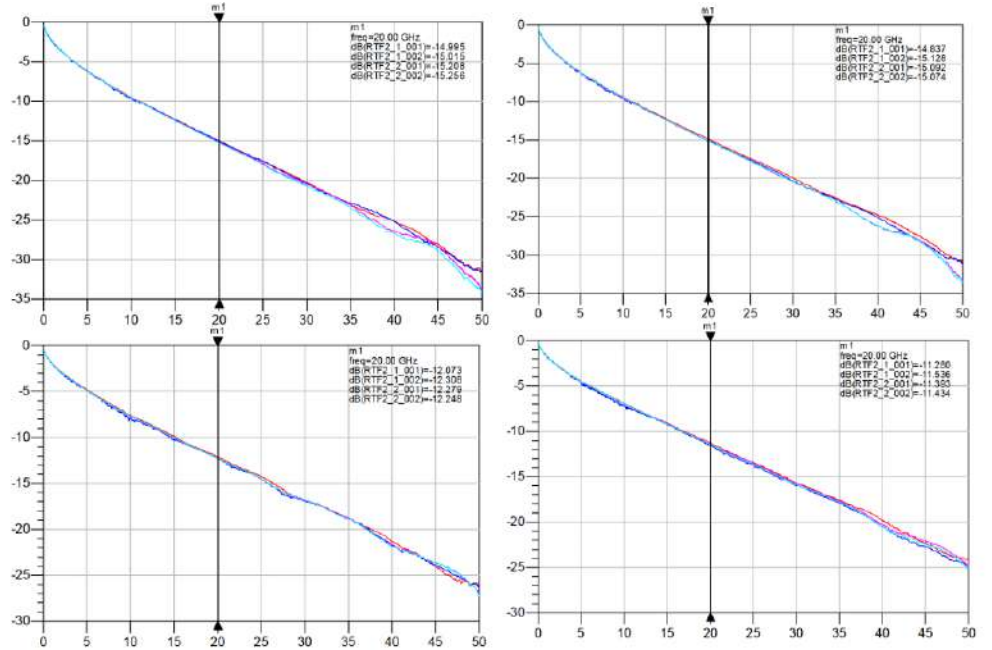






Surface morphologies of the samples of copper foils by SEM observations at 0° .

Copper foil	RTF2-1	RTF2-2	HVLP2-1	HVLP2-2
Sdr (%)	11.476	10.981	10.945	11.358
Rz (μm)	1.924	1.877	1.890	1.899

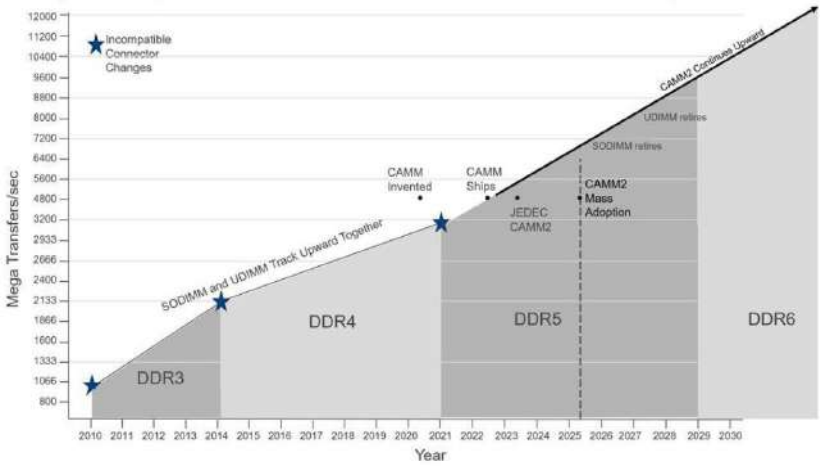


Insertion Losses of RTF2 - 1 and RTF2 - 2 at a Frequency of 50 GHz with a Line Length of 16 Inches. The Line Widths and Spacings Are (a) 4.2/6.8, (b) 4.6/13.4, (c) 5.7/5.3, and (d) 7.2/10.8 mil Respectively.

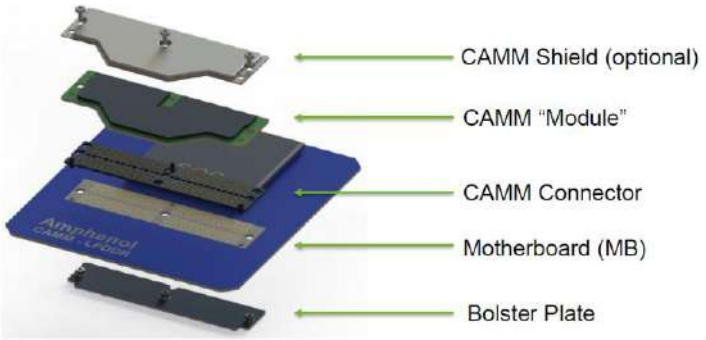
3. DesignCon 2025 자료 소개

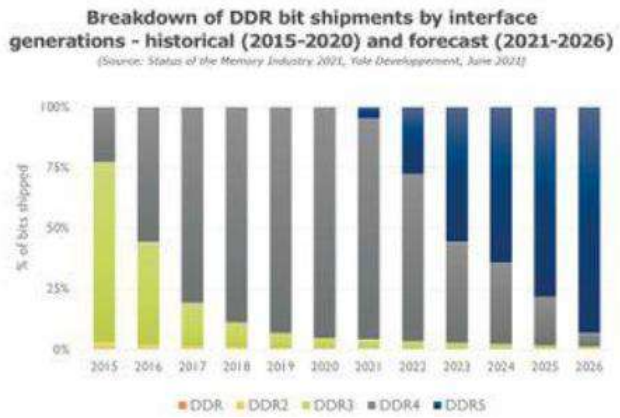
3-8 : CAMM: The New Standard for Memory

❖ 오랫동안 DIMM을 사용했으나 2023년도 JEDEC은 LGA(Land Grid Array) 방식의 CAMM2를 발표함
❖ 분리 가능하여 재사용이 가능하고 각 핀은 하우징 캐비티 내부에 보호됨



CAMM Interface



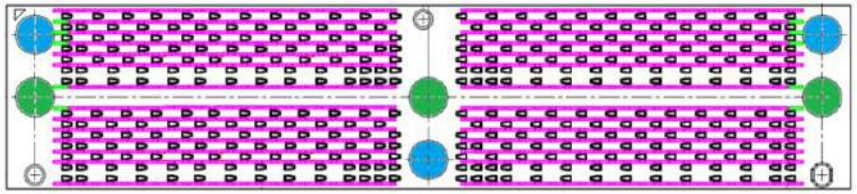


DIMM Interface

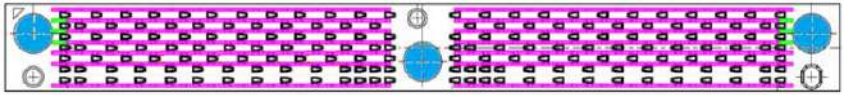
3-8 : CAMM: The New Standard for Memory

❖ JEDEC Standardization

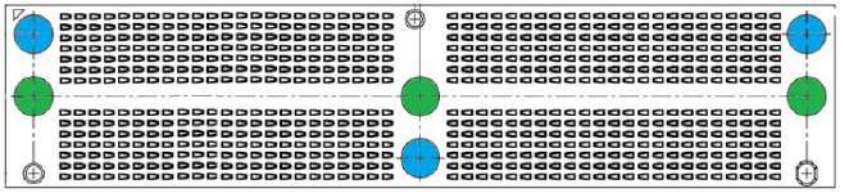
➢ DC CAMMs
- Ground shields(PINK)
- Mounting holes for DDR5(BLUE)
- Mounting holes for LPDDR5(GREEN)



➢ SC CAMMs
- Ground shields(PINK)
- Mounting holes for DDR5(BLUE)



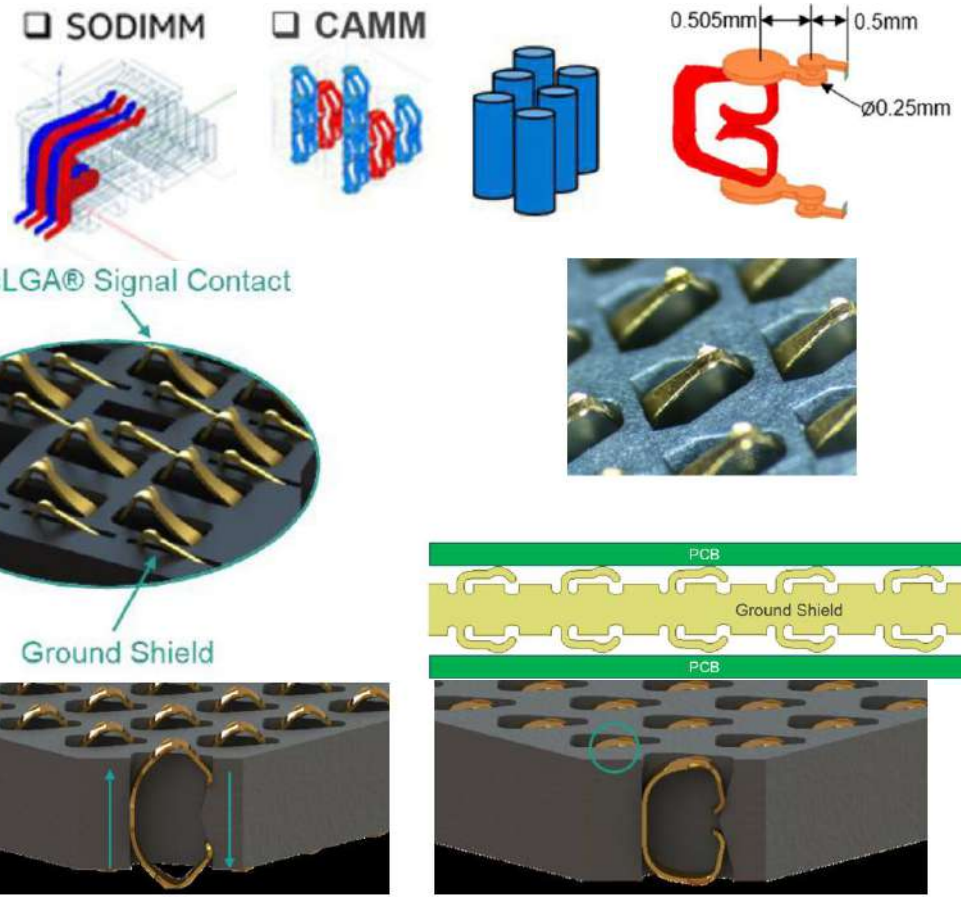
➢ LPCAMM
- Ground pins instead of shields
- Mounting holes for DDR5(BLUE)
- Mounting holes for LPDDR5(GREEN)



❖ cLGA 장점

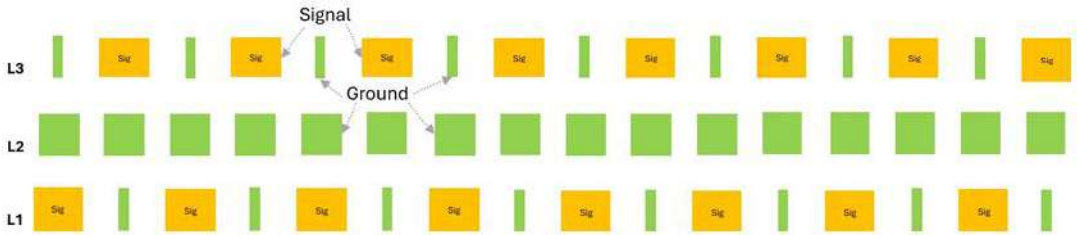
➢ 핀이 하우징 내부에 있어 손상될 가능성이 적음

➢ 수직으로 움직여서 PCB 평탄도 편차 영향이 없음



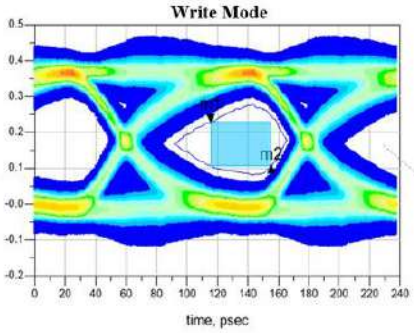
3-9 : Innovative Interposer Solutions for HBM3/4: A path to 12.8Gbps

- AI/ML 컴퓨팅 증가로, 고대역폭 메모리(HBM)의 속도 및 I/O 수 증가 (HBM3->HBM4)
- 기존 Si interposer 방식은 Cross talk 및 IL 저하로 고속 전송에 제약

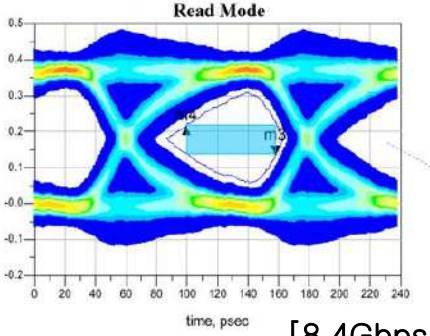


L1/L2/L3 레이어 기반 GSG 구조

[기존 Si 인터포저 구조]



S.NO	Parameters	Write Mode	formula
a	Si-Interposer	Conventional	
b	Speed (Gbps)	8.4	
c	1 UI (ps)	119.05	
d	PHY Tx Jitter (PSIJ, RJ, DCD) (ps)	17.67	
e	**Simulated EYE width in ADS (ps)**	**40.00**	
f	Interposer induced jitter (ps)	79.05	c - e
g	JEDEC min EYE spec (ps)	35.71	
h	Total margin available(ps)	-13.38	c - d - f - g



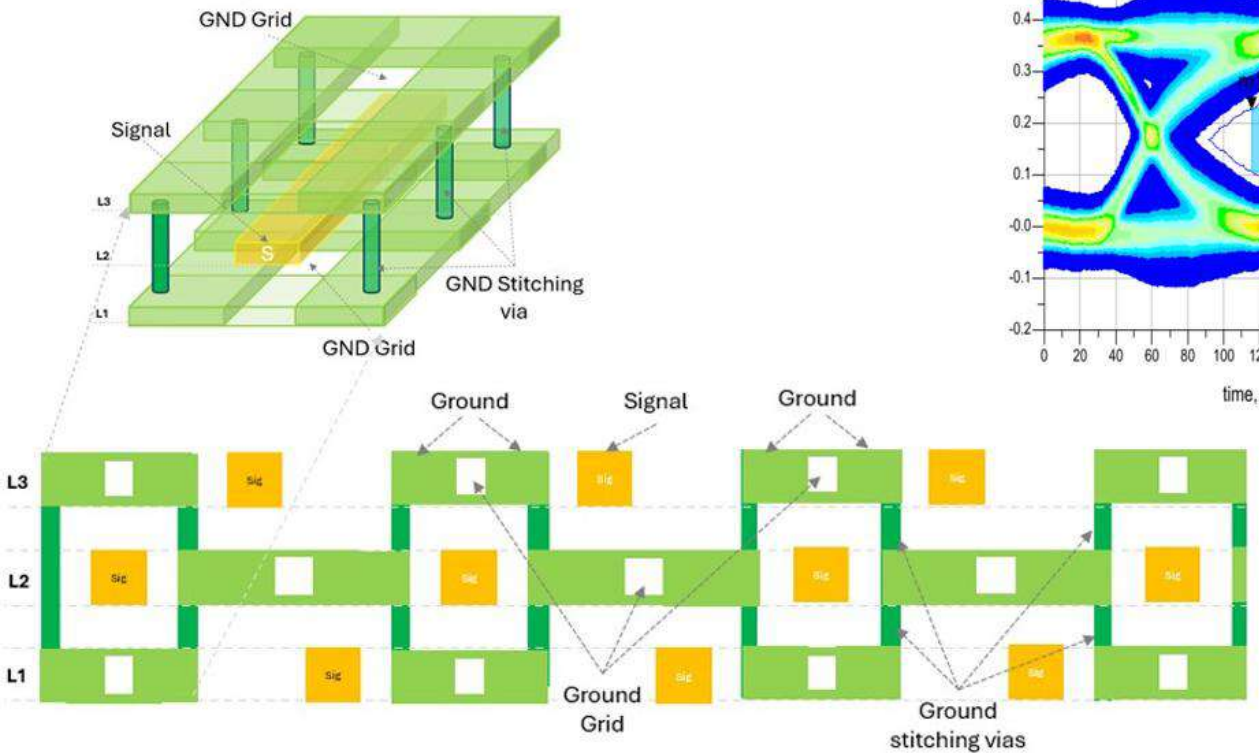
S.NO	Parameters	Read Mode	
a	Si-Interposer	Conventional	
b	Speed (Gbps)	8.4	
c	1 UI (ps)	119.05	
d	Rx Path Jitter (PSIJ, RJ, DCD) (ps)	56.93	
e	**Simulated EYE width in ADS (ps)**	**58.93**	
f	Interposer induced jitter (ps)	60.12	c - e
g	Min EYE (internal) spec (ps)	11.00	
h	Total margin available(ps)	-9.00	c - d - f - g

기준 마스크 미달 -> 채널 성능 부족

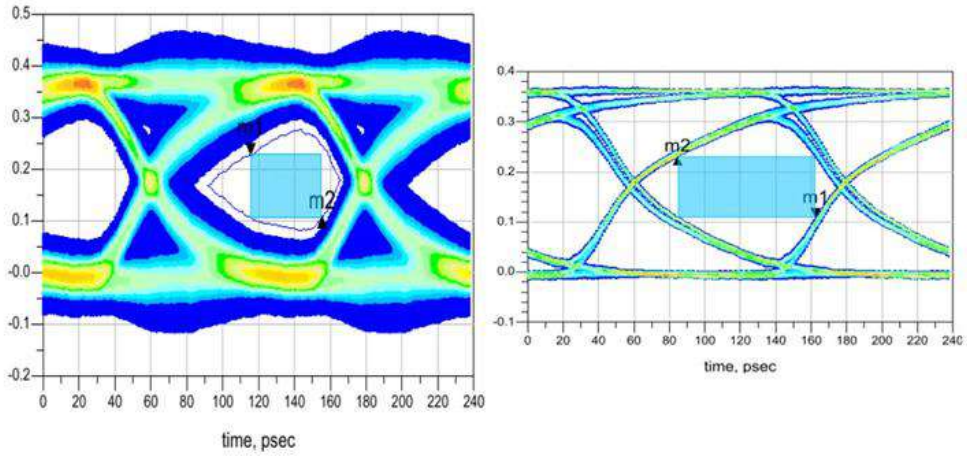
[8.4Gbps Conventional layout EYE]

3-9 : Innovative Interposer Solutions for HBM3/4: A path to 12.8Gbps

- Novel Crosstalk Shielding 구조 제안 (수직/수평 GND + stitching via)
- VTF(Voltage Transfer Function) 기반 채널 특성 지표 사용 – IL, PSXT, ICR
- ISI, Crosstalk, Rise-Fall degradation으로 Jitter 분해 -> EYE closure 원인 분석



[제안하는 Novel Shielding 구조도]



[Conventional vs Novel Eye 비교]

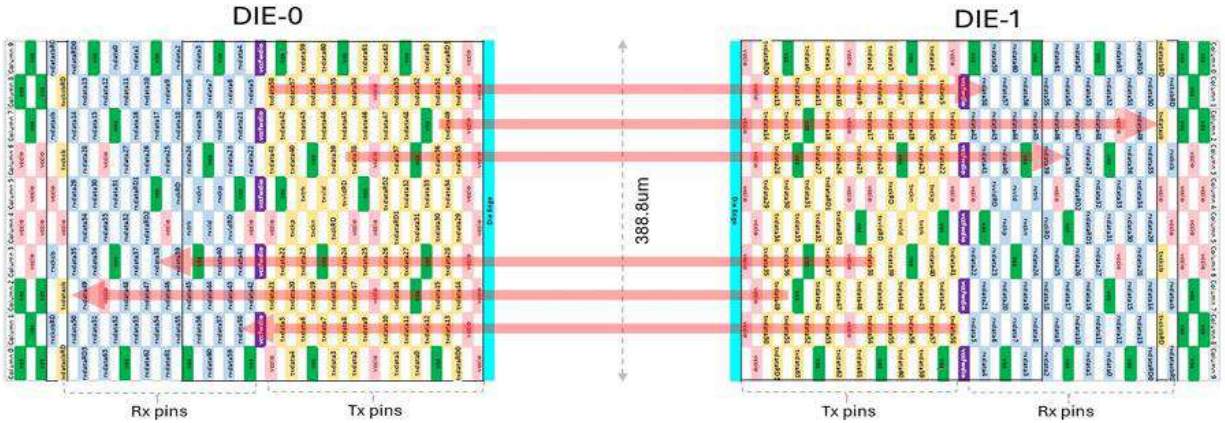
3. DesignCon 2025 자료 소개

3-10 : Innovative Layout Optimization Methodology and Via Routing Pattern to Enable UCIe 36Gbps in Organic Interposer (1/3)

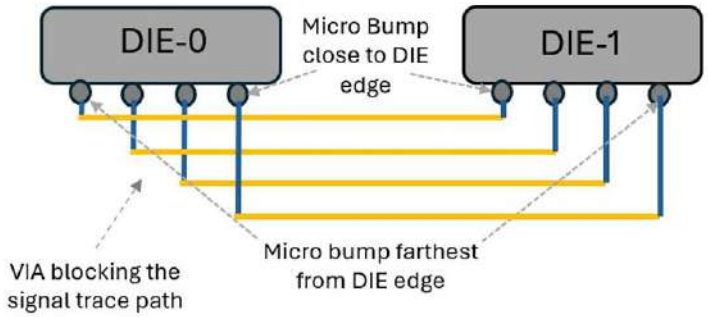
GSG 구조 최적화와 크로스토크 저감

- Organic Interposer는 Via 크기 및 trace 폭/간격으로 인해 GSG 라우팅 패턴 적용이 어려움
- 마이크로 범프 필드 내 Via 충돌로 인해 신호 거리 증가하고 Cross talk 및 UCI 규격 미달 발생

→ 2D+3D EM기반 하이브리드 SI-PI 최적화 방법론 제안



[GSG Routing 및 UCIe x64 마이크로 범프 구성]

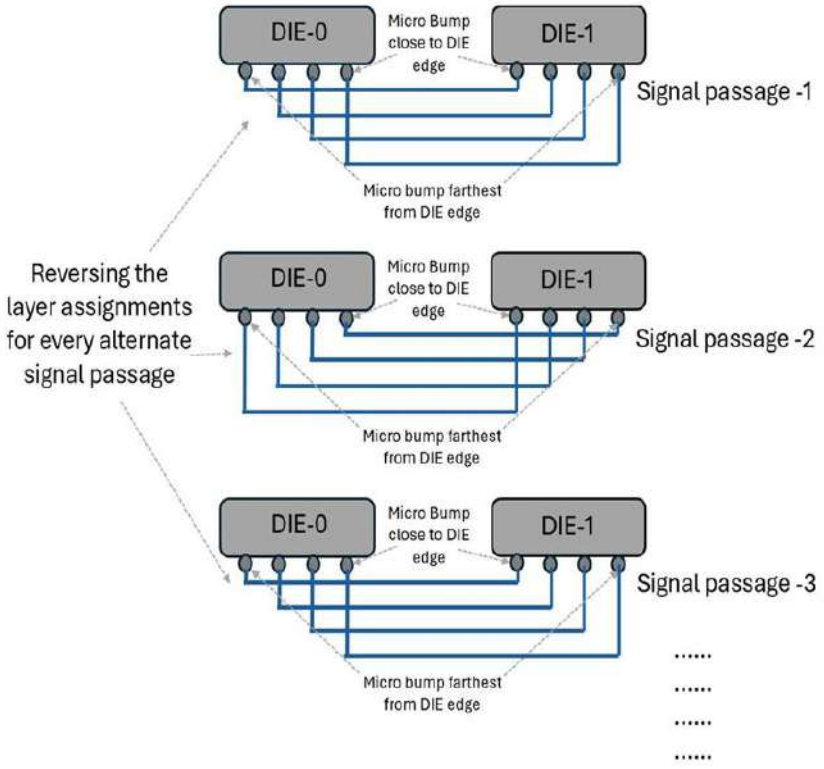


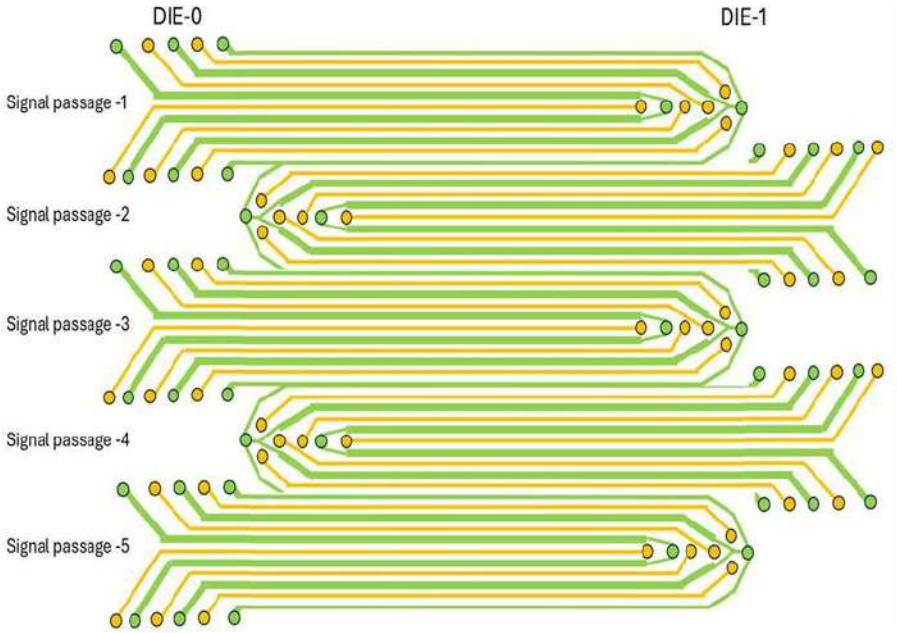
[Innovative Via fanout and routing pattern]

3-10 : Innovative Layout Optimization Methodology and Via Routing Pattern to Enable UCIe 36Gbps in Organic Interposer (2/3)

Via Fanout & Routing 패턴 설계

- Via들을 마이크로 범프 사이에 배치하여 신호 통로(Signal Passage) 확보
- GSG 라우팅이 가능한 신호 통로 구성
- RX/TX 신호를 레이어 분리하여 간섭 최소화



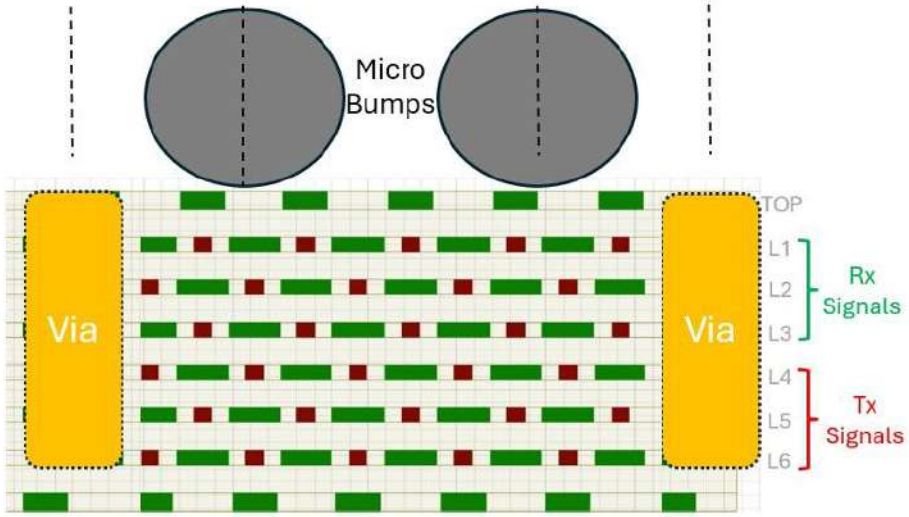


3. DesignCon 2025 자료 소개

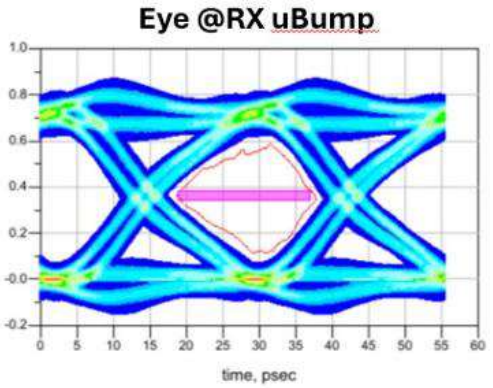
3-10 : Innovative Layout Optimization Methodology and Via Routing Pattern to Enable UCIe 36Gbps in Organic Interposer (3/3)

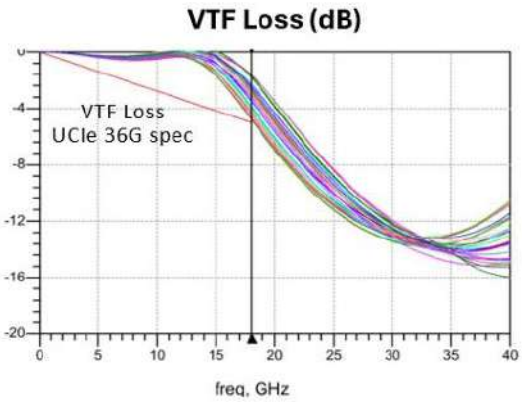
Via Fanout & Routing 패턴 설계

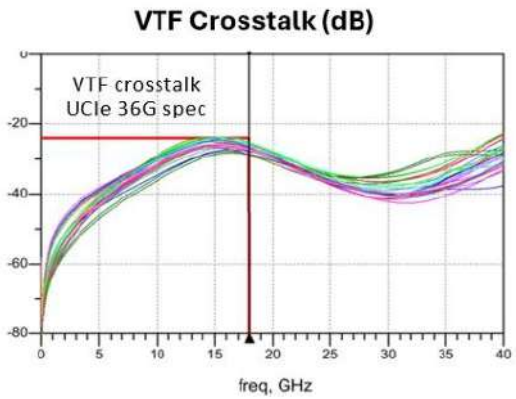
- Via들을 마이크로 범프 사이에 배치하여 신호 통로(Signal Passage) 확보
- GSG 라우팅이 가능한 신호 통로 구성
- RX/TX 신호를 레이어 분리하여 간섭 최소화



[Cross-sectional view of GSG inside micro bump field]







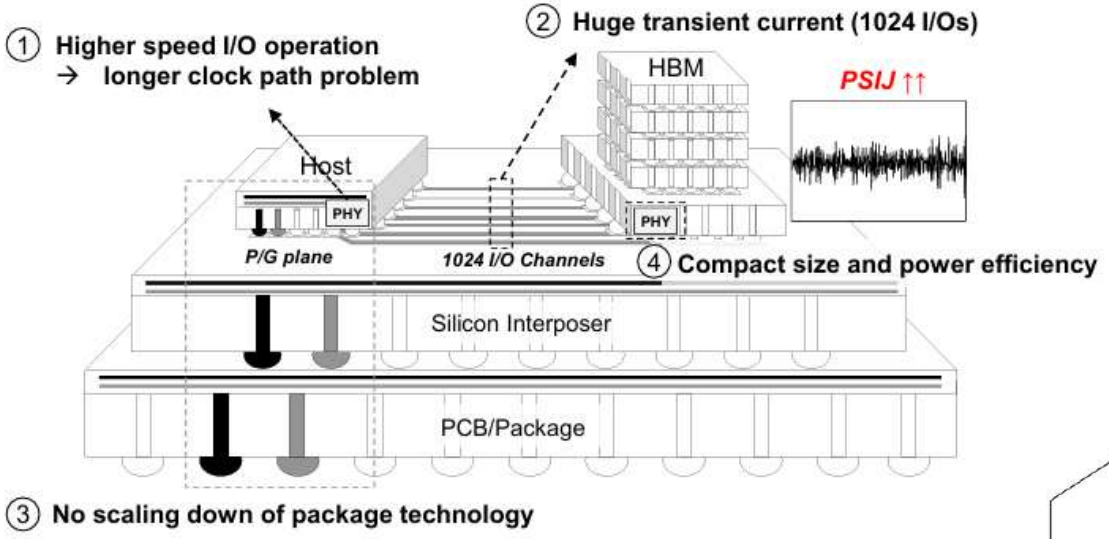
→ UCIe 36G 기준 만족
→ VTF Crosstalk : -40dB 이하 유지

3. DesignCon 2025 자료 소개

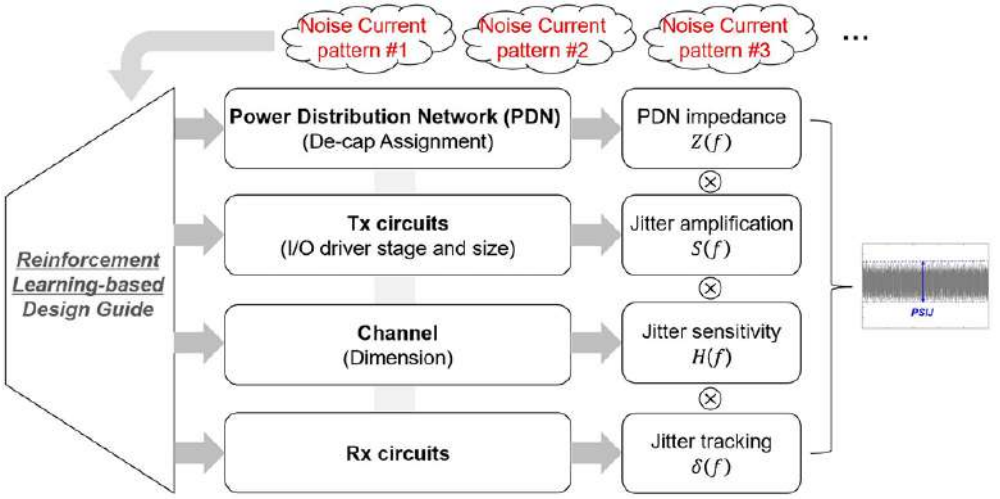
3-11 : PSIJ Based Integrated Power Integrity Design for HBM Using Reinforcement Learning: Beyond the Target Impedance

❖ 고속 I/O 시스템에서는 PSIJ(Power Supply Noise Induced Jitter)가 전체 지터의 주요 원인이 됨

❖ 기존의 Target impedance 기반 PI 설계만으로는 부족하기 때문에 PDN+Channel+I/O Drive를 통합적으로 고려한 PSIJ 기반 설계 최적화가 필요



⟶ 패키지 및 면적 제약, 디캡 배치의 한계로 인해 PSIJ 제어가 어려워짐

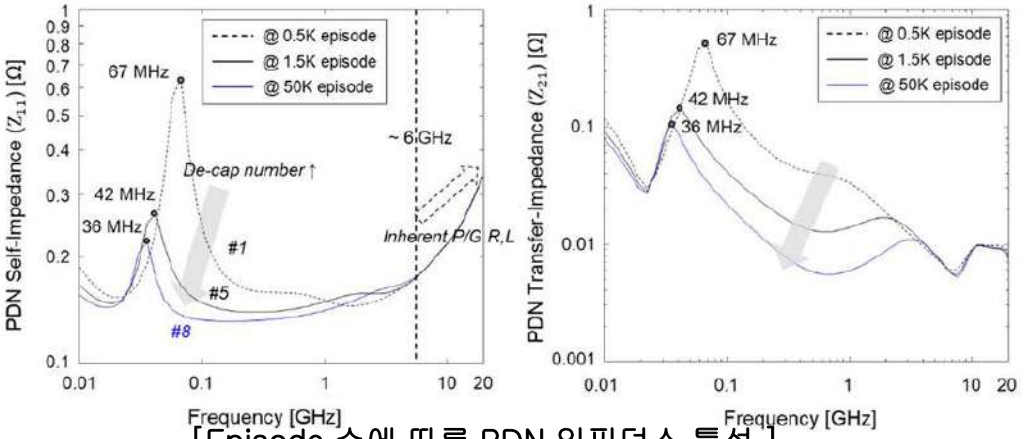


[PSIJ 설계 흐름도]

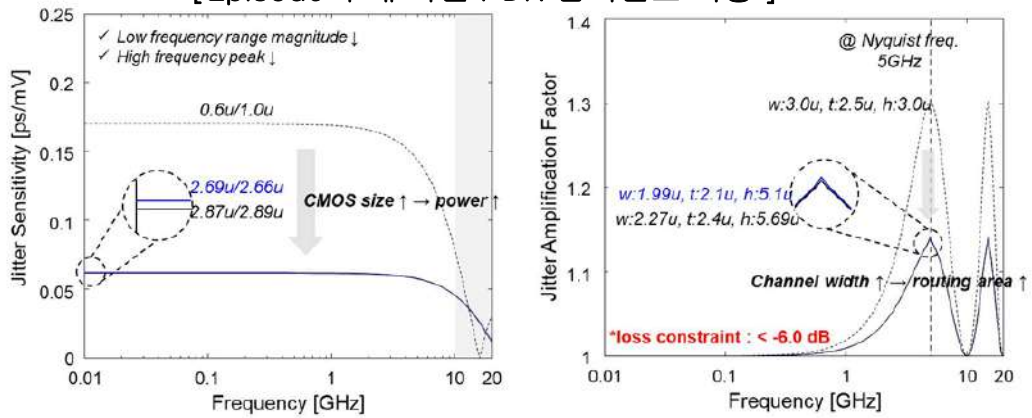
3. DesignCon 2025 자료 소개

3-11 : PSIJ Based Integrated Power Integrity Design for HBM Using Reinforcement Learning: Beyond the Target Impedance

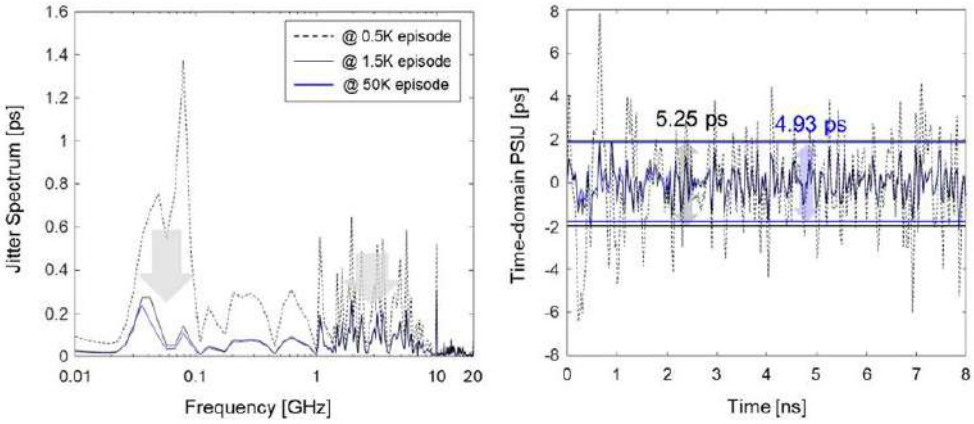
❖ RL(Reinforcement Learning)을 활용하여 HBM I/O 인터페이스의 PSIJ를 최소화하면서도 면적 및 전력을 효율적으로 사용하는 최적 설계 도출
- PSIJ 구성요소 : PDN 임피던스, I/O Driver Jitter 민감도, 채널 손실에 따른 Jitter 증폭, Rx 측 Jitter Tracking 능력



[Episode 수에 따른 PDN 임피던스 특성]



[Rule-based 대비 RL 결과 비교]

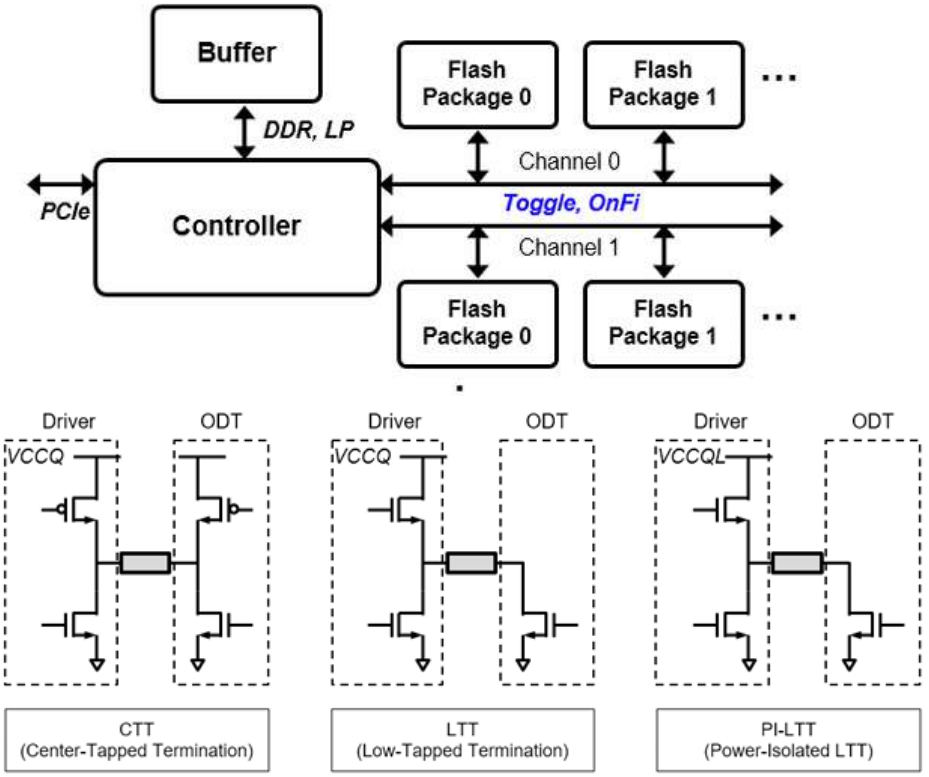


[최적화 전/후 구조 결과]

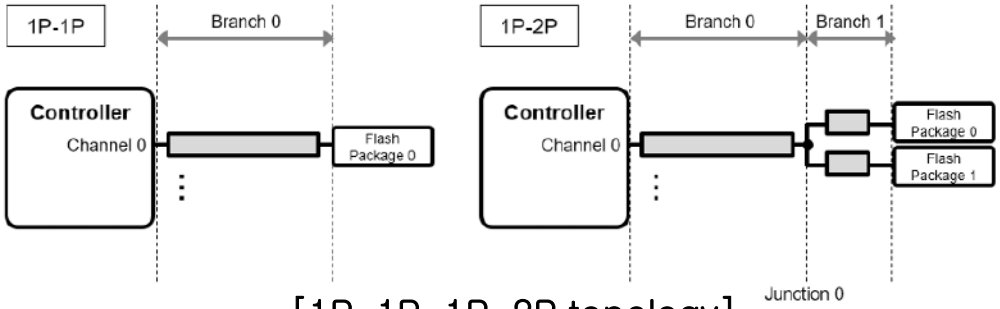
3-12 : Off-Chip Design Method for Improving Signal Integrity in Multi Branch Parallel interface of Non-Volatile Memory (1/2)

SSD(Solid State Drive)의 Architecture

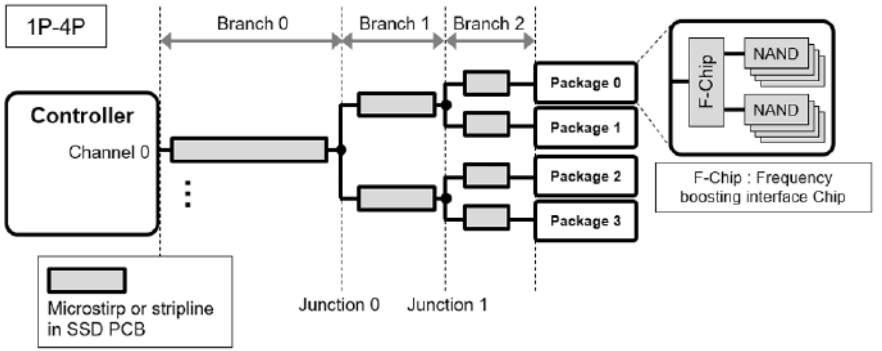
- 고속 SSD 시스템에서 컨트롤러와 NAND 간 병렬 인터페이스(1P-2P, 1P-4P) 사용 증가
  → 멀티 브랜치 구조의 일반화로 인해 SI/PI 문제 발생 -> Reflection, Cross Talk, Noise
- 1p-4p구조에서 Eye Margin 급감
- 기존 방식은 branch 길이 비율을 90:10~93:7로 조절하여 stub을 최소화 하려했지만, 반사타이밍이 비효율적



[SSD의 Arichitecture]



[1P-1P, 1P-2P topology]



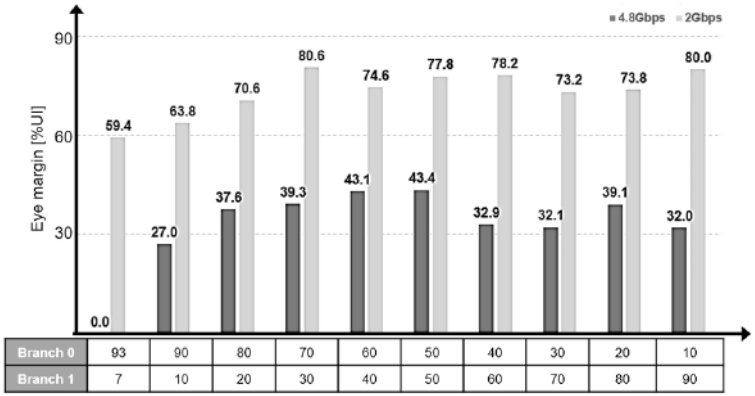
[1P-4P topology]

3. DesignCon 2025 자료 소개

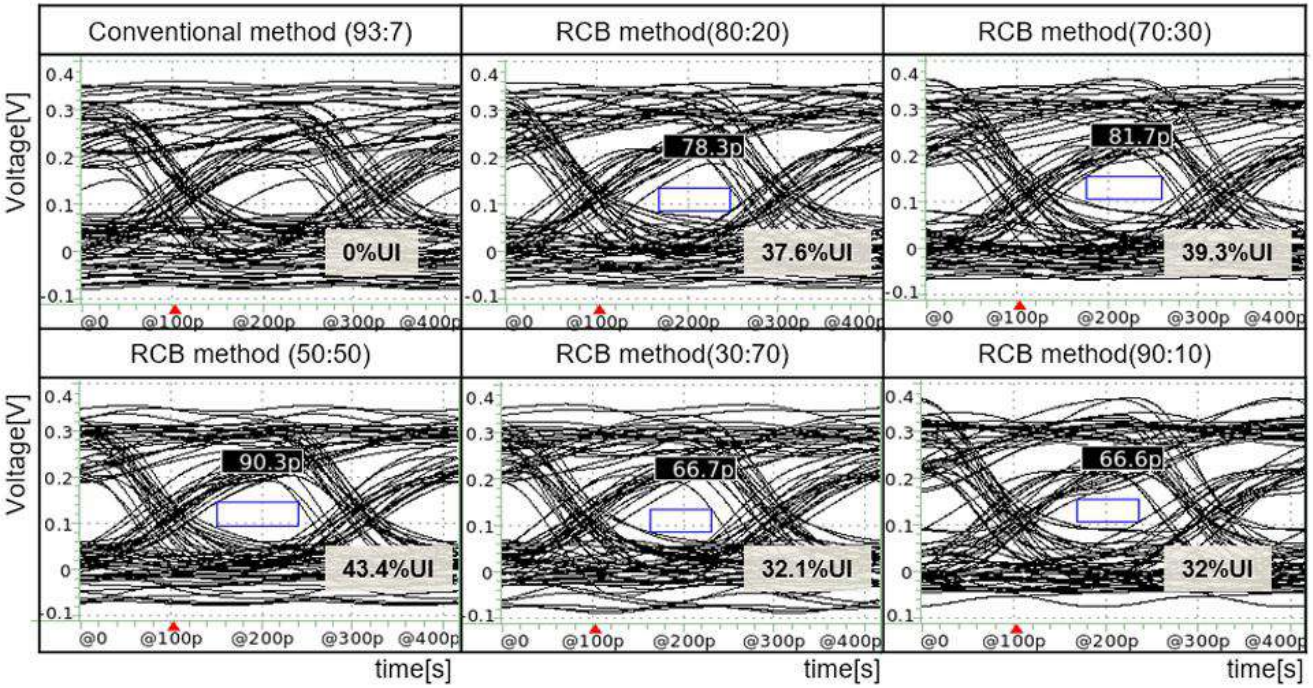
3-12 : Off-Chip Design Method for Improving Signal Integrity in Multi Branch Parallel interface of Non-Volatile Memory (2/2)

Proposed Method

- RCB(Reflection-Controlled Branch) Method
  - 브랜치 길이 비율을 50:50 등으로 조절하여 반사파 도달 시간 제어
- 강화학습 기반 ODT 최적화
  - 강화학습+Virtual Environment + Simulation DB



[1P-4P topology]



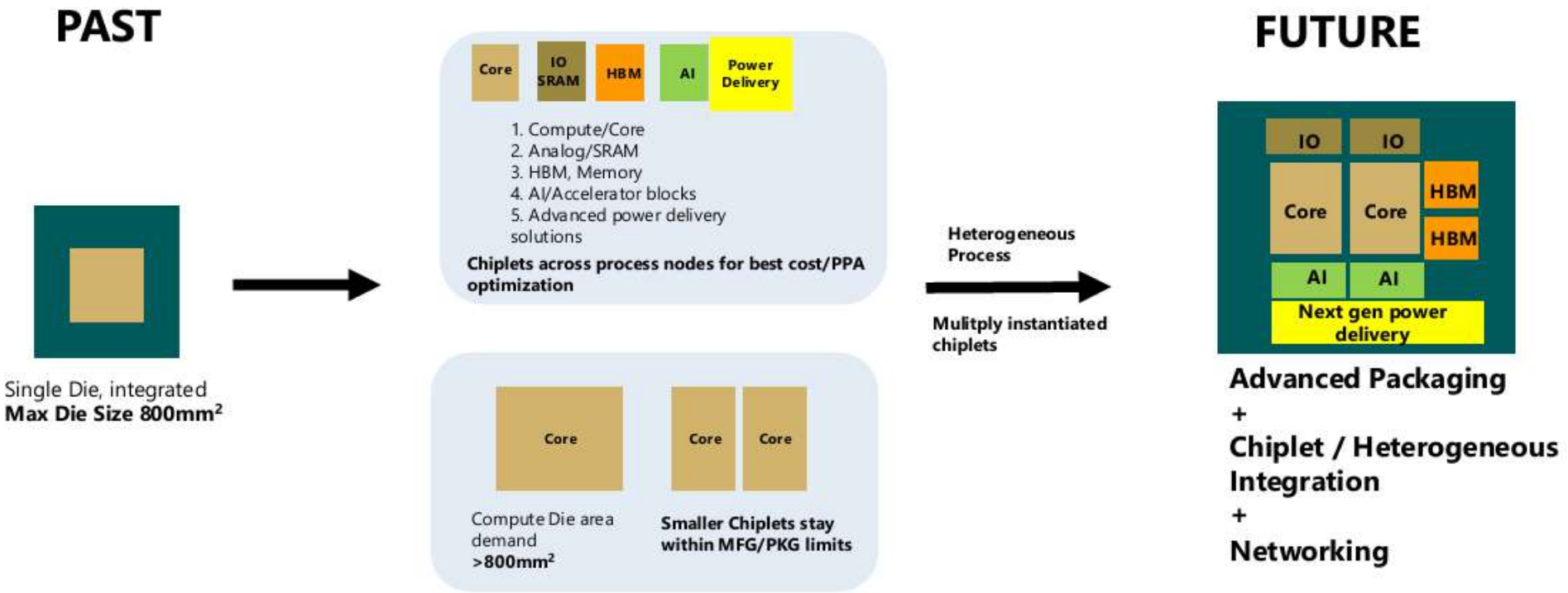
2Gbps에서 Eye Opening은
59%에서 81% UI

3-13 : Navigating the Complexities of Silicon Interposer Design (1/4)

반도체 아키텍처(Architectural)의 진화

- Past : Single Die 기반 아키텍처
- Future : **Advanced Packaging** + **Chiplet/Heterogenous Integration** + **Networking (Co-design 필수)**

→ 기능별로 칩을 분리하고 각각 다른 공정 노드 사용하는 방향으로 진화



Moore's law still alive – delivered through Advanced Packaging and Chiplets

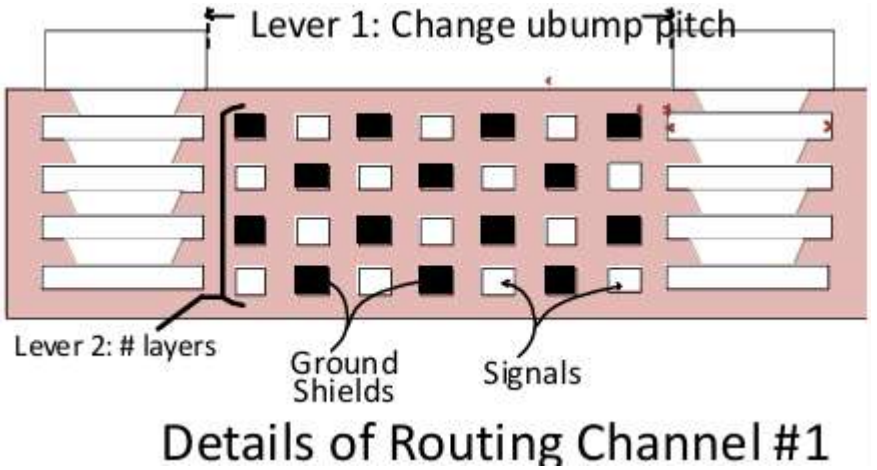
Chiplet/Heterogenous Integration - Requires Architecture, Packaging & Manufacturing Co-Design

3-13 : Navigating the Complexities of Silicon Interposer Design (2/4)

Bandwidth = # of data signals * Speed of Signaling

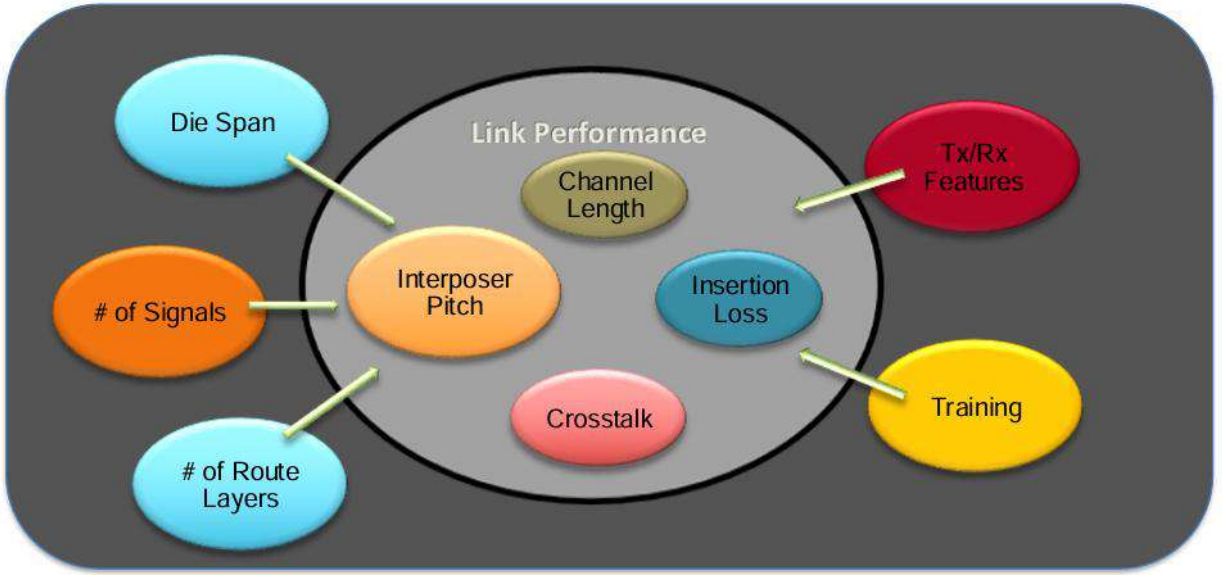
Levers for optimizing across vectors:

- Scaling ubump pitches
- Increase number of routing layers
- Scale routing layer density
- Metal thickness of routing layers
- Dielectric thickness



Details of Routing Channel #1

SI&PI challenges in interposer design



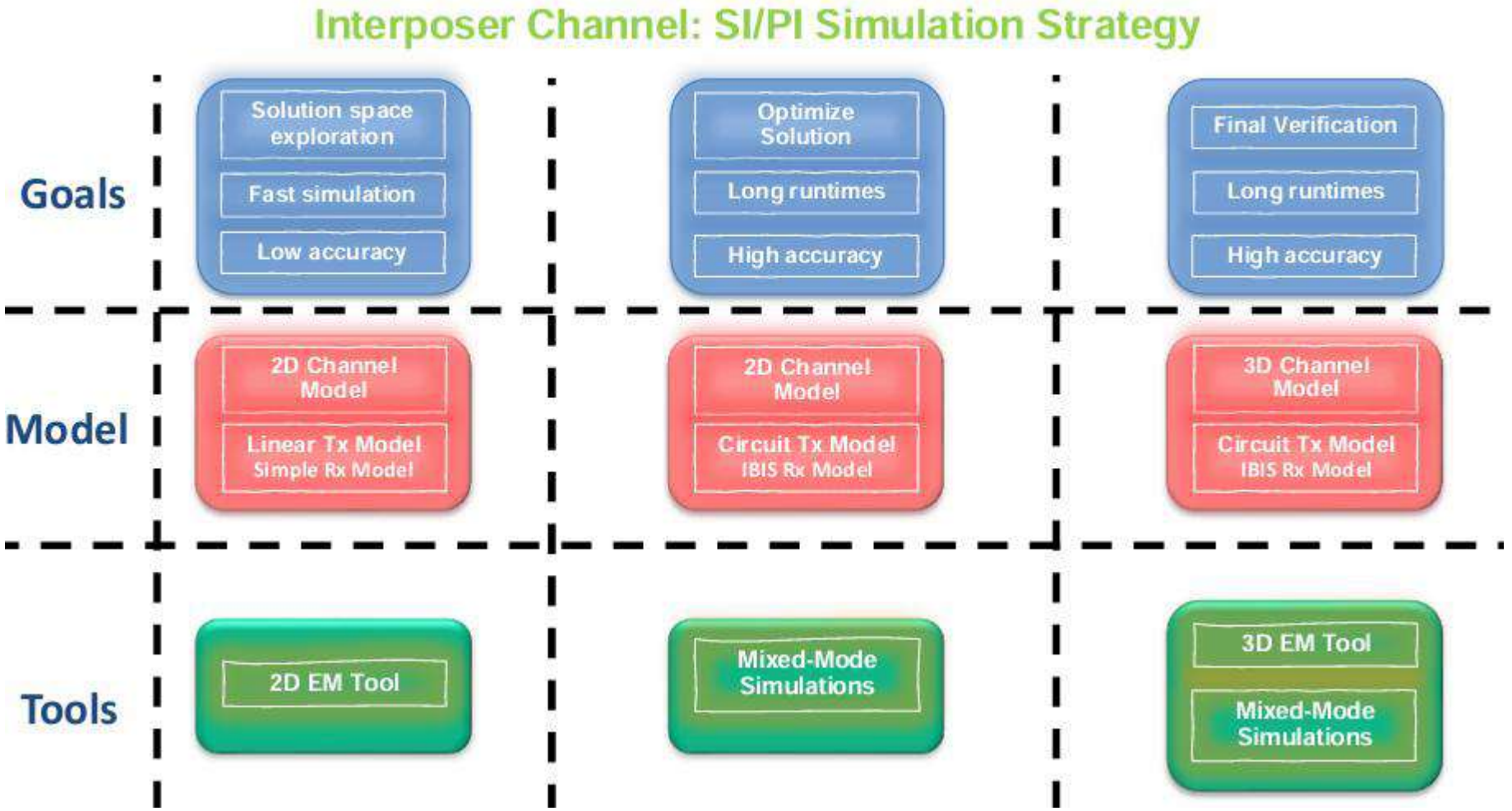
주요 SI 문제

- Crosstalk, Insertion Loss, Eye Margin 저하
- Routhing pitch, 채널 길이., Tx/Rx 특성, GND 레이어 등 영향

3-13 : Navigating the Complexities of Silicon Interposer Design (3/4)

3-step simulation approach

- Multi-block flow로 HBM 등 1k 채널 이상 대용량 채널 병렬 추출
- 64 코어 병렬 분석

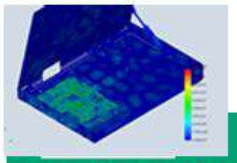


3. DesignCon 2025 자료 소개

3-13 : Navigating the Complexities of Silicon Interposer Design (4/4)

Eda 툴/산업 과제 및 미래 방향

- 복잡한 레이아웃에 대해 SI/PI 모델 추출과 검증 시간 증가
- PI 분석, 레이아웃-모델 변환 속도 문제
- Hybrid Solver + AI 기반 자동화 흐름 필요



•Limited SIPI Resources

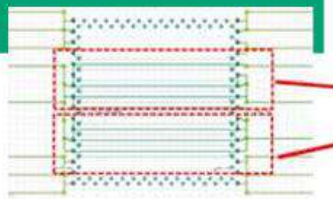
- Not all nets are extracted or closely reviewed for SI
- Coupling/Noise between PDN and SI interfaces is identified later in the design cycle. (during EMI/EMC lab testing)
- Increased design risk (simple SI issues may lead to a board re-spin or SI performance inconsistency, etc.)

• Scalable Workflow

- An efficient workflow to identify SIPI issues enables the team to prioritize resources.
- Database management is key as it will enable the team to iterate effectively over the layout and validation flows.
- Automation can be effectively deployed with a well-defined extraction methodology.

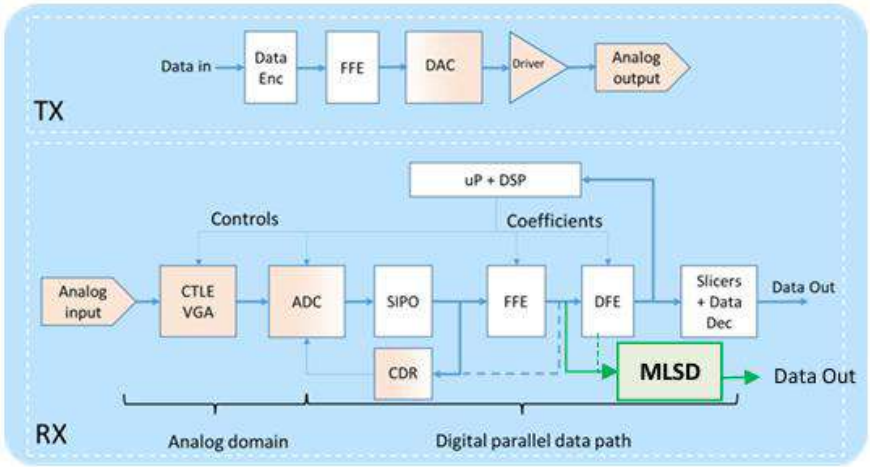
• ODM and CM Design Reviews

- Manual steps and consumes SIPI resources for repetitive tasks.
- Translation runtimes and scale limit the ability of the SIPI team to validate changes and optimizations.

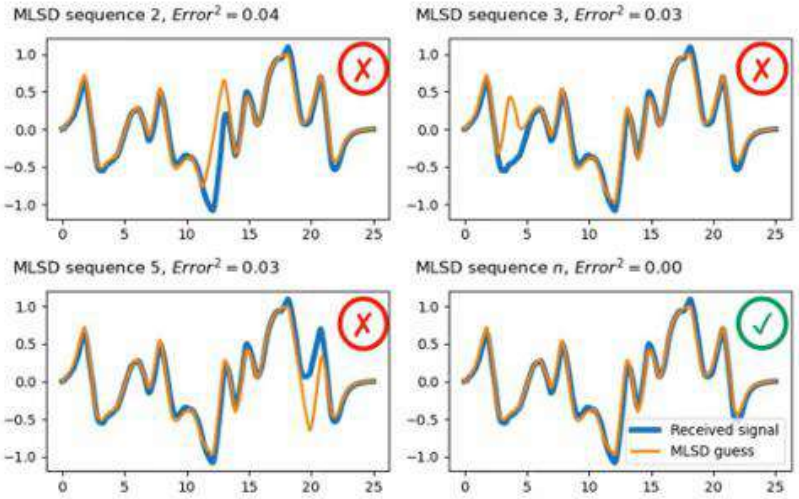


3. DesignCon 2025 자료 소개

3-14 : Beyond 200G Challenges Towards 400G Systems: Investigating OIF and IEEE compliant Channel Design with COM-MLSE Equalization. Implementation, Measurement and Correlation. (1)



Recently stepped up to the **M**aximum **L**ikelihood **S**equence **D**etection (**MLSD**).

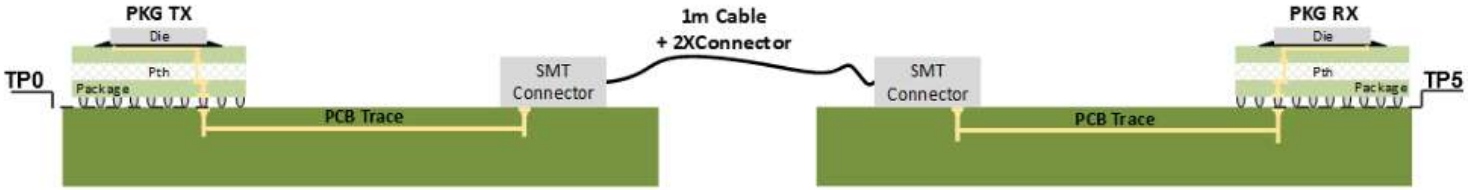


- 기존의 Equalization 기법 : FFE, DFE → SerDes 아키텍쳐에서 BER을 충족시키기 어려워짐
- 강한 FEC(Forward Error Correction) 적용은 복잡성 증가, 전력 소비 증가, latency 문제가 발생함
- MLSD Equalization : Viterbi Algorithm 활용하여 이전 심볼이 현재 심볼에 영향을 받는 ISI 패턴을 이용
- 가장 가능성 높은 데이터 시퀀스를 결정

3. DesignCon 2025 자료 소개

3-14 : Beyond 200G Challenges Towards 400G Systems: Investigating OIF and IEEE compliant Channel Design with COM-MLSE Equalization. Implementation, Measurement and Correlation. (2)

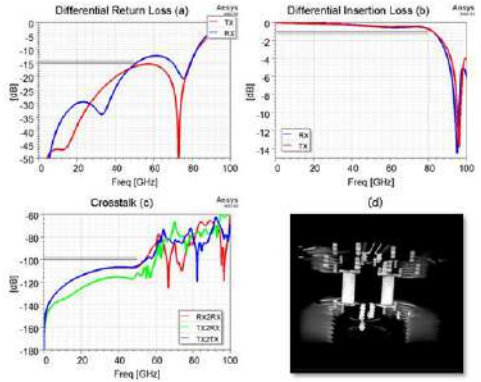
[200G E2E Channel Design – Simulation and Measurement Correlation]

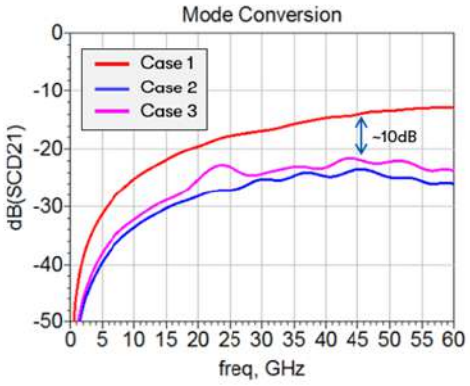


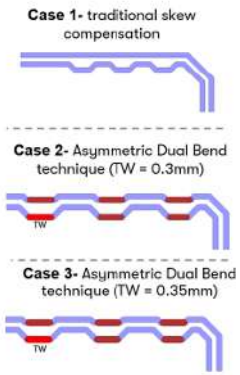
224G 패키지 디자인 요소
- Advanced material
- Skip-layer routing
- Finer BGA pitch
- Thinner cores

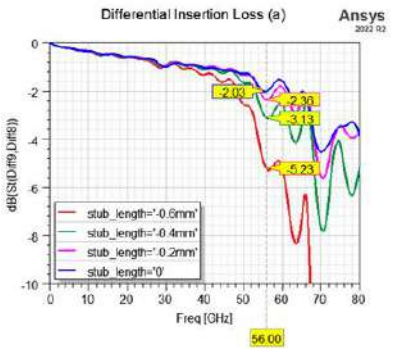
224G PCB 디자인 요소
- Skip-layer Design
- Smooth copper (HVLP type)
- Ultra-low loss dielectric material
- skew 보상기법

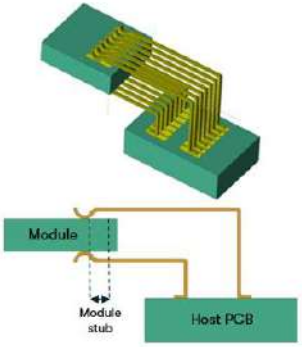
224G OSFP/QSFP Connector
- Soldering
- 조립 및 결착에 따른 Alignment 변화
- 결착부 Stub의 길이







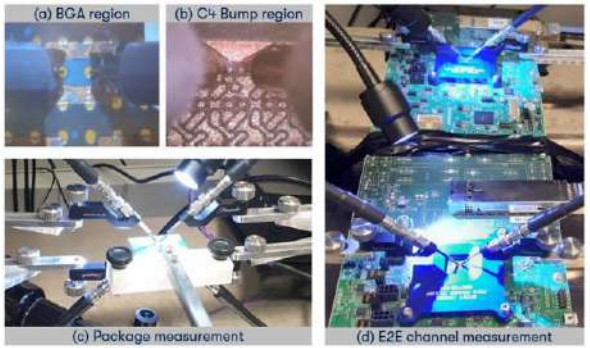


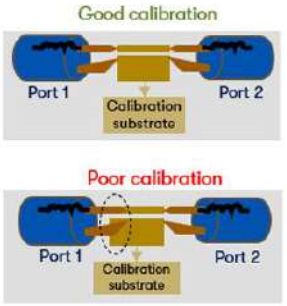


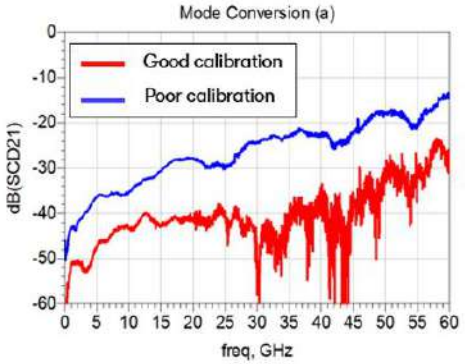
3. DesignCon 2025 자료 소개

3-14 : Beyond 200G Challenges Towards 400G Systems: Investigating OIF and IEEE compliant Channel Design with COM-MLSE Equalization. Implementation, Measurement and Correlation. (3)

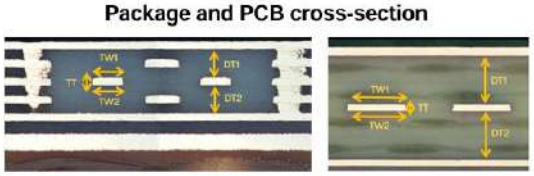
224G 패키지 및 PCB 측정
- Probe : parasitic 최소화 선정 (논문에서 SG 50um pitch, GSG 500um pitch 사용)
- Calibration : E-cal 또는 De-embedding 기법 활용
- Symmetry and Probe Placement : Probe calibration 시 대칭적으로 수행 필요

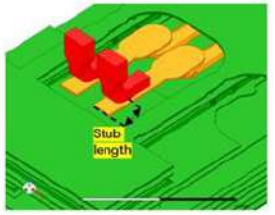


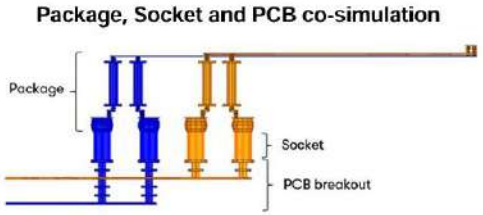


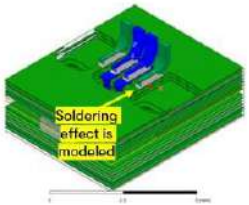


Co-Modeling 요소
1) 패키지 및 PCB 특성 : 층간 두께, 선폭/선간, 에칭factor
2) Copper Roughness 모델링
3) 시뮬레이션 모델 구분 : 패키지, 소켓, PCB 등으로 분리
4) 완성된 모델 : Cascade 연결하며 모델 간 특성 검증









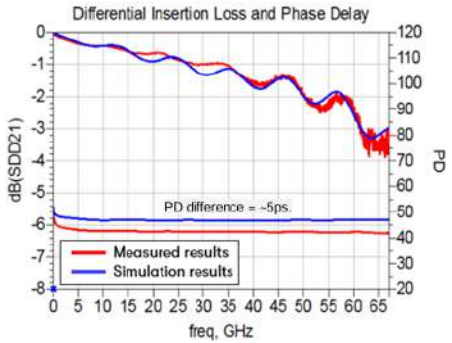
3. DesignCon 2025 자료 소개

3-14 : Beyond 200G Challenges Towards 400G Systems: Investigating OIF and IEEE compliant Channel Design with COM-MLSE Equalization. Implementation, Measurement and Correlation. (4)

[200G Package 및 E2E 측정결과와 시뮬레이션 결과의 비교]

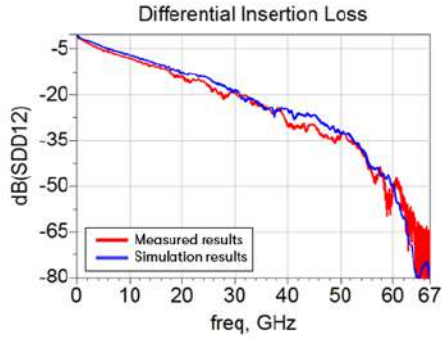
Package Measured vs. Simulation

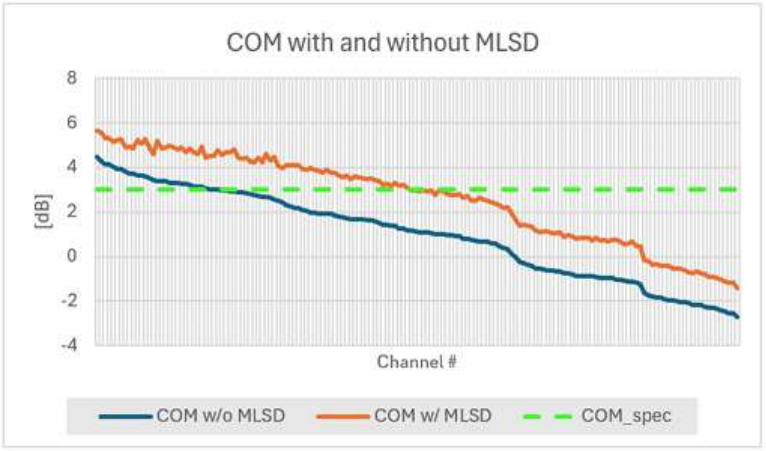
Loss Ripples: Caused by impedance mismatch (package traces at 85 ohms vs. measurement equipment at 100 ohms)



E2E Channel Measured vs. Simulation

Module stub length and other channel building blocks adjusted for accurate correlation.



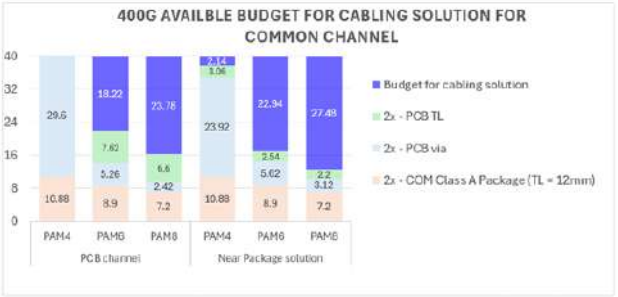


- 패키지 및 E2E 측정결과와 시뮬레이션 결과간 유효성 확인
- MLSE Equalization 적용 시 1~1.5dB 이상 COM 개선 확인 (COM Base 여서 실제 환경에서 검토 필요)

[Challenges Toward 400G System]

PAM-L	$\log_2(L)$	Nyquist Frequency [GHz]
4	2	112
6	~2.5	89.6
8	3	74.66

Data Rate [Gb/s]	112	224	448		
Number of PAM levels	4	4	4	6	8
Bits per symbol	2	2	2	2.58	3
Signaling rate [Gbaud]	56	112	224	179.2	149.32
Unit interval [ps]	17.85	8.92	4.46	5.58	6.69
Fundamental frequency [GHz]	28	56	112	89.6	74.66
Required SNR at slicer [dB]	18.42	18.42	18.42	22.04	24.56
SNR penalty [dB]	0	0	0	3.62	6.14



- 400G PAM4는 1.33ps 미만의 skew 처리가 필요하나, 재료 특성과 pcb 허용 오차로 쉽지 않음.
- MLSD의 증가는 복잡성을 증가시키고, 소비 전력 증가로 이어짐. 400G는 기술적으로 많은 발전이 필요함

3-15 : PCI Express & PAM4: Balancing Silicon and interconnect interdependencies for 128 GT/s (1)

PCIe 7.0 Advances in Technology

Version 0.7: Foundation from Prior 6 Generations

- Data Rate: 128 Gb/s with PAM4 Signaling
- Maximum First Bit Error Rate (without accounting for burst errors): 1e-06
- Target Channel Reach: Like PCIe 6.0 (4"-14" system routing and 2"-4" AIC routing in 1-conn topology)
- Pad-to-Pad Channel Loss: -36dB. JTOL is NOT defined yet
- Ref Transmitter : 4-tap Tx Equalization scheme, Link margin sensitivity to tap coefficient resolution and Tx presets to be studied
- Ref Receiver : Reference CTLE proposal & ADC-based Rx Architecture (Rx FFE with 24 post-cursor taps and 4 pre-cursor taps + 1-tap DFE) (h1/h0 < 0.5 to limit DFE burst error)
- Reference Package Models for Root Complex (RC) and End Point (EP) will be defined

Improvements Required

- Root Complex reference package insertion loss and reflection
- Connector insertion loss and return loss
- PCB loss
- Via insertion & return loss
- Xtalk reduction

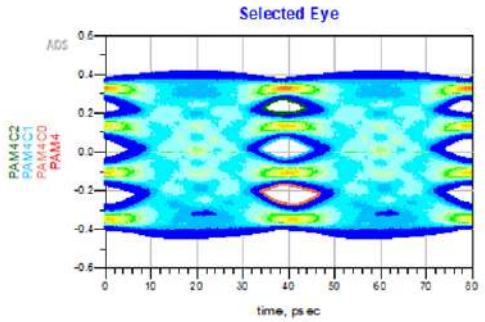
3. DesignCon 2025 자료 소개

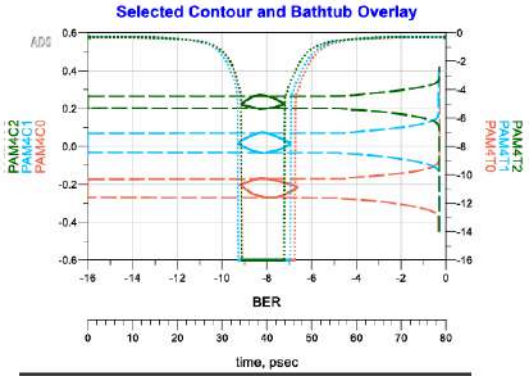
3-15 : PCI Express & PAM4: Balancing Silicon and interconnect interdependencies for 128 GT/s (2)

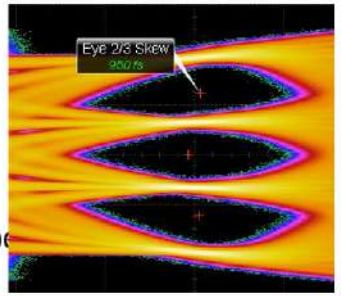
[모델링 및 시뮬레이션 요구 사항]

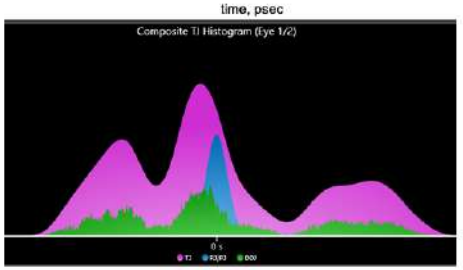
Comprehensive Simulation Capability

- **SER** (Up to millions per minute)
  - Eye measures
  - Bathtubs
  - Mask tests
- **Diagnostics** for design development
  - Waveforms
  - Linearity
  - Skew
  - Jitter
- Models
  - Channel, Pre and Post layout
  - Tx and Rx, IBIS-AMI, PAM capable, Standard Spe
- Statistics, Swept Measurements;
  - for design space exploration and case studies







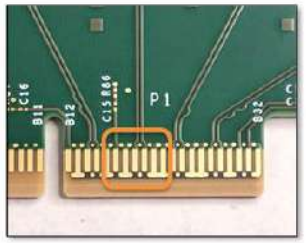


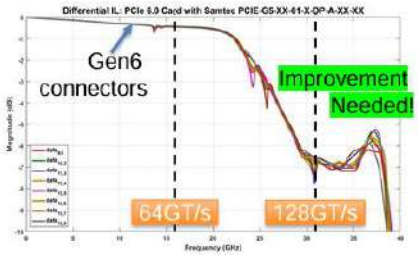
- 대규모 SER 분석 필요
- Eye Diagram, Jitter, Mask Test 등 가능해야 함
- Channel, TX, Rx, IBIS-AMI 등 모델링 중요
- 정확한 초기 시뮬레이션 중요
- Statistical 과 Bit-by-Bit 시뮬레이션 둘 다 필요

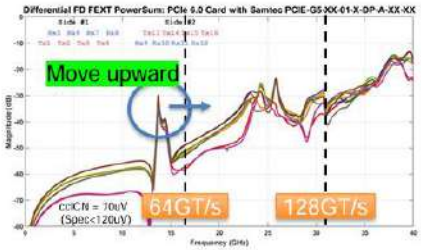
3-15 : PCI Express & PAM4: Balancing Silicon and interconnect interdependencies for 128 GT/s (3)

CEM Interface 6.0 → 7.0

- Still backwards compatible
- Expect most changes to occur at the edge card pad
- Shorter pads will improve insertion and return loss
- Ground vias moved into the pads move resonances
- Pathfinding is ongoing…





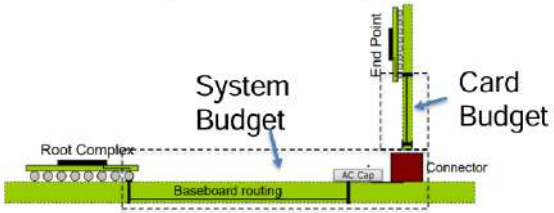


Guidelines for System and Cards

- First order "Loss Budgets" are no longer working
- Channel noise detracts a penalty from otherwise maximum length calculations
- Gap\Penalty near 4 dB!

	PCIe 4	PCIe 5	PCIe 6
Target	28	36	32
PCB	10" 1.35 db\inch @ 8GHz	10" 1.1 db\inch @ 16GHz	9" 1.0 db\inch @ 16GHz
RC Package	5	8.5	8
Vias, Caps	1	1.5	1.75
Connector	0.5	1.5	0.75
Card	8.5	9.5	8.5
Reflection & Crosstalk Penalty	<1	4	4
Total	28.5	36	32

- Considering system and card budgets from PCI-SIG
  - IL, RL, and crosstalk
  - Frequency domain mask + integrated metrics
  - Clarity for 'What is good enough'
  - Design aid and simulation only – not measurable

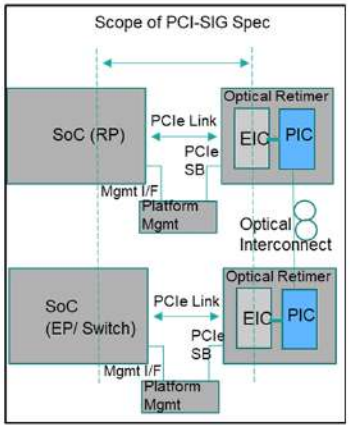


CEM(Card Electromechanical Specification) 6.0 → 7.0 진행중
- 기존 loss budget 방식이 유효하지 않음
- 패드를 짧게, GND Via의 위치 변경 등 커넥터 인터페이스의 변화 (IL, RL 개선)

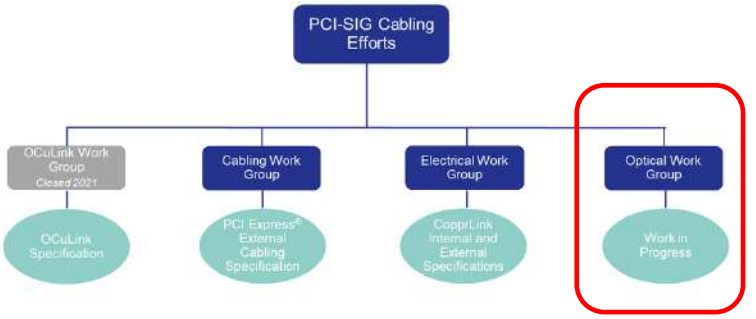
3-15 : PCI Express & PAM4: Balancing Silicon and interconnect interdependencies for 128 GT/s (4)

Current Goals of Optical PCIe

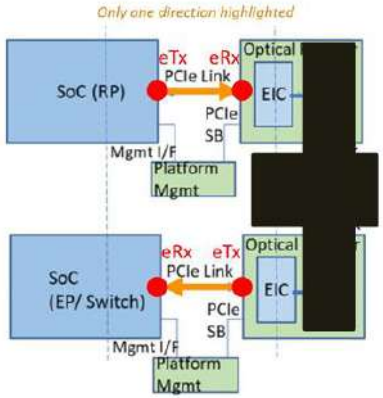
- Define optical link extension with technology neutrality
- Take advantage of recent PHY Logical enhancements
- Form Factor Flexibility
- Standardize PCIe module management



Scope of PCIe Cabling Efforts



The success of optical PCIe will depend on the broad adoption of PCIe cabling

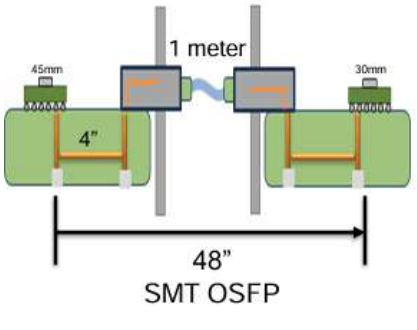


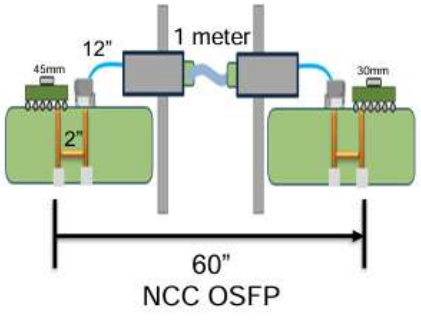
Need to define functional "what, where, how…"

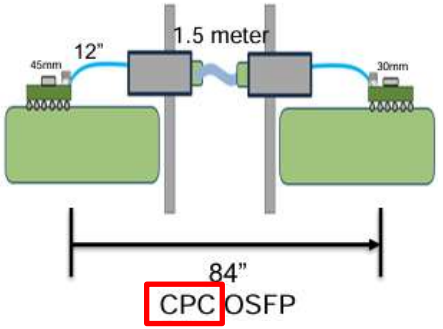
- PCIe 7.0에서 기존 Copper 기반의 채널은 Insertion Loss 및 Crosstalk, Jitter 문제 큼
- PCI-SIG에 Optical Work Group에서 Optical PCIe 솔루션 준비
- 기존 PHY 유지하면서 새로운 Optical interface 적용 시도
- 데이터센터 및 AI/ML 인프라에서 서버 간 PCIe 인터페이스 확장에 적합
- 현재 솔루션 공간이 확보되지 않았음. 표준화 진행

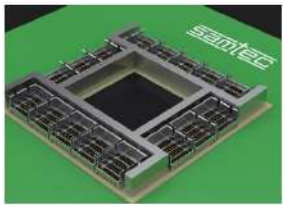
3-16 : Direct to Substrate 200G-PAM4 Co-Packaged Connectors: Is it a Reality? (1)

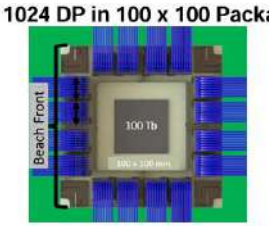
- Co-Packaged Connector(CPC) : PCB Trace 최소화하여, 패키지에서 직접 케이블을 연결하는 방식

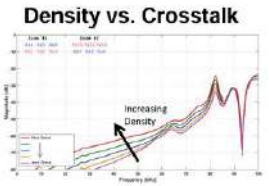


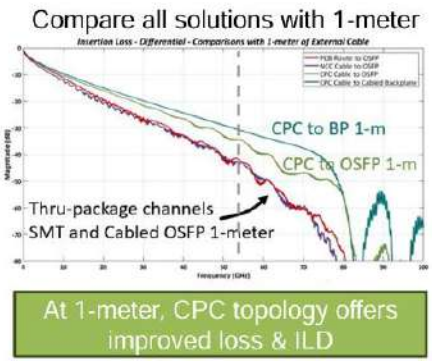


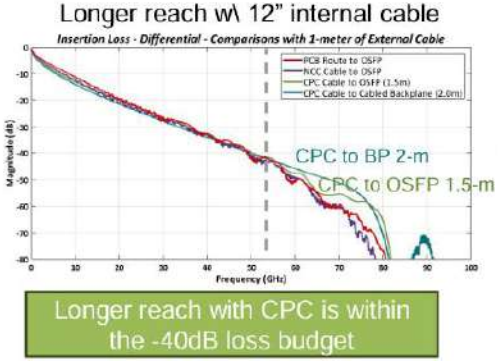


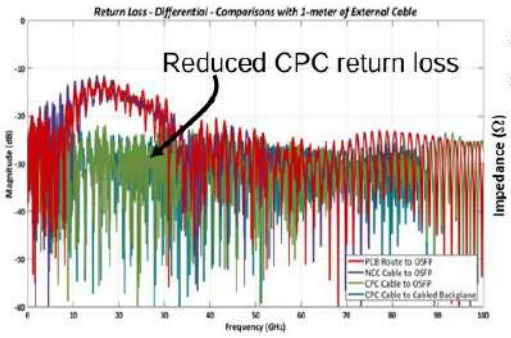


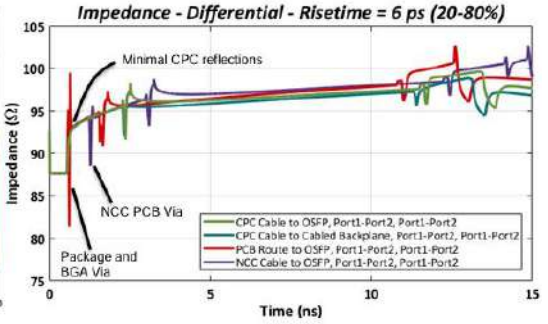










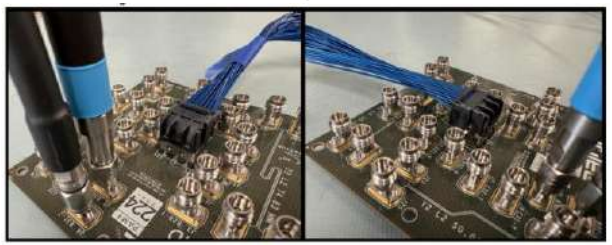


- 기존 방식에서 PCB Trace의 손실이 특히 53~56GHz 대역에서 심각함. 1m 이상 전송 어려움
- Package core, solder-ball, PCB via 등 반사 및 Crosstalk 증가 요인이 많음
- CPC 방식은 패키지에서 직접 OSFP/QSFP 등과 연결할 수 있음
- 개별 신호라인을 Shielding 하여 SI 확보하고, 2m 이상 신호 전송 가능

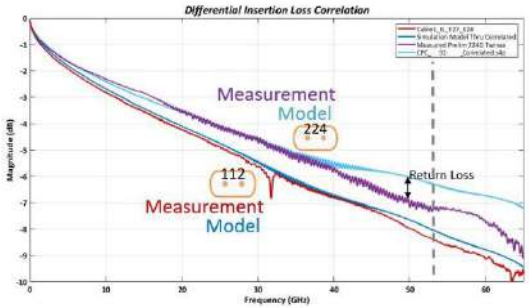
(NCC : Near Chip Cabled, OSFP : Octal Small Form-Factor Pluggable)

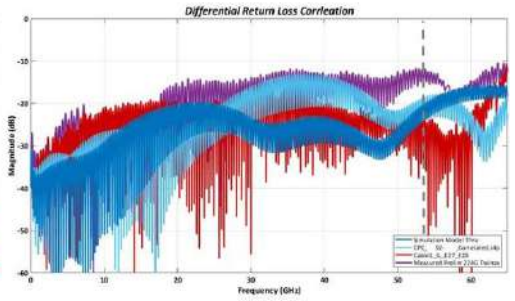
3-16 : Direct to Substrate 200G-PAM4 Co-Packaged Connectors: Is it a Reality? (2)

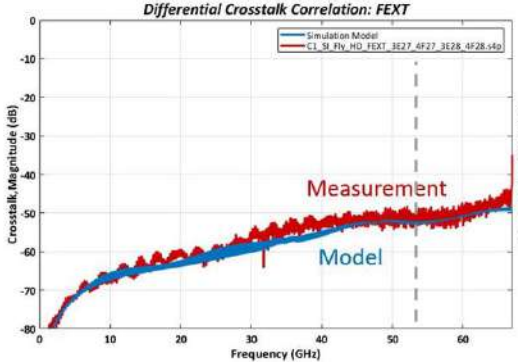
[Cable Assembly Measurement]

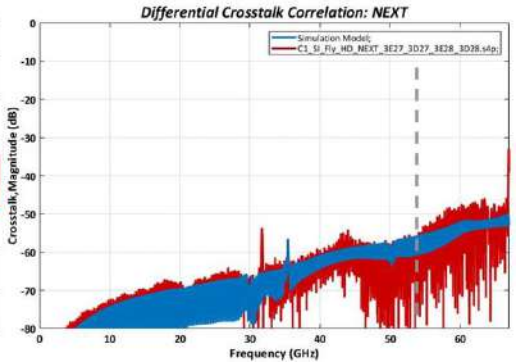


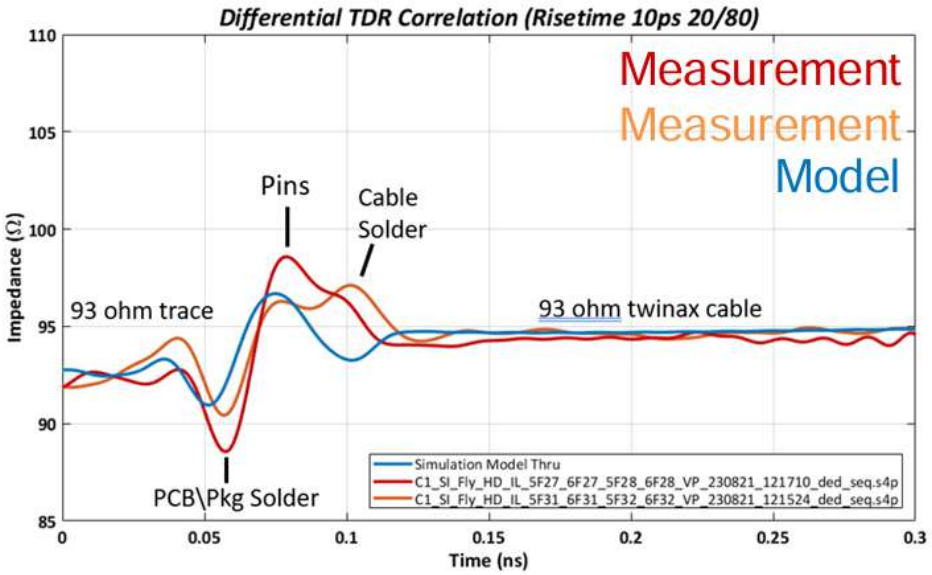
- 1.85mm Test points
- Fixture De-embedding bandwidth 65GHz
- 2X-THRU Impedance Correcting method를 활용하여 via-cable-via 특성 측정









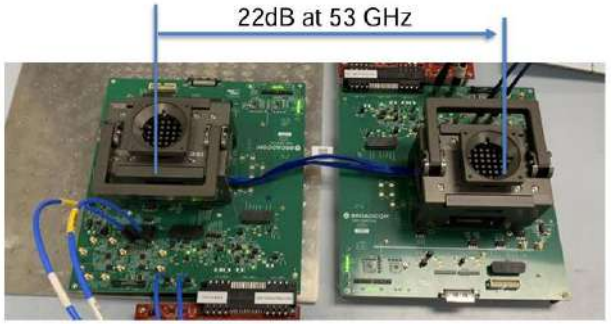


- IL, RL, Crosstalk, TDR 등 주요 항목에서 시뮬레이션 결과와 실측 결과간 유사성 확인
- 고밀도의 shielding effect가 Crosstalk 최소화하였음을 보임

3-16 : Direct to Substrate 200G-PAM4 Co-Packaged Connectors: Is it a Reality? (3)

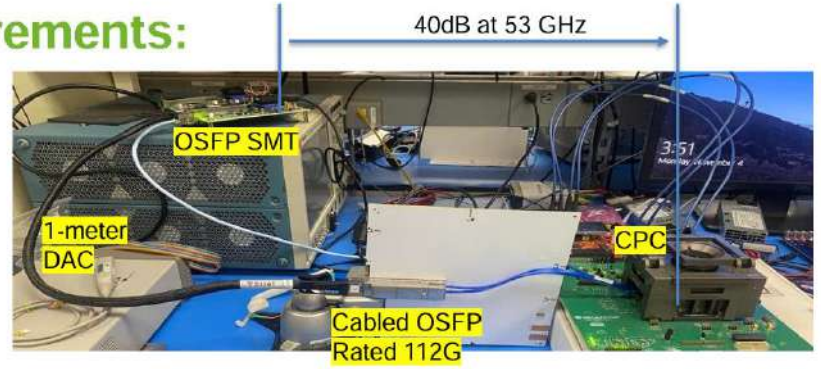
Channel Measurements:

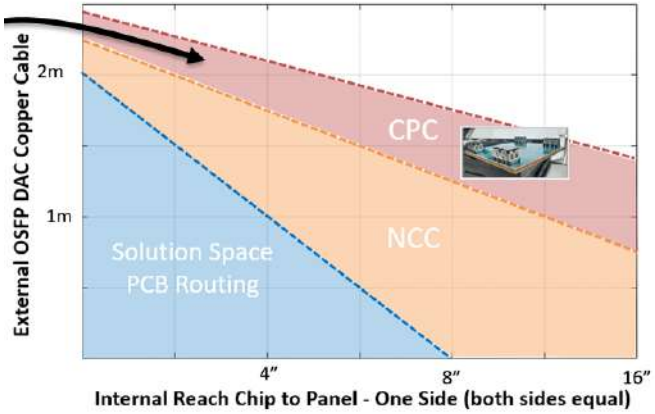
- Package-to-Package connectivity by CPC
- Total loss including package is ~ 22dB
- Results: < 1e-13BER, pre-FEC



Channel Measurements:

- CPC to OSFP
  - CPC Connector \ Device
  - OSFP 112G-Rated Connector
  - 1-meter 224G DAC Cable
  - OSFP 224G SMT Connector
  - BGA Device
- Total loss ~ 40 dB
- Results: < 1e-9, pre-FEC





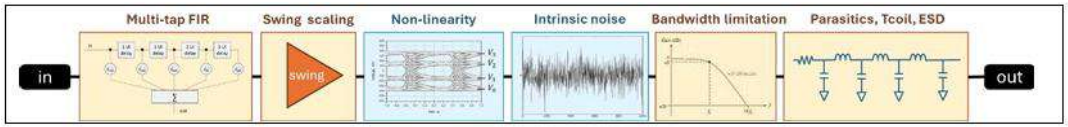
- CPC 사용 시 도달 거리 증가함을 보임
- 부품 간 변동성을 최소화 하는 것이 SI 유지의 핵심
- ERL, IRL 및 COM 등 시스템 수준 지표 활용하여 정량적 평가 필요
- Connector, Solder, PCB 가공 정밀도 개선 → IL, RL 최소화

(ERL : Effective Return Loss, IRL : Intergrated Return Loss)

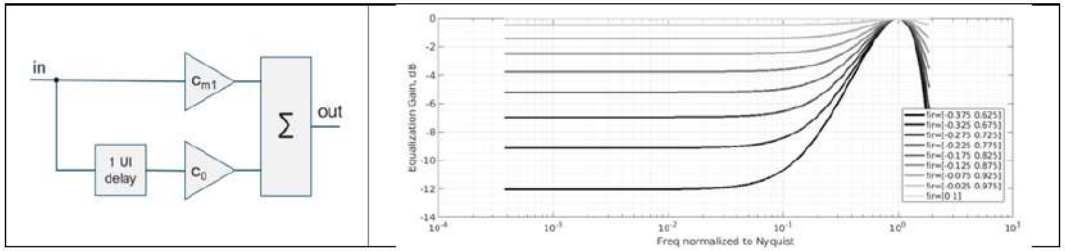
3. DesignCon 2025 자료 소개

3-17 : Genetic Algorithm-Driven IBIS-AMI Optimization for Robust 200G SerDes Design (1)

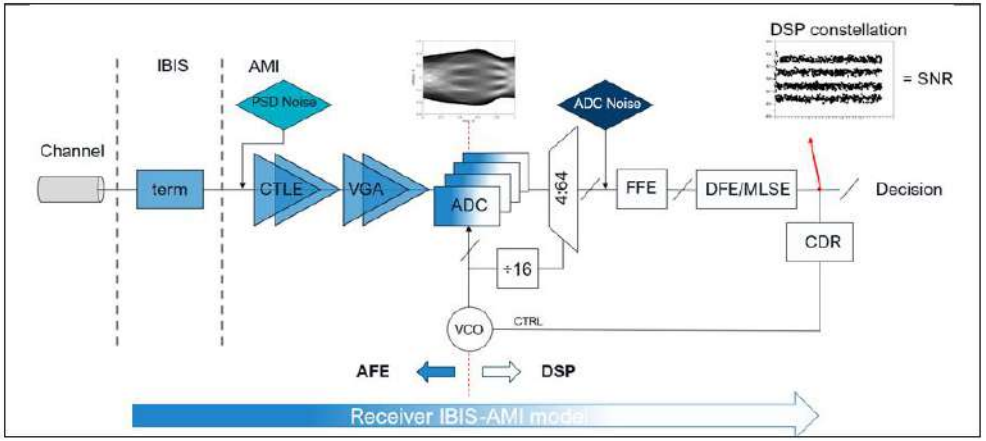
[Transmitter model block diagram]



[Transmitter FIR transfer function sweep]



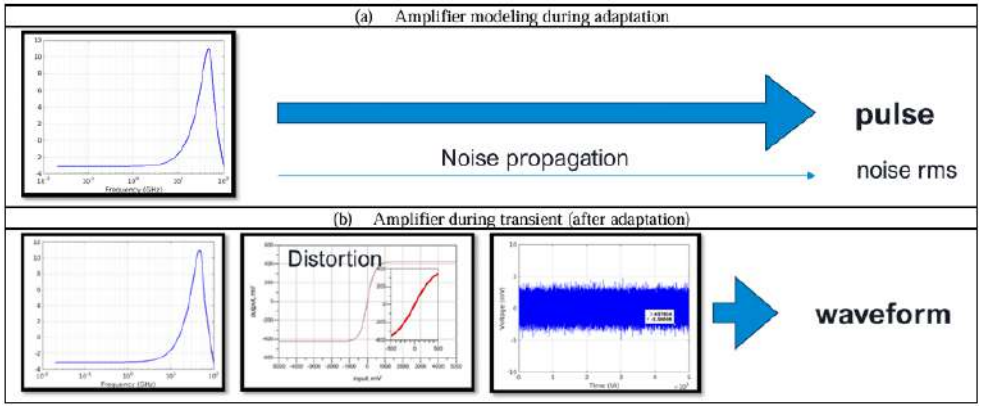
[Receiver model block diagram]



[EQ parameter optimization pool]

Block	EQ Parameter	100G permutations	200G permutations
TX	FIR	~4,000	~15,000
RX AFE	Mid-Band Boost	~4	~10
	CTLE	~25	~500
	VGA (is self-adapted)	~1	~1
RX DSP	FFE anchor point	~15	~15
	DFE 1st tap ratio	~6	~6
	FFE roaming	~3	~6
	Total	**36 million**	**6.75 billion**

[Amplifier stage modeling]



- AI 및 고속 컴퓨팅 환경에서 고속 신호 전송이 필수적임
- TX FIR, RX AFE(CTLE, VGA), RX DSP(FFE, DFE) 등 여러 EQ 파라미터 조합이 존재
- 100G SerDes의 경우 3,600만 가지 조합, 200G SerDes의 경우 67억 개 이상의 EQ parameter 조합 발생
- IBIS 모델의 신뢰성을 높이고, 과도한 연산 없이 최적의 SerDes EQ 설정을 찾는 방법 제안

3. DesignCon 2025 자료 소개

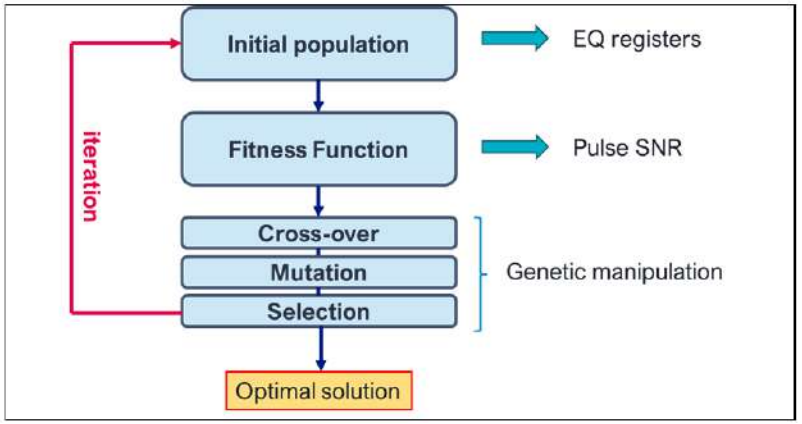
3-17 : Genetic Algorithm-Driven IBIS-AMI Optimization for Robust 200G SerDes Design (2)

- 기존 방식 (Brute Force, Hybrid Search) 의 연산량이 매우 큼
- 새로운 방식 (Genetic Algorithm) 적용

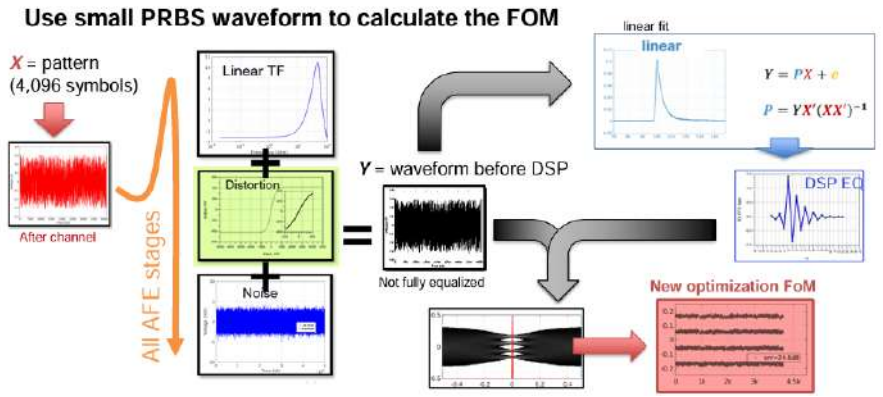
: non-Linearity 요소 반영하여 Waveform을 시뮬레이션 하면서 최적의 EQ 설정 (ISI 보정+증폭기 비선형 왜곡 최소화)

: Fitness function으로 SNR 및 BER 평가하며, Brute 대비 99% 연산 시간 절약

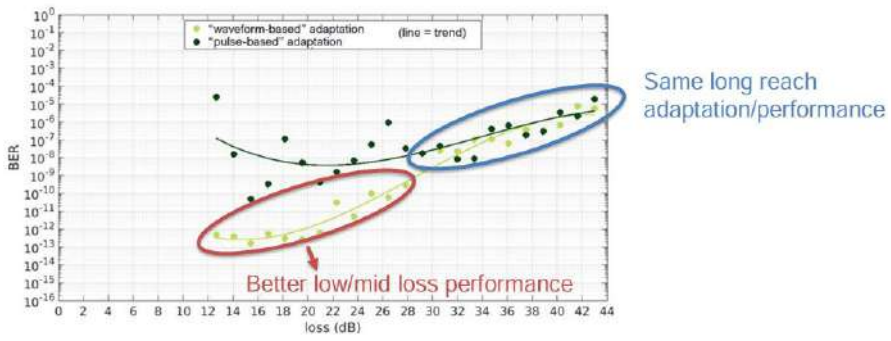
[Genetic algorithm diagram]



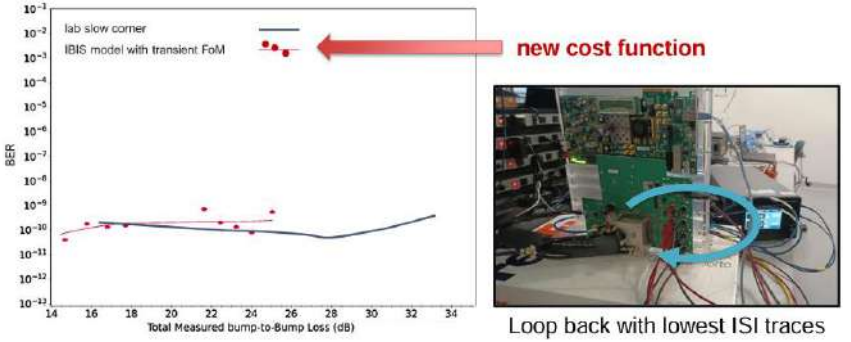
[New cost Function]



[New cost function results across loss]



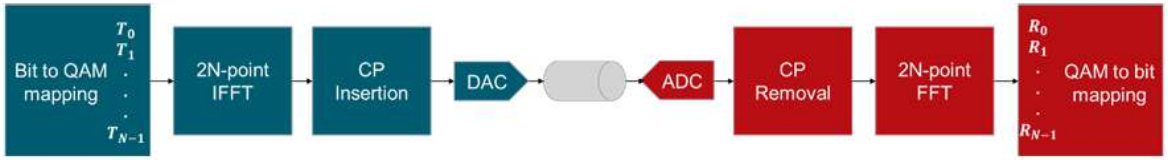
[Low loss lab comparison]



Loop back with lowest ISI traces

3-18 : IBIS-AMI Modeling and Simulation of DMT in Preparation for 448Gbps Applications (1)

[DMT signaling scheme]

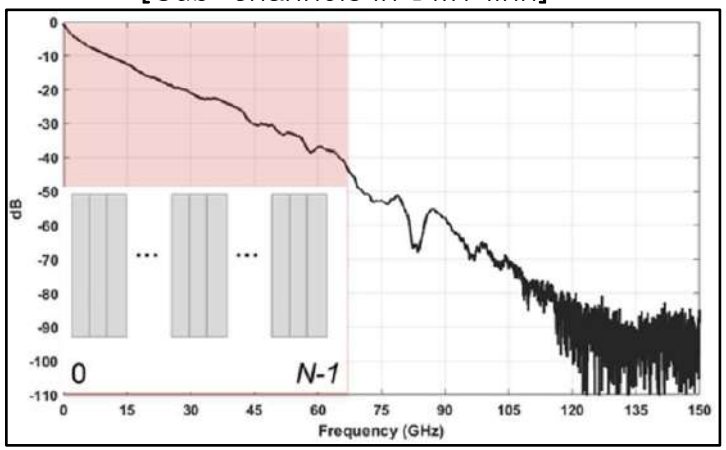


- 224Gbps 이상으로 증가하면서 PAM4, PAM6, PAM8 외 DMT(Discrete Multi-tone) Signaling 이 주목됨
- 주파수 대역을 여러 개의 sub-channel로 나누어 전송하며, sub-channel 별 SNR에 따라 최적의 변조방식 적용 가능
- IBIS-AMI 모델 확장하여 DMT 적용 → 차세대 400G+ SerDes 시스템

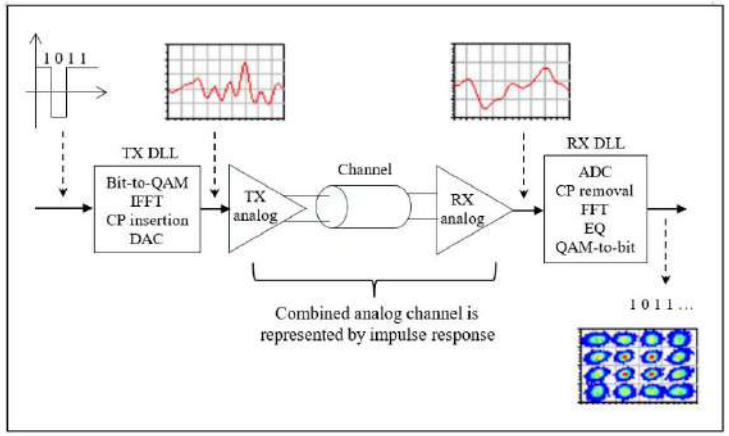
1)Tx : Bit loading 적용, IFFT 변환, CP(Cyclic Prefix) 삽입, DAC 모델 추가

2)Rx : ADC 모델 추가, CP 제거, FFT 변환, FDE(Frequency-domain Equalization), Bit recovery 및 QAM Decoding

[Sub-channels in DMT link]



[AMI Simulation flow of DMT link]



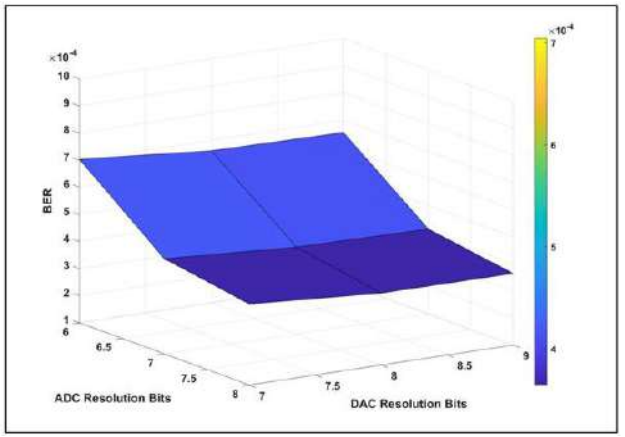
3-18 : IBIS-AMI Modeling and Simulation of DMT in Preparation for 448Gbps Applications (2)

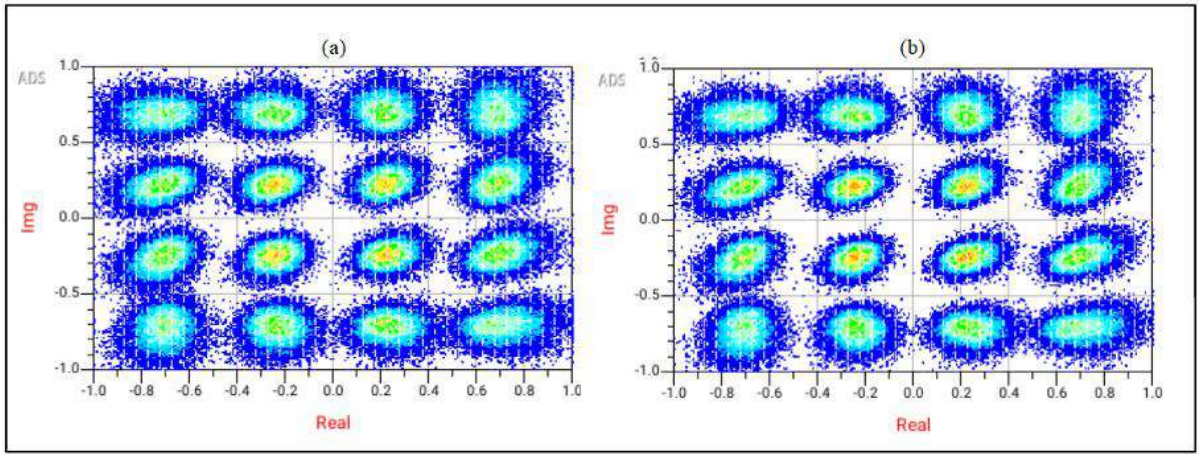
	Uniform QAM16	Uniform QAM32	Uniform QAM64	With bit loading
Overall BER	1.76×10^{-4}	2.61×10^{-3}	9.37×10^{-3}	3.42×10^{-5}
Actual data rate	152.44 Gbps	190.56 Gbps	228.67 Gbps	200.08 Gbps

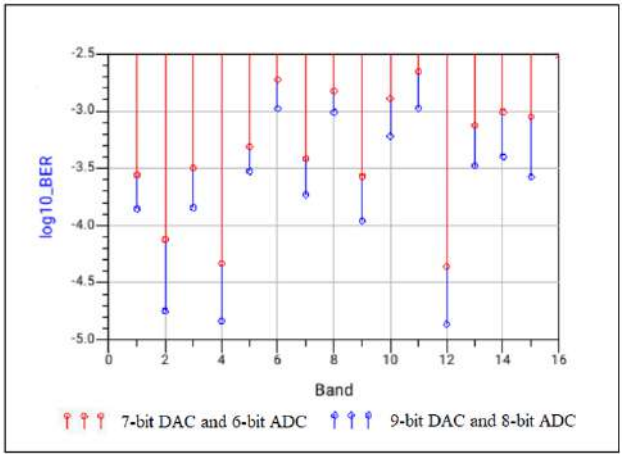
Table 3. BER and data rate at 100 GHz sample rate with uniform QAM order and with bit loading

	Uniform QAM16	Uniform QAM32	Uniform QAM64	With bit loading
Overall BER	8.72×10^{-4}	6.88×10^{-3}	1.67×10^{-2}	3.64×10^{-4}
Actual data rate	182.93 Gbps	228.67 Gbps	274.40 Gbps	242.96 Gbps

Table 4. BER and data rate at 120 GHz sample rate with uniform QAM order and with bit loading



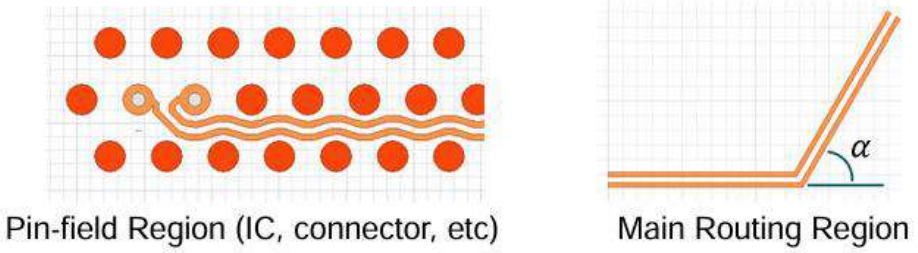




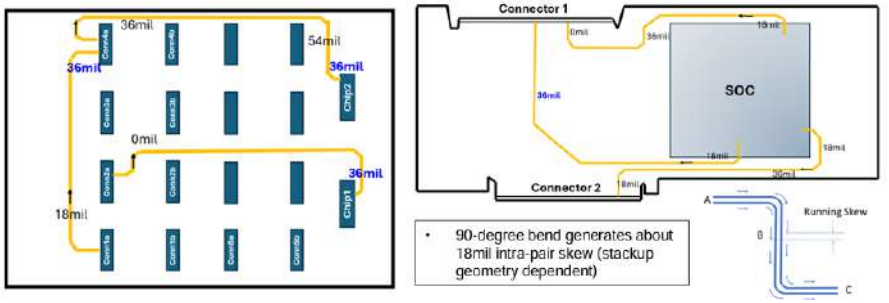
- 모든 sub-channel에 uniform한 QAM16, QAM32, QAM64 order를 적용한 경우와 bit loading을 적용한 경우 비교
- 100GHz & 120GHz sample rate에서 모두 bit loading을 적용한 경우가 BER 좋음
- ADC&DAC의 Resolution bit가 높을수록 SNR에 유리하여 BER 좋음
- IBIS-AMI 모델 확장을 통해 DMT 기반 시스템의 설계 및 최적화 가능

3-19 : Intra-pair Skew Electrical Delay Compensation for PCIe 6.0 (1)

[Source skew structure]

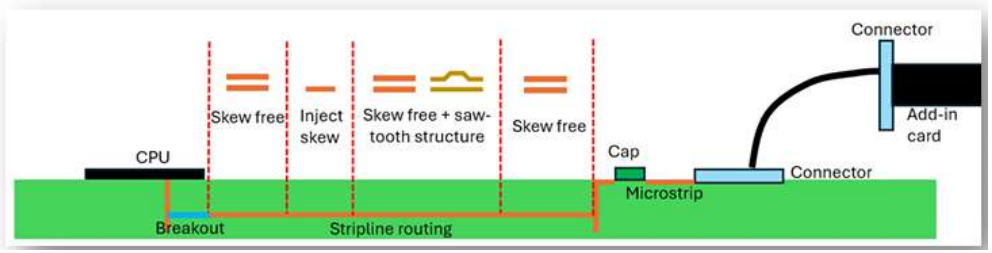


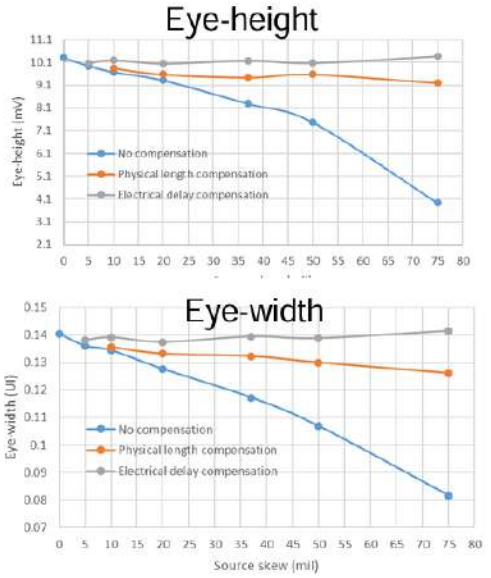
[Running skew examples]



- Intra-pair Skew : 차동 신호 쌍에서 P, N 경로 간 길이차이로 발생하는 시간 차이
- 주로 pin-field와 main routing에서 발생하며, 데이터 속도 증가할 수록 Eye-diagram 축소 유발
- Physical length 보상만 할 경우 Electrical Delay 보정하지 못함. Electrical Delay 보정이 중요

[PCIe 6.0 2-connector add-in card topology]





- PCIe 6.0 2-connector 토폴로지에서 시뮬레이션 진행
- Electrical delay 보정이 Eye-diagram 성능이 가장 좋음
- PCIe 6.0의 Eye mask의 약 12% 개선 효과

3-19 : Intra-pair Skew Electrical Delay Compensation for PCIe 6.0 (2)

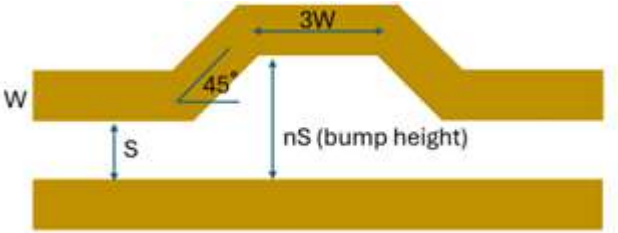
Effective Intra-Pair Skew

$$EIPS = \sum_{Nmin}^{Nmax} W(d \cdot df) \cdot |skew(f)| df$$

EIPS : intra-pair skew를 frequency domain에서 분석하여 단일 값으로 표현하는 개념
- 각 주파수 대역에서의 Attenuation, Phase shift, Dispersion 영향 고려 안됨
- PCB 기판의 유전율, loss, 도체 두께 등의 영향 반영 안됨
- 물리적 길이 보상을 Saw-tooth bump 등으로 하지만 EIPS값을 바로 적용하기 어려움

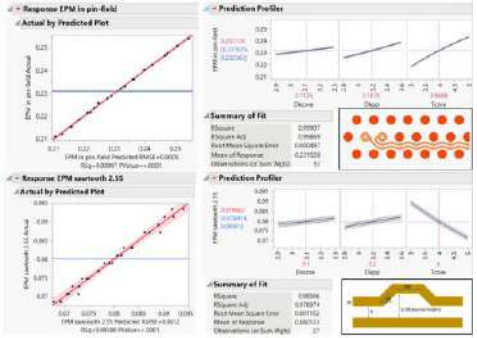
$$EPM = \frac{EIPS\ in\ ps}{skew\ in\ length\ in\ mil} \quad \& \quad CC = \frac{EPM\ of\ Source\ Structure}{EPM\ of\ Compensation\ Structure}$$

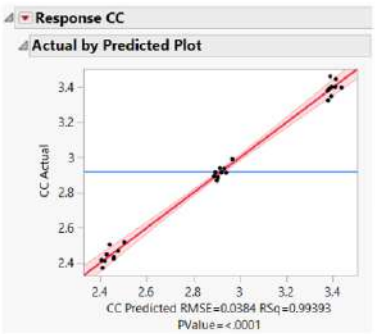
[Saw-tooth structure]

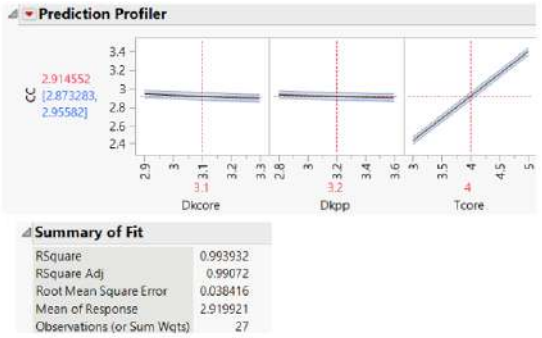


EPM(EIPS Per Mil) & CC(Compensation Coefficient) 개념 도입
- 단위 길이(mil)당 electrical delay 계산 방법 추가
- Saw-tooth 구조의 최적 길이를 결정하는 계수 도입

→ 어떤 skew 발생했을 때, 보상 구조를 얼마나 추가해야 하는지 계산하는 기준이 됨.







- 도출된 EPM, CC를 이용하여 Saw-tooth 구조 (3W2S, 3W2.5S)의 최적 보정 경로 설계 가능

3-20 : Intra-pair skew in 224G DAC cables, mitigation and operating environment (1)

Twinax DAC cable skew의 주요 원인
1) Conductor 중심 정렬 문제
2) 절연체 두께 변형 및 물성 차이
3) Shield 불균형
→ 제조 공정 정밀도가 skew에 직접적 영향

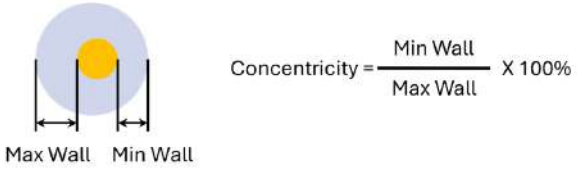


Figure 2: Definition of concentricity

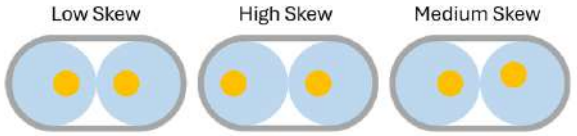


Figure 3: Examples of concentricity/eccentricity position and rotation

Figure 6: Longitudinal Wrap

Figure 7: Helical Wrap

Figure 8: Non-uniform tightness

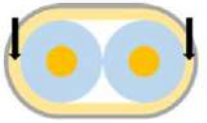


Figure 9: Deformation of Thickness

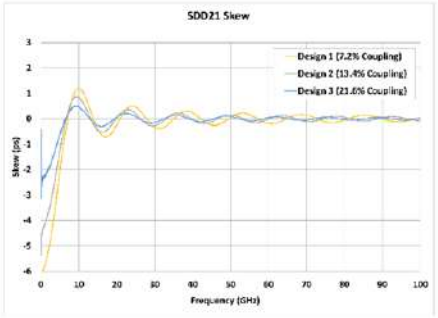


Figure 28: Skew vs Coupling %

Design	Coupling	TDT Skew
Design 1	7.2%	1.09ps
Design 2	13.4%	0.73ps
Design 3	21.6%	0.34ps

Figure 29: Skew vs Coupling %

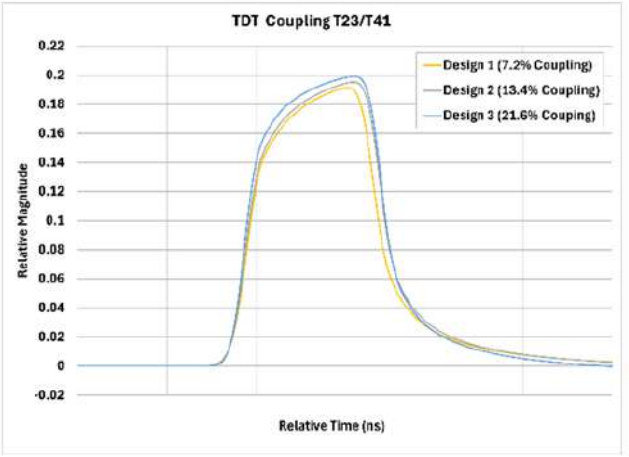


Figure 30: TDT Coupling for Figure 29

$$Percent\ Coupling = \frac{2 \cdot Z_{comm} - Z_{diff}/2}{2 \cdot Z_{comm} + Z_{diff}/2} \cdot 100$$

- Tight coupling → Skew 감소 효과 → 제조 공정의 한계로 20% 수준의 Coupling이 최적

3. DesignCon 2025 자료 소개

3-20 : Intra-pair skew in 224G DAC cables, mitigation and operating environment (2)

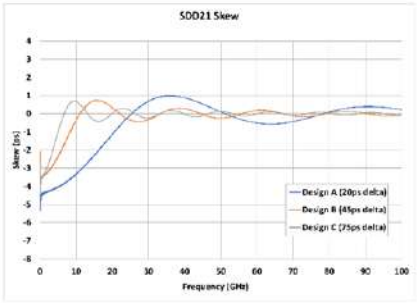


Figure 31: Frequency Skew vs Delay delta

Design	Diff to Com Mode delay delta	TDT Skew
Design A	20ps	1.80 ps
Design B	45ps	0.80 ps
Design C	75ps	0.56 ps

Figure 32: TDT Skew vs Delay delta

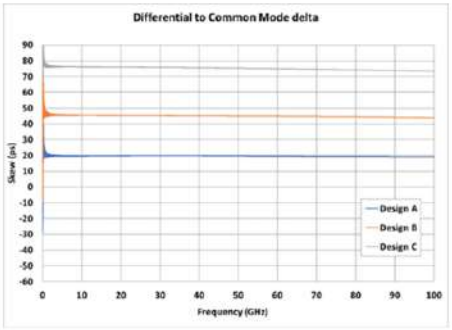


Figure 33: Delay delta for Figure 31/32

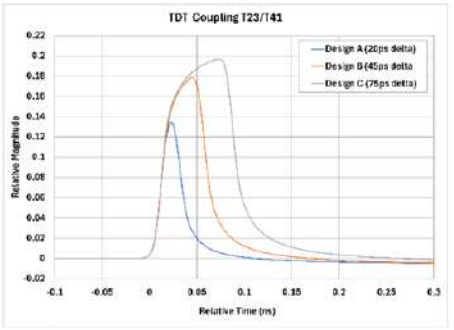


Figure 34: TDT Coupling Figure 31/32

- Differential to Common mode delay delta 값이 클수록 Frequency domain에서의 skew는 peak에 일찍 도달 후 감쇄

→ Time domain 에서의 skew 크게 감소

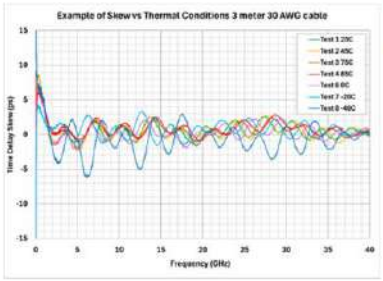


Figure 39: Skew vs Temperature

Temperature	TDT Skew
25 C	1.86ps
45 C	1.89ps
75 C	1.98ps
85 C	1.79ps
0 C	1.53ps
-20 C	1.28ps
-40 C	-1.20ps

Figure 40: TDT

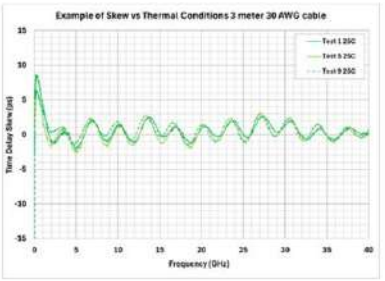


Figure 41: Skew thermal stability

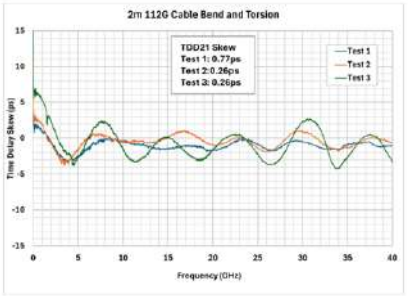


Figure 42: Skew with Bend & Torsion

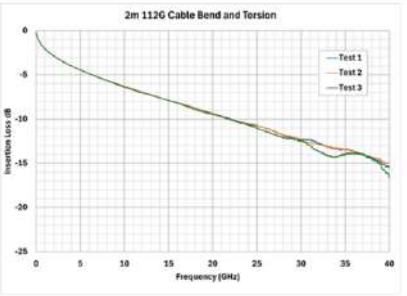


Figure 43: SDD21 Loss with Bend / Torsion

- 일반적으로 상온이나 고온 (25~80°C) 에서의 skew는 큰 문제 없음, 저온(-40°C) 에서는 재료 수축으로 인해 변화가 큼
- 단순한 Bending은 skew 변화가 적지만, 꼬임이 추가되면 skew와 insertion loss 증가

→ Cable의 설계 및 제조 정밀도에 영향을 많이 받음.

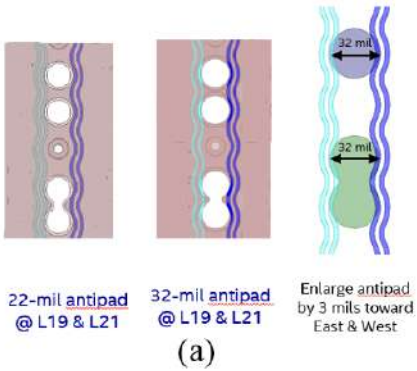
3-21 : Investigation of Pin Field Crosstalk Degradation due to PCB Manufacturing Variation (1)

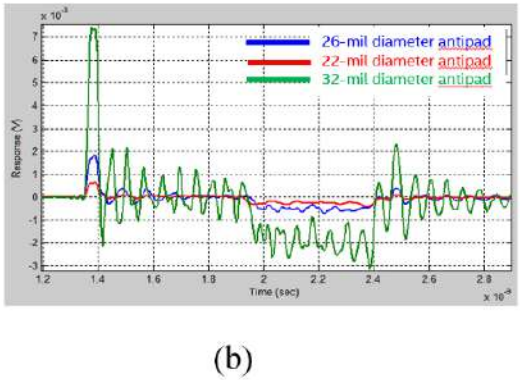
Crosstalk에 영향을 미치는 제조 및 설계 요인 (높은 pin 밀도, 인접한 신호 간 coupling 증가)

1) Antipad 크기 (Antipad 크기가 클수록 crosstalk 증가)
2) Differential pair trace 간 Alignment 문제 (1mil shift 4.5mV → 7.1mV)
3) Breakout trace를 따라 주기적으로 배치된 antipad의 크기와 개수 (antipad 크기가 작고 개수가 적을수록 감소)
4) PCB 제조 변동성 (PCB 제조사마다 편차 → 정밀 분석을 통해 시뮬레이션에 반영)

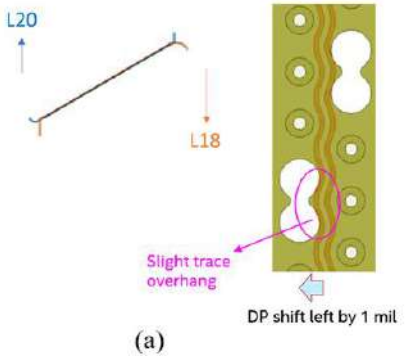
→ 제조 변동성을 고려해 시뮬레이션과 측정값 간 불일치 문제 해소 필요

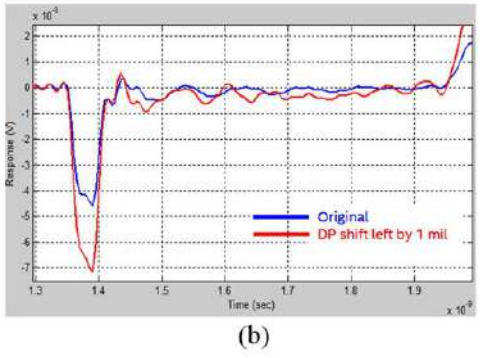
[Antipad size 변화에 따른 crosstalk level simulation]



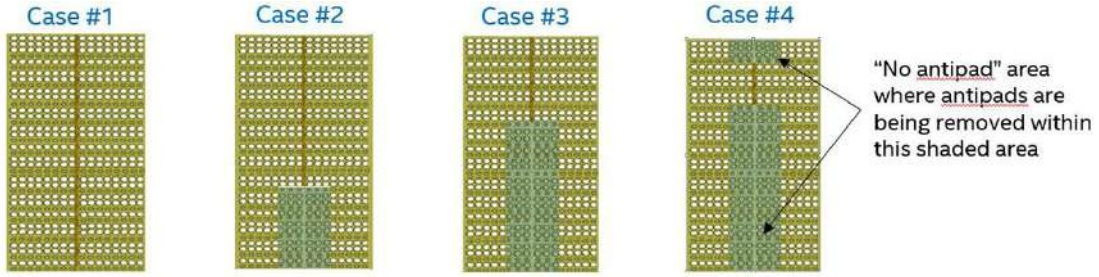


[Differential pair trace 간 alignment 변화 simulation]





[Breakout trace를 따라 배치된 Antipad 개수 변화에 따른 4가지 경우의 simulation 결과]



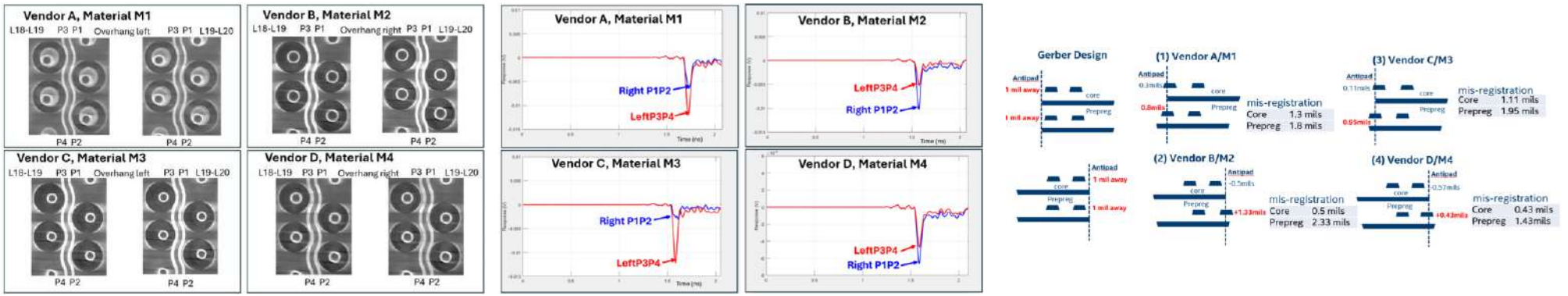
Coupling Type	Figure	Case Number	antipad diameter		# of antipads are removed	Remaining antipads vs. original	TDFEXT, Tr = 40 ps (0-100%)	
			No antipad	w/antipad			1st Peak, mV	Ratio (vs. #1)
L18-L20 broadside		Case #1	26	26	0	100.0%	8.526	-
		Case #2	0	26	18	77.5%	6.329	74.2%
		Case #3	0	26	45	43.8%	3.587	42.1%
		Case #4	0	26	69	13.8%	1.578	18.5%

3. DesignCon 2025 자료 소개

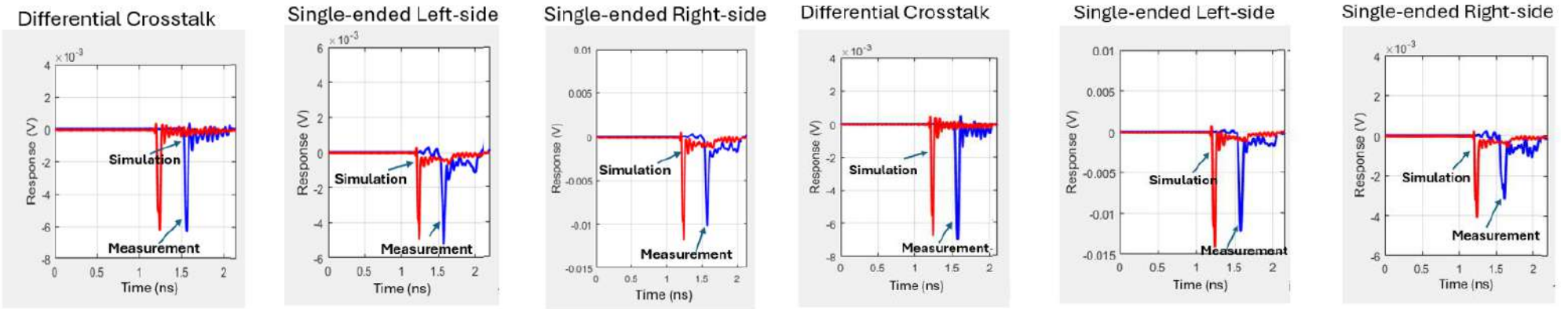
3-21 : Investigation of Pin Field Crosstalk Degradation due to PCB Manufacturing Variation (2)

High Resolution 3D X-ray를 이용한 PCB 분석 후 Simulation에 반영
→ via 위치, antipad 크기, core와 prepreg 두께 등 제조사별 편차 발생
→ 분석된 공정 편차를 Simulation 에 다시 적용하여 해석하면 측정결과와 잘 일치함을 확인

[4개의 PCB 제조사에서 제작한 PCB의 3D X-ray, 측정결과, Layer mis-registrations]



[분석된 공정 편차 반영한 Simulation 결과와 측정결과 비교]

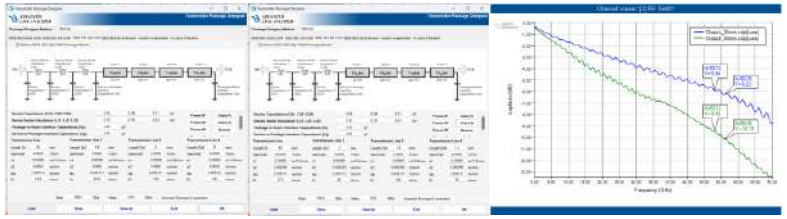


3-22 : Next Generation 224 Gbps-PAM4 Chip-to-Chip/MR SERDES, Package, Channels, and Link Simulation and Analysis (1)

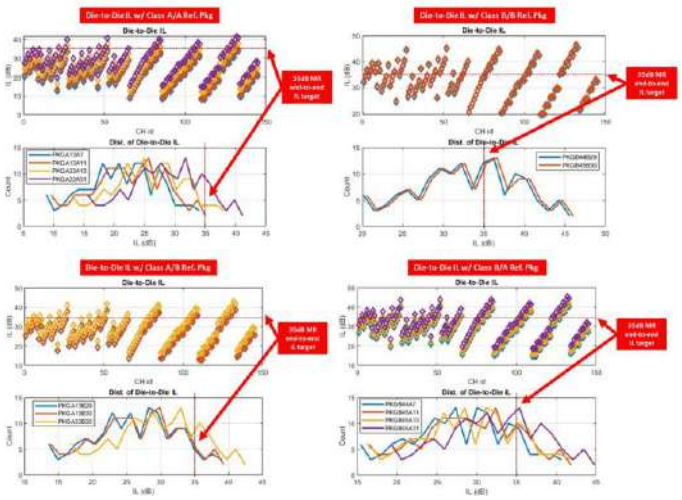
IEEE 802.3dj & OIF-CEI-224G

- CLASS A ("loss optimized") : maximum package I.L 6dB(Ethernet) or 6.2dB(OIF-CEI), 33mm
- CLASS B ("radix optimized") : maximum package I.L 9.5dB(Ethernet) or 10dB(OIF-CEI), 45mm

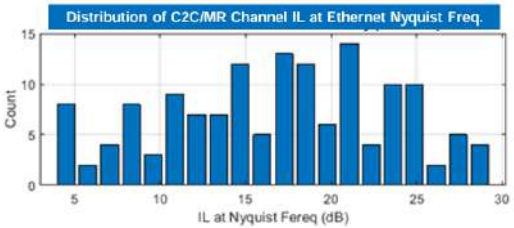
[200+ Gbps Reference Package model]

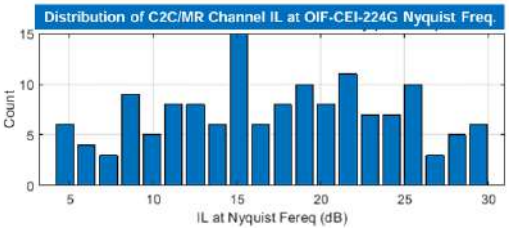


[bump-to-bump IL of MR test channel at 212.5 Gbps]

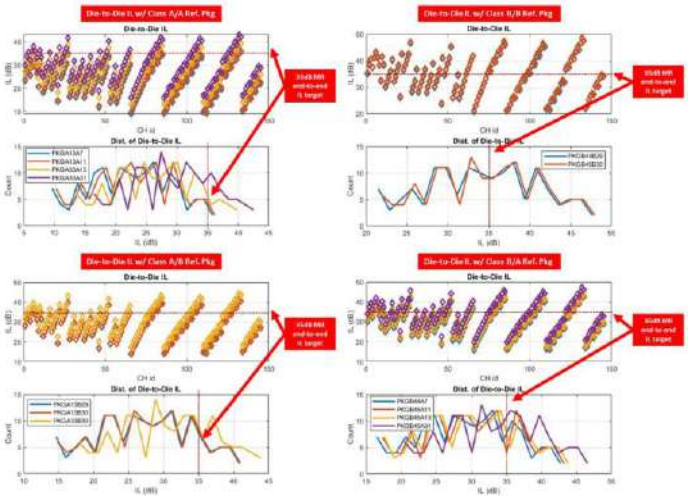


[Distribution of C2C/MR(Medium Reach) Channel IL]





[bump-to-bump IL of MR test channel at 212.5 Gbps]



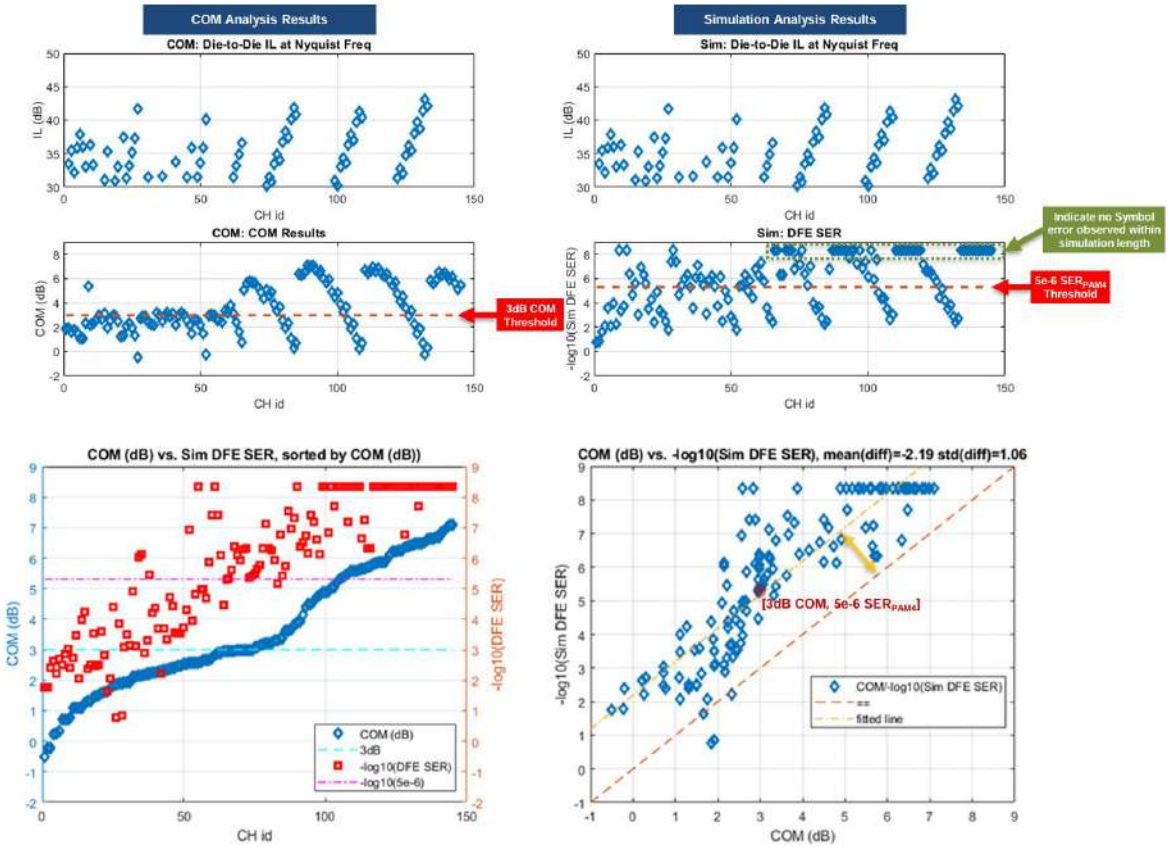
- Package IL은 Class A 에서 ~12dB, Class B에서 ~19dB 소모
- 35dB IL limit target은 Class A에서는 ~90% 정도이지만, Class B에서는 50% 수준임

3-22 : Next Generation 224 Gbps-PAM4 Chip-to-Chip/MR SERDES, Package, Channels, and Link Simulation and Analysis (2)

- Waveform-Domain Analysis 를 통해 실제 데이터 패턴에서 발생하는 jitter 및 non-linear distortion 반영

→ 실질적인 BER 평가 가능, 그러나 COM Analysis 도 상당한 정합성을 갖음

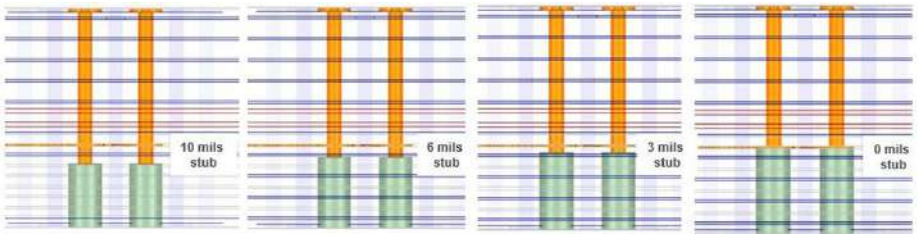
- COM≥3dB 인 채널에서는 Waveform-domain 분석에서도 양호한 Eye-opening과 낮은 BER 확인됨
- COM≤3dB 일 경우 Waveform-domain 시뮬레이션 추가적으로 필요



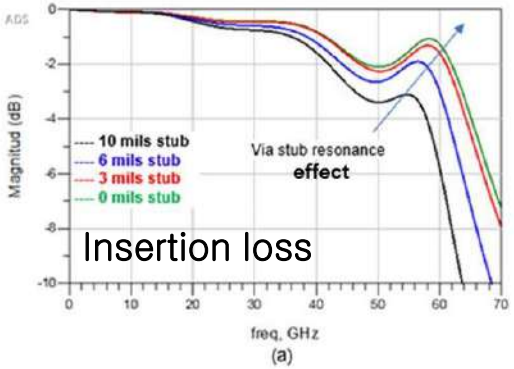
[OIF-CEI-224G-MR COM results and link simulation SER result of 145 IEEE 802.3dj CR/KR/C2C test channels]

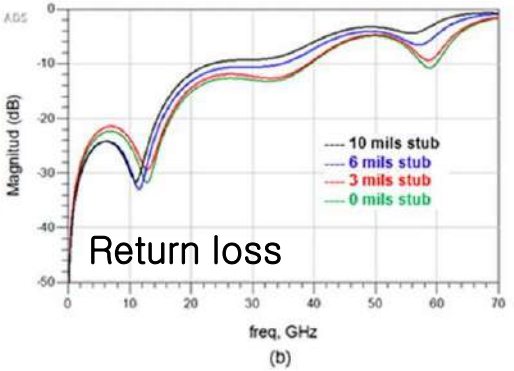
3-23 : Solving a Key Signal Integrity Bottleneck Issue to Continue Scaling PCIe 7.0 over Copper Channels (1)

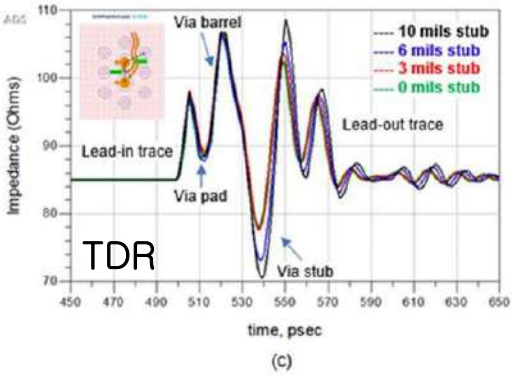
[Pin field via stub 길이 변화에 따른 3D model 과 simulation 결과]

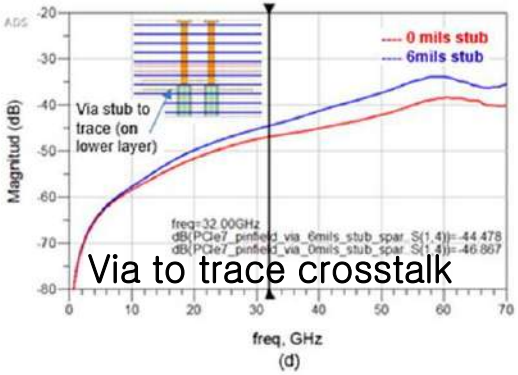


Stub Length (mils)	Impedance (Ohms)	Insertion Loss (dB) @ 32 GHz	Return Loss (dB) @ 32 GHz
10	70.5	0.79	9.2
6	73.3	0.62	10.6
3	78.6	0.46	12.6
0	79.0	0.42	13.2









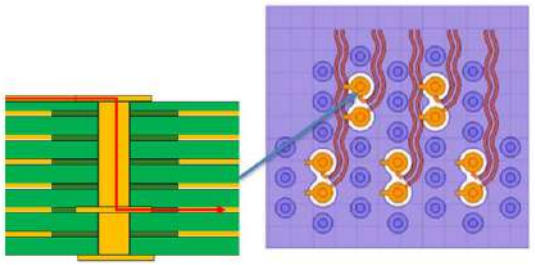
- Pin field via stub의 길이가 짧아지면 (128G Nyquist frequency = 32GHz)

1) Insertion loss의 감소 + Stub로 인한 공진이 관심대역 밖으로 이동효과
2) Return loss의 감소
3) 임피던스의 via stub로 인한 capacitive dip 감소
4) Via to trace coupling의 감소 → Crosstalk 감소

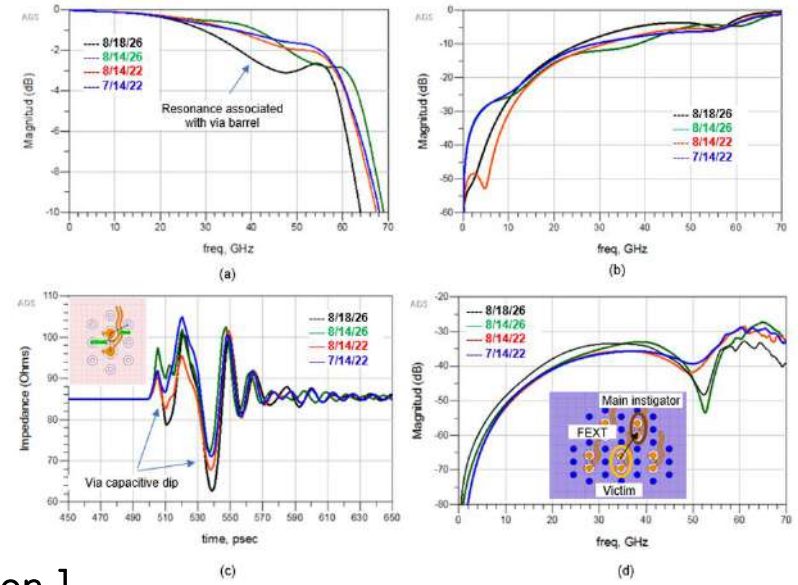
→PCIe7.0 속도에서 10mil의 via stub 길이를 3mil 정도까지 줄이면 좋고, 3mil~0mil 까지는 더 이상 큰 이점이 없음

3-23 : Solving a Key Signal Integrity Bottleneck Issue to Continue Scaling PCIe 7.0 over Copper Channels (2)

[3D model via stack geometry and simulation cases]



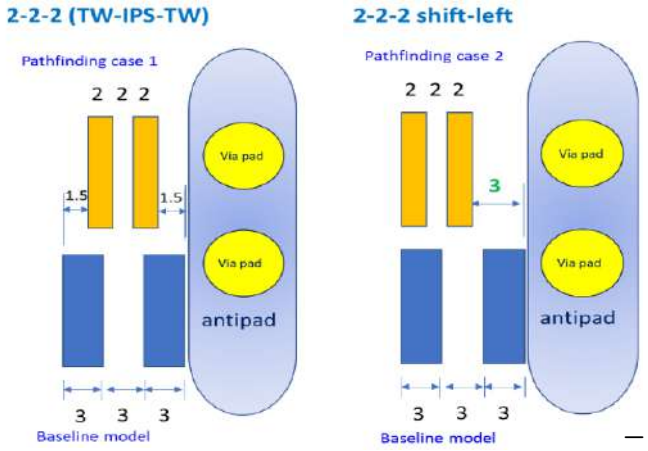
Case	Drill Size (mils)	Pad Size (mils)	Anti-pad Size (mils)
1	8	18	26
2	8	14	26
3	8	14	22
4	7	14	22

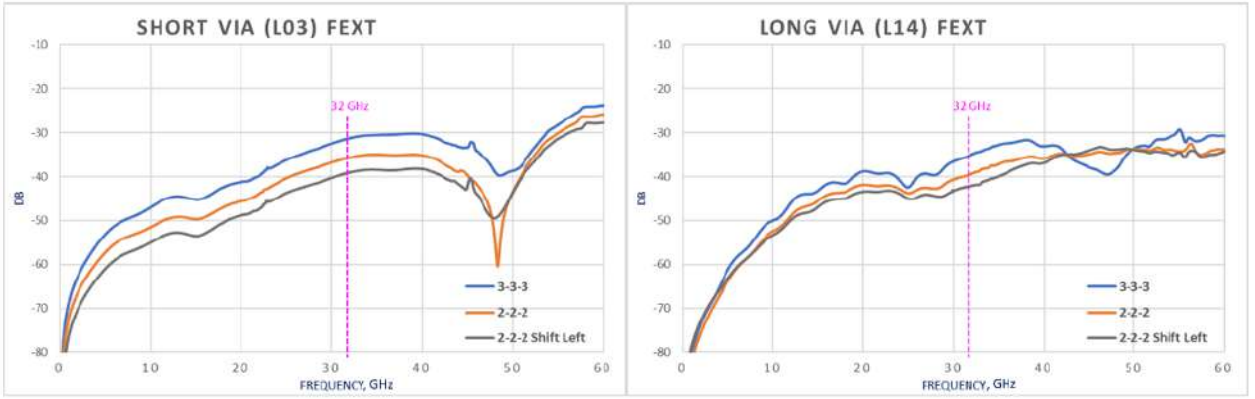


- Via pad와 anti-pad의 크기 최적화 필요
- Via pad와 anti-pad 크기가 줄어들면 FEXT도 낮아짐
- Drill 사이즈를 줄이는 것은 성능상 이점 거의 없음

→ 다양한 parameter들이 있고 매우 민감하게 동작함

[Pin field routing 구조 비교 simulation]

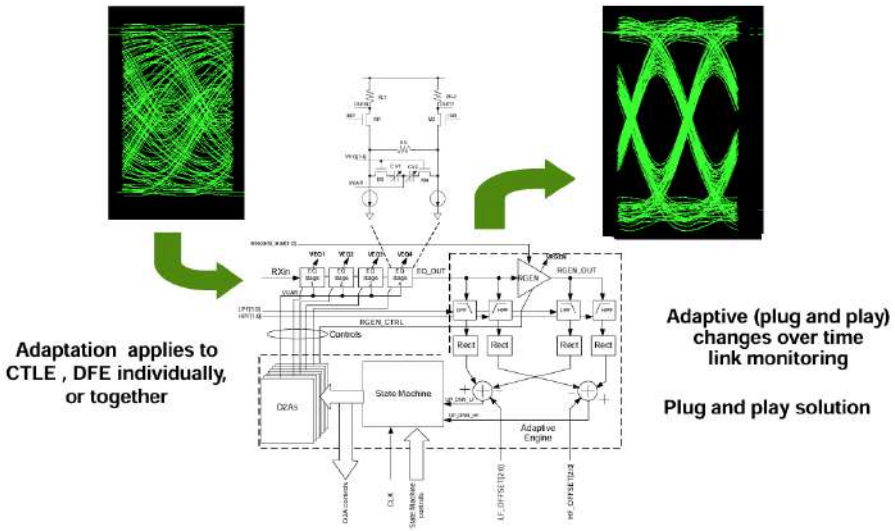




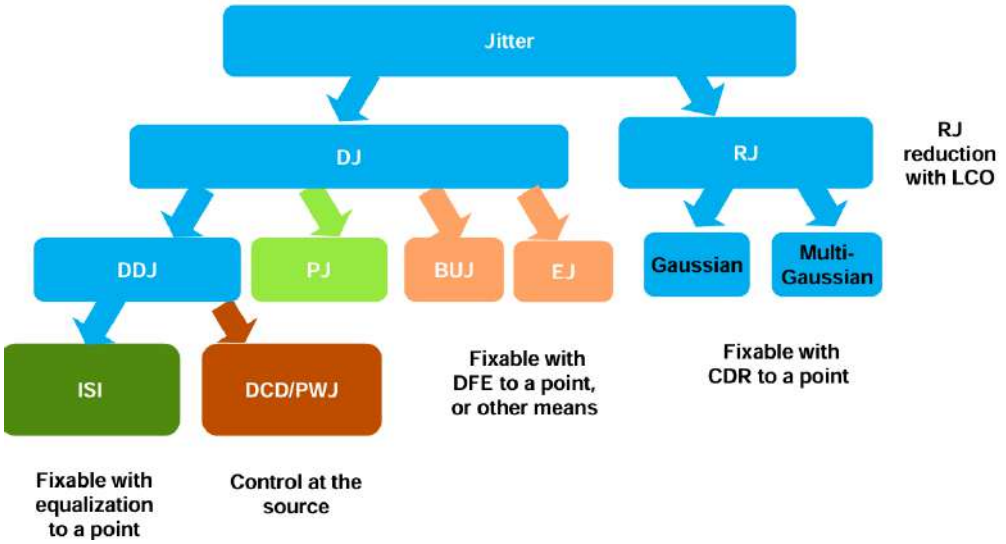
- Intra-pair 간격을 줄여 Differential 쌍 사이의 간격을 확보 -> FEXT 개선 가능

3-24 : Design and Verification for High-Speed I/Osat 10 to 112 to 224 Gbps and beyond with Jitter, Signal Integrity, and Power Optimized (1)

- 224Gbps 고속 I/O 설계는 Jitter 분석, Equalizer 전략, 계측 기술, 시뮬레이션 정확도 향상 등 통합적 접근이 필요



Flexible PLD interface to enable link monitoring usage



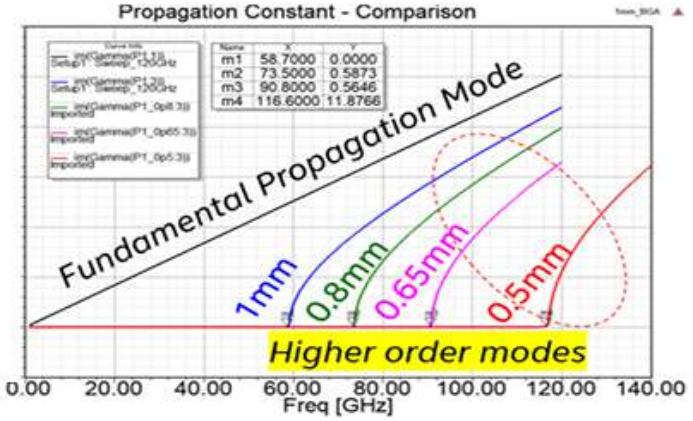
- RJ(Random Jitter)의 경우 본질적으로 제거 불가함. 통계적 모델링과 BER 기반의 설계 필요
- DCD(Duty Cycle Distortion) 와 PWJ(Pulse Width Jitter) 같은 High/Low Pulse의 비대칭성으로 인한 문제 제어 필요
- Jitter의 종류에 따라 EQ 설정, Power 설계, Signal path 최적화 등 다양하게 대응 필요 → Jitter mitigation 전략 필요

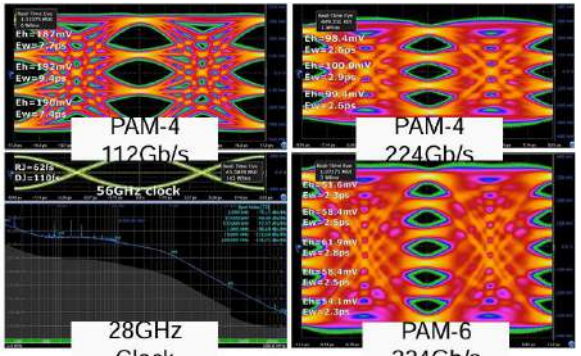
3. DesignCon 2025 자료 소개

3-24 : Design and Verification for High-Speed I/Osat 10 to 112 to 224 Gbps and beyond with Jitter, Signal Integrity, and Power Optimized (2)

- Package BW depends on ball pitch
  - 112G (PAM4): ≤ 1mm
  - 224G (PAM4): ≤ 0.8mm
  - 448G (PAM4): ≤ 0.5mm
- **Package ball pitch of <= 0.5 mm is available today**

[448 Gbps Package]





Cut-off frequency of BGA ball pitch

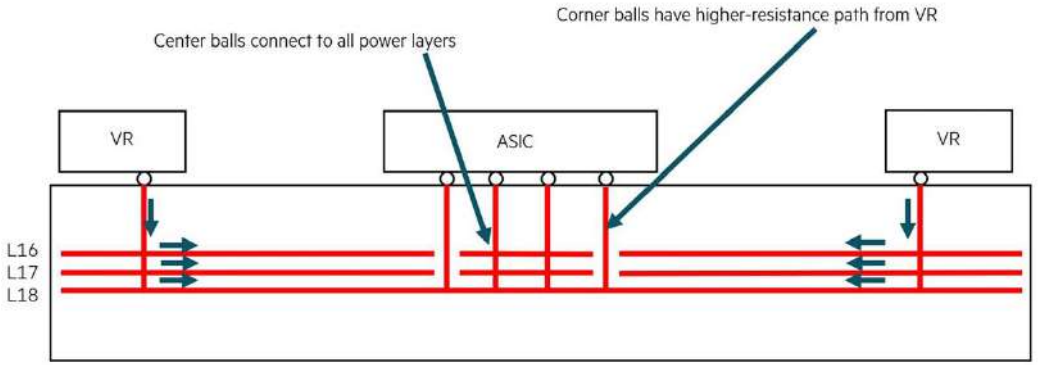
BGA pitch	1.0mm	0.8mm	0.65mm	0.5mm
Cutoff Frequency	58GHz	72GHz	90GHz	115GHz

	224G		448G			
Modulation	PAM4	PAM6	PAM4	PAM6	PAM8	PAM16
Nyquist Freq, GHz	56 GHz	44.8 GHz	112 GHz	89.6 GHz	74.67 GHz	56 GHz

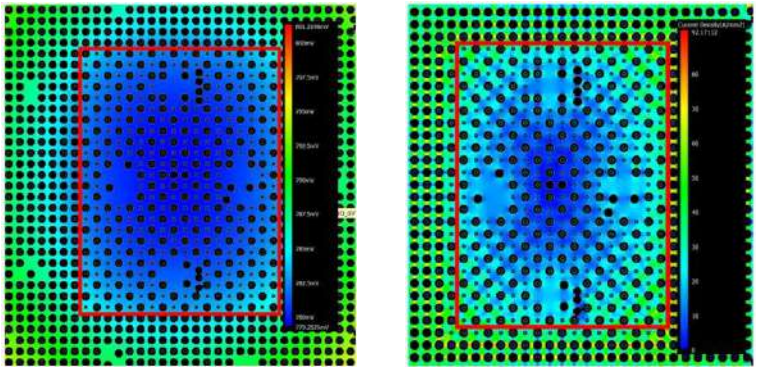
- PAM4는 OIF-CEI-56/112/224G, Ethernet 53/106/212G에서 잘 동작했으며, 56Gbps 이후 일반적인 modulation 방식
- 0.5mm 이하 ball pitch, advanced materials/stack-up(e.g., skip layer)로 448Gbps-PAM4 구현 가능

3-26 : Balancing Current Density to High-Power ASICs in Lateral Power Delivery Designs (1)

- 고속 ASIC의 전력 소비 증가로 PCB에서 Current density 불균형 문제 발생 (corner via에 전류밀도가 높음)
- Power via 전류 과부하는 Overheating & Electromigration 문제 유발
- 균형 잡힌 전류 분포를 유지하는 것은 PCB 및 package의 전력 손실을 최소화하고 신뢰성을 향상시킬 수 있음



[Concept diagram of partially disconnected coner vias]



[VDD power plane voltage gradient & current density]

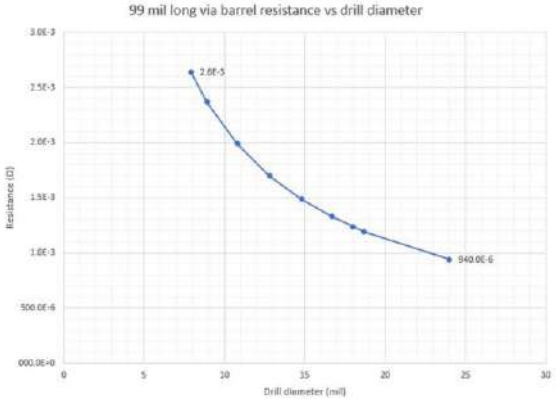
- Corner via를 여러 Power plane 중 제일 먼 layer와 연결하는 방법 제안
- Corner via feeding되는 path의 저항을 증가시켜 전류를 줄이는 방식
- 이 경우 나머지 power rail에 대한 물리적 도체 길이 증가 → 일부 decoupling capacitor 에 대한 inductance와 resistance 증가 → corner에 있는 ASIC ball field의 PDN 증가되는 단점이 있을 수 있음

3. DesignCon 2025 자료 소개

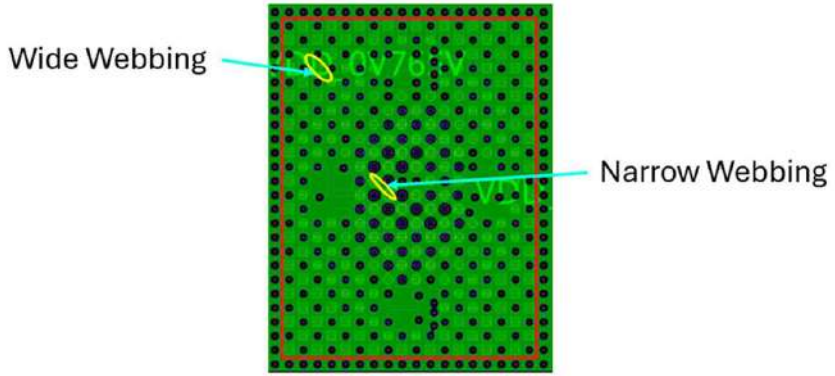
3-26 : Balancing Current Density to High-Power ASICs in Lateral Power Delivery Designs (2)

- Via drill의 diameter를 줄여 저항 높이는 방법 사용 가능 → 부가적으로 Webbing 너비를 증가시킬 수 있음

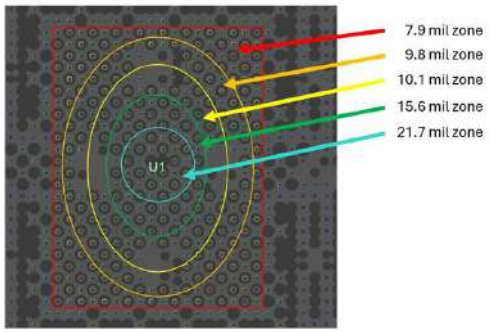
[Typical via barrel resistance]

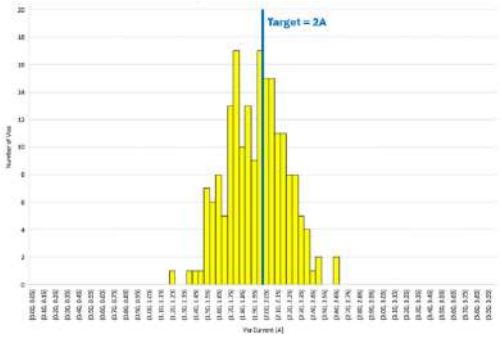


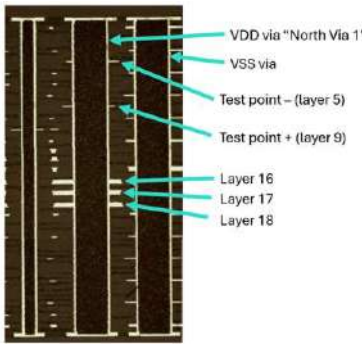
[Webbing width increase with smaller drills and antipads]

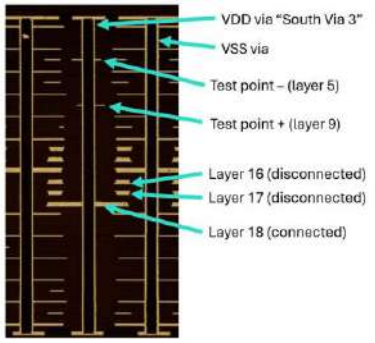


- 불균일한 전류밀도를 갖는 power plane 형상은 lumped equivalent circuit으로 변환하기 어려움
- PCB artwork, Package artwork, die bump current map이 있어야 2차원 DC Simulation 가능







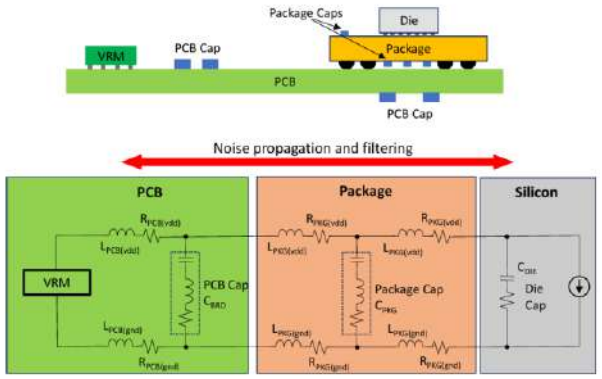


- Via의 diameter를 영역을 나누어 바깥쪽으로 갈 수록 작게 하며 corner via들은 가장 먼 power plane 과 연결
- Via의 diameter를 줄이는 방식과 corner via를 특정 Power plane과 연결하는 방법을 통해 적절한 전류 분배 가능

3. DesignCon 2025 자료 소개

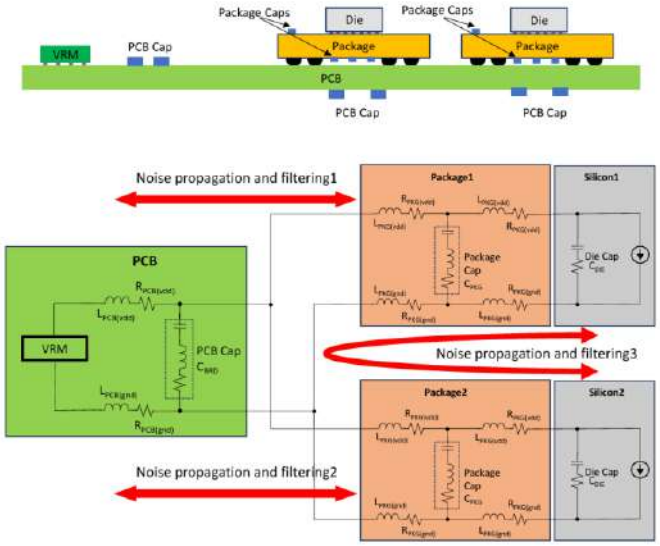
3-27 : Determining the Requirements, Die vs. Package vs. Board: Multi level Power Distribution Network Design

- ❖ 최근 칩(Die), 패키지, 보드(PCB)의 전력 요구 조건이 상이해짐에 따라, PI를 보장하기 위한 PDN 설계가 복잡해짐
- ❖ 기존 Target Impedance 기반 PI 설계 방식이 아닌, 각 패키지 및 보드레벨과 위치에 최적화된 PDN 설계가 필요함



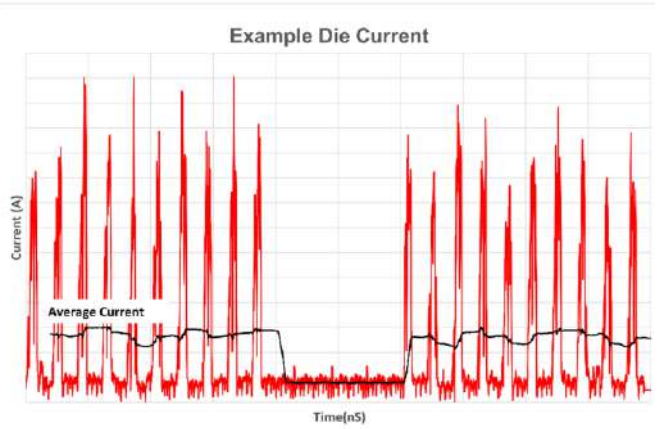
POL(Single-load PDN)

→ 단일 부하라서 Target impedance 기준을 적용하기 쉬움



Multi-Load PDN

→ 각 부하마다 위치,거리,캡 배치가 달라 임피던스 경로가 달라짐



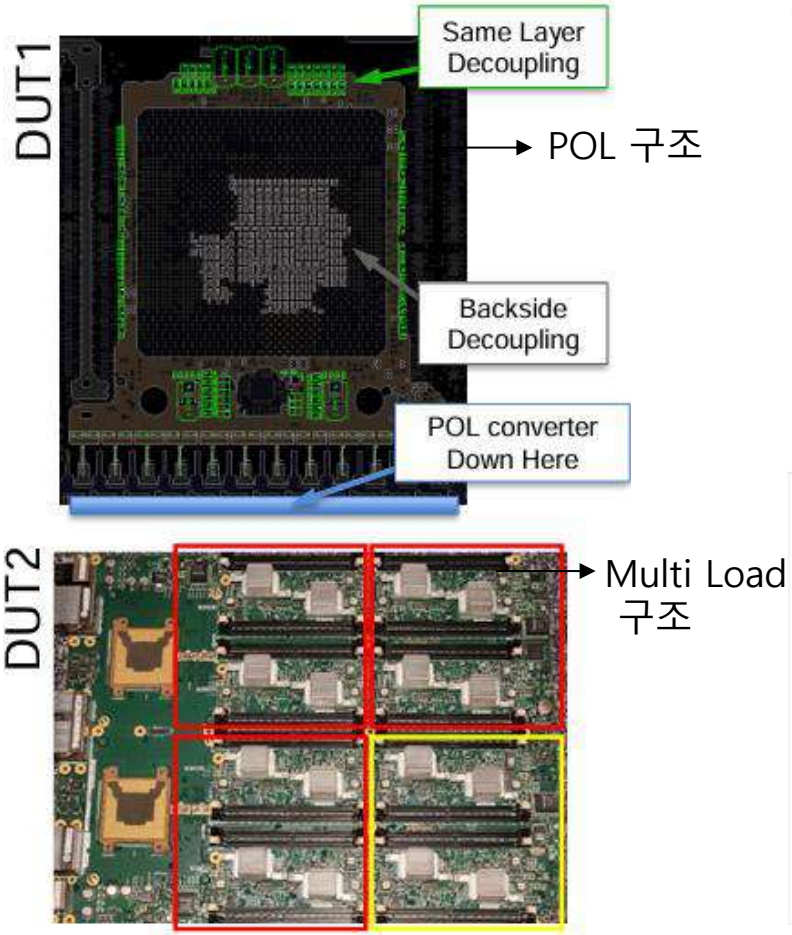
다이 레벨 전류 특성

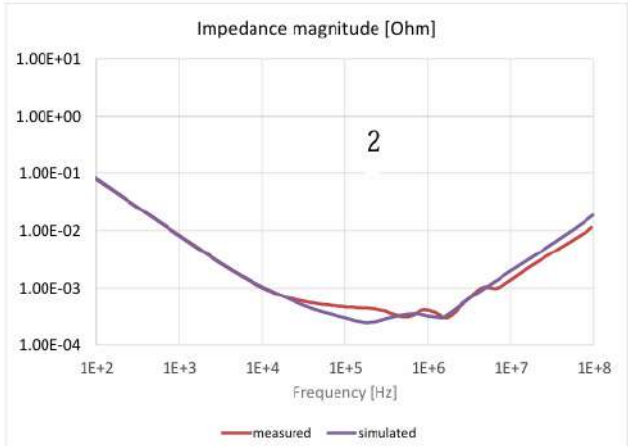
→ 고속 로직 동작 시 높은 피크 전류가 발생하여, PDN에서 빠르게 공급되지 않아 전압 강하 및 PI 문제 발생

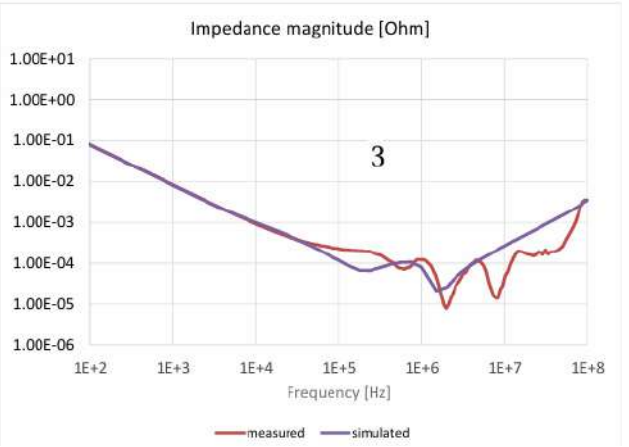
3. DesignCon 2025 자료 소개

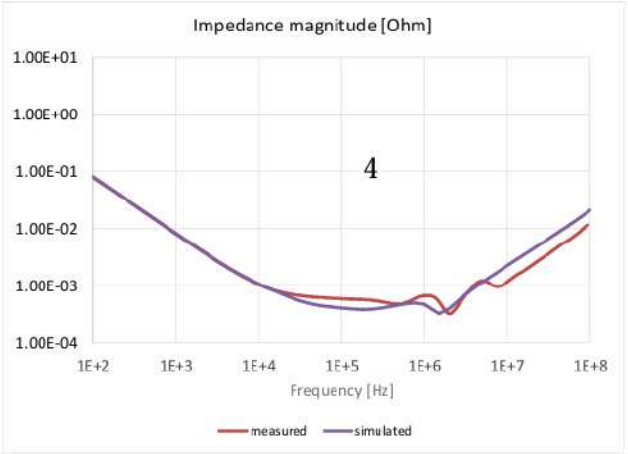
3-27 : Determining the Requirements, Die vs. Package vs. Board: Multi level Power Distribution Network Design

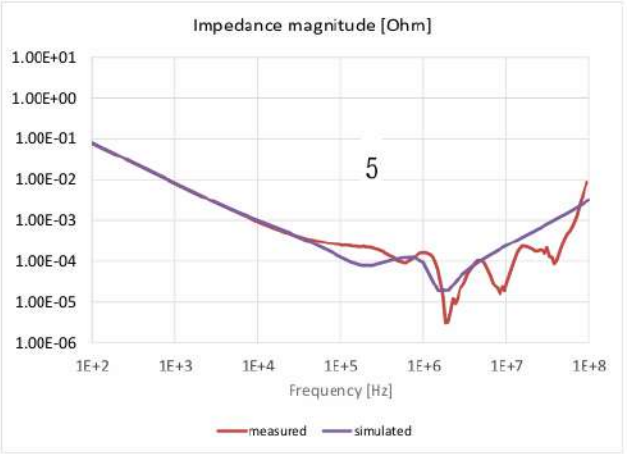
❖ PDN 설계는 flat target impedance 기준이 아닌 위치/주파수 기반 맞춤 설계가 필요함을 실측 및 시뮬레이션으로 검증함



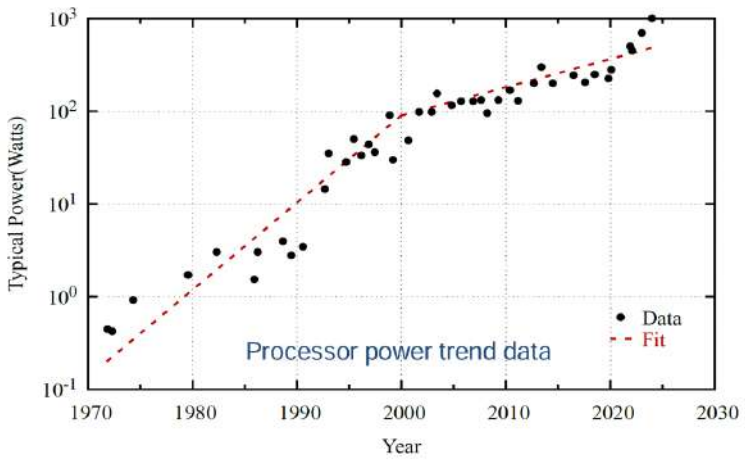




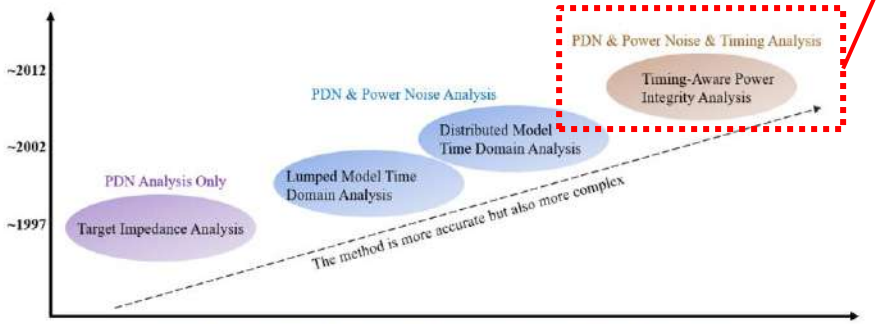




3-28 : High Efficiency Timing Aware Power Integrity Analysis Methodology for Digital Integrated Circuits



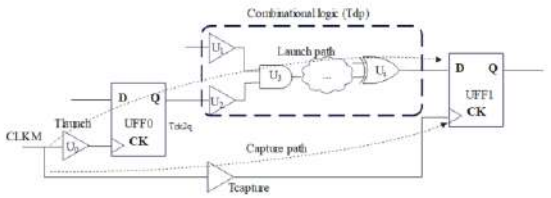
- The power consumption of the processor has been increasing rapidly
- The importance of PI is becoming increasingly prominent and requires more attention



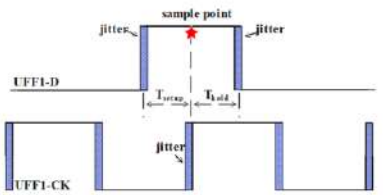
The development history of power integrity methodology

- The development of PI analysis methods has gone through three stages, namely target impedance analysis, transient power noise analysis, and time-aware PI analysis
- Timing-Aware Power Integrity Analysis is the new approach method we introduced here

Timing-Aware Power Integrity Analysis



Clock and data path



Sampling jitter

- Timing-aware power integrity analysis is a method that evaluating power integrity by timing path analysis
- To evaluate the supply power integrity quality that we focus on, we should analyze all the timing paths in the supply power domain to confirm whether the timing margin is enough

➢ 기존 PI 분석 방법은 Target impedance analysis, Transient Simulation Analysis Based Lumped model & Distributed Model 로 발전

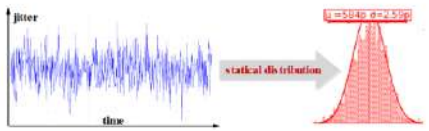
➢ 기존 방법론과 Timing Aware Power Integrity Analysis의 장점
- Accurate Timing Margin Assessment
  PSIJ (Power Supply Induced Jitter), DCD (Duty Cycle Distortion), and RJ (Random Jitter) 고려
- Dynamic Jitter Library (DJL) Utilization
- Power Noise Impact Quantification

3-28 : High Efficiency Timing Aware Power Integrity Analysis Methodology for Digital Integrated Circuits

➢ Timing Aware Power Integrity Analysis는 아래 3가지를 고려하여 과도한 설계 방지 및 비용 절감

- Accurate Timing Margin Assessment
  PSIJ (Power Supply Induced Jitter), DCD (Duty Cycle Distortion), and RJ (Random Jitter)
- Power Noise Impact Quantification 고려
- Dynamic Jitter Library (DJL) 획득

Random Jitter - $RJ^{k,v}_{Setup}$ & $RJ^{k,v}_{Hold}$



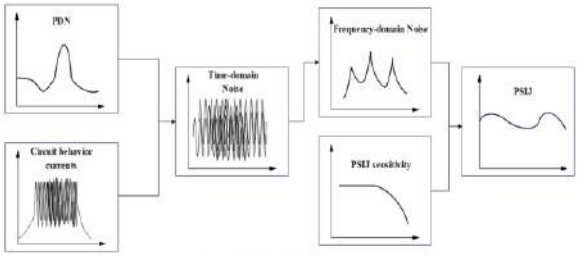
Sample of RJ

$$RJ^{k,v}_{Setup||Hold} = \sqrt{\sum_{i=0}^{n-1}\left(RJ_i^{k,v}\right)^2}$$

Note:
n represents the total number of standard cells in the timing path

- RJ is caused by thermal noise of semiconductors and generally Gaussian-distributed
- This result of total RJ is peak-to-peak amplitude, we need to transform it to RMS value because RJ is unbounded

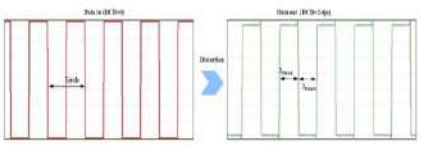
Power Supply Induced Jitter - $PSIJ^{k,v}_{Setup}$ & $PSIJ^{k,v}_{Hold}$



PSIJ Evaluating Flow

- PSIJ is the jitter caused by power supply noise
- We compute PSIJ with the inputs of noise spectrum on supply rail and jitter sensitivity of circuit

Duty Cycle Distortion - $DCD^{K,v}_{Hold}$



Waveform of DCD

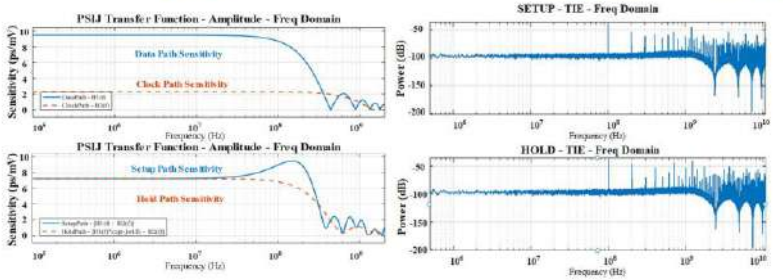
$$DCD^{v} = \frac{T^{v}_{PulseL} - T^{v}_{PulseS}}{2}$$

$$DCD^{k,v}_{Hold} = \sum_{i=0}^{n-1} DCD_i^{k,v}$$

Note:
T^{v}_{PulseL} represents the longer pulse in one cycle
T^{v}_{PulseS} represents the shorter pulse in one cycle

- We stimulate a clock code pattern to the circuit, then monitor the output to get the DCD jitter

Power Supply Induced Jitter - $PSIJ^{K,v}_{Setup}$ & $PSIJ^{K,v}_{Hold}$



- A sample of PSIJ result is showed, left figure is the jitter sensitivity curve, right figure is the PSIJ in frequency domain
- It is the difference between STA and TAPIA, TAPIA consider the frequency response characteristics of PI, while STA reserve a fixed margin for PI

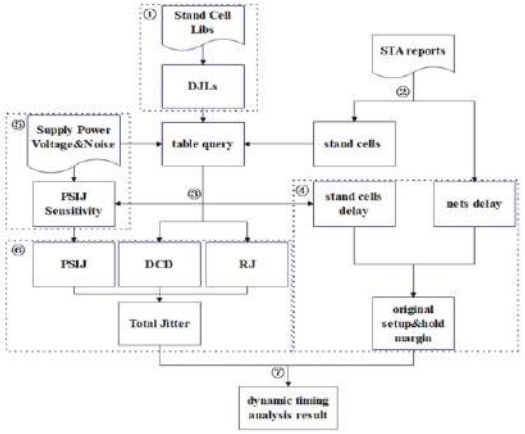
3-28 : High Efficiency Timing Aware Power Integrity Analysis Methodology for Digital Integrated Circuits

➢ 결론

- Timing Aware Power Integrity Analysis Methodology는 power noise가 디지털 회로에 미치는 영향을 평가하고, Dynamic Jitter Library (DJL)를 활용하여 타이밍 성능을 재구성
- Timing Aware Power Integrity Analysis Methodology는 과도한 설계를 방지하고 비용을 절감을 할 수 있음을 확인

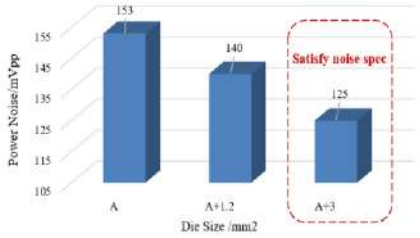
Overall flow

- Step 1 Get corresponding DJLs
- Step 2 Obtain all standard cells in the timing paths and all nets delay from static timing analysis (STA) reports
- Step 3 Get the PSIJ sensitivity, DCD, RJ and delay time from DJLs
- Step 4 Calculate the original setup and hold time margin without considering the effect of jitters
- Step 5 Calculate the PSIJ
- Step 6 Calculate the total jitter
- Step 7 Evaluate the final dynamic timing analysis result.

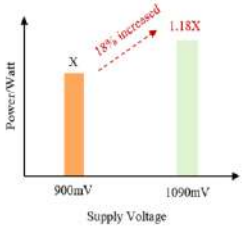


Overall flow diagram

Benefits Over Traditional Methods



Power noise reduced with more on die decap



More power is consumed when supply voltage increased

- The approach of TAPIA can avoid over design and reduce product costs

3. DesignCon 2025 자료 소개

3-29 : Power Delivery Strategies for AI and Data Center ASICs: Horizontal vs. Vertical

➢ AI 및 데이터 센터의 전력 수요 증가
- AI 기술 발전으로 인해 데이터 센터의 전력 소비가 급증
- 데이터 센터는 소규모 도시보다 더 많은 전력을 소비할 수 있으며, Google, Amazon (AWS), Microsoft, Oracle과 같은 기업들은 데이터 센터에 전력을 공급하기 위해 원자력 발전에 투자

News about AI in Data Centers

- *Google*, *Amazon (AWS)*, *Microsoft*, and *Oracle* are all investing in Nuclear Power to power their data centers
- *Oracle* is building a gigawatt data center powered by 3 small nuclear reactors
- A gigawatt data center using 85% of its peak demand ≈ 710,000 U.S. households or 1.8 million people
  - Implies data centers will consume more power than small cities

Source: Data centers powering AI could use more electricity than entire cities

An Amazon Web Services data center in Ashburn, Virginia, US, on Sunday, July 28, 2024.
Nathan Howard | Bloomberg | Getty Images

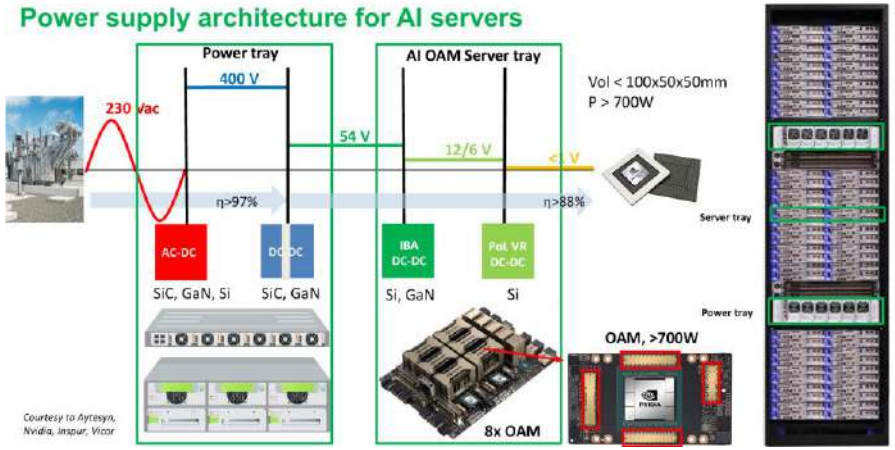
The Power Demands of AI in Data Centers

- **According to Goldman Sachs:**
  - ChatGPT query needs ***~10x*** as much electricity to process a Google search
  - By 2028, it is expected for AI to represent *~19% of the data center power demand*
- At CES 2025 - Nvidia launched the ***Blackwell GPU***
- Nvidia DGX B200 chassis with QTYx8 B200 Blackwell GPUs will consume roughly ***14.3kW!!***
  - That means ***60kW*** of rack power and thermal headroom to handle

Source: AI is poised to drive 160% increase in data center power demand | Goldman Sachs

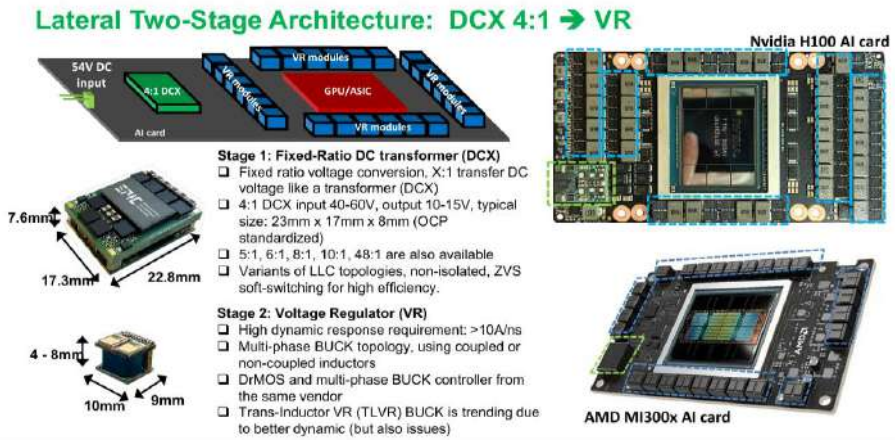
Source: nvidia.com

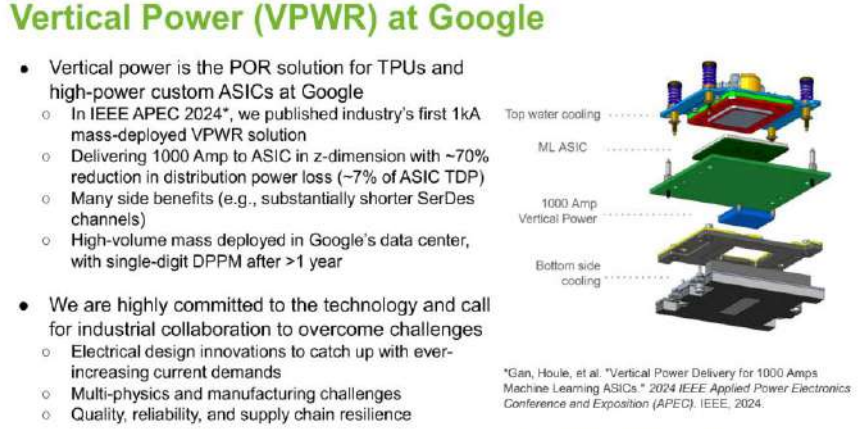
Power supply architecture for AI servers



3-29 : Power Delivery Strategies for AI and Data Center ASICs: Horizontal vs. Vertical

➢ Lateral Power Delivery(Horizontal) vs Vertical Power Delivery(Vertical)





	Lateral Power Delivery(Horizontal)	Vertical Power Delivery(Vertical)
장점	기존 기술 활용 가능 비교적 간단한 구현	전력 손실 감소 및 효율 증가 높은 전력 밀도 물리적 거리가 줄어짐으로써 향상된 dynamic response
단점	전류 요구량이 증가함에 따라 전력 손실 증가 PCB 두께 증가 및 신호 무결성 저하 냉각 문제 발생 Decoupling capacitor 배치 제한	맞춤형 모듈 필요로 인한 비용 증가 제한된 전류 용량 냉각 문제 VRM 제어 루프 안정성 문제 높은 주파수에서의 crosstalk 증가 신뢰성에 대한 우려

3-29 : Power Delivery Strategies for AI and Data Center ASICs: Horizontal vs. Vertical

- Vertical Power Delivery(Vertical) 고려하는 이유
  - I^2R Losses 감소
  - 양면 냉각(Double-sided Colling)
  - VRM 제어루프의 안정성 등

Benefits

Possibly reduce I^2R losses

Concerns

Cooling both sides of board

Vertical current increased crosstalk

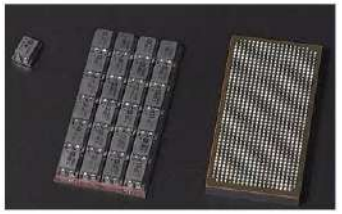
Higher density reliability/efficiency

VRM control loop stability

Limited current, room for growth

Vertical Reduces I^2R Losses

LTM9790 Vertical Power Delivery Module



Vertical and Lateral Power Solutions for AI Systems, Data Centers | Analog Devices

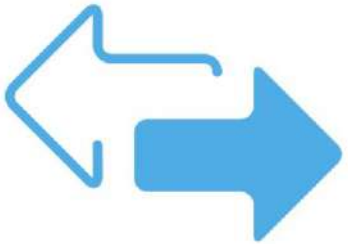
Does it? This is very difficult to say since there is little, if any, data provided for any of the vertical solutions currently on the market (though in secret).

The trend for lateral parts is the efficiency declines rapidly with reduced size.

Double-Sided Cooling

Unless the board is immersion-cooled, cooling manifolds are required on both sides of the PCB, adding cost, weight, and complexity.

The cooling could be achieved through the board and out through the ASIC, but this will make the ASIC run even hotter than it already does.



VRM Control Loop Stability

Assume a 33uΩ, 1500A, 16 phase board switching at 1MHz. Further assuming an aggressive 150kHz control loop bandwidth.

The capacitance at the aggregate module must be >32mF or 2mF/module. ESR must be below 1mOhm per bulk capacitor. How can this be achieved?

A plane inductance of 1nH per bulk capacitor is required. How can this be achieved?

3. DesignCon 2025 자료 소개

3-30 : Thermal Analysis and Optimized Design for Power Ground Vias of PMIC in DDR5 DIMM

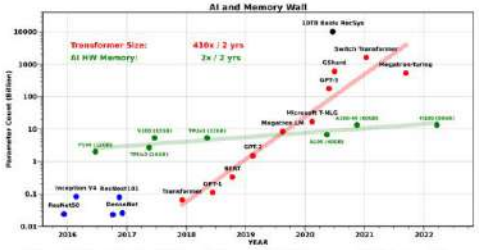
➢ Introduction & motivation

- AI 서버 및 데이터 센터에서 DRAM 수요가 폭발적으로 증가
- DDR5 DIMM부터는 안정적인 전원 공급을 위해 PMIC가 DIMM의 PCB에 직접 장착
- PMIC의 출력 전류 증가는 PMIC 및 전원 인덕터의 전력 소모를 증가시켜 온도를 상승
- PMIC의 PGND 패턴을 개선하거나 Ground 비아를 추가하여 PCB 레이아웃을 개선하는 것이 중요

AI Server, Data Center and Memory Wall

- Explosive increase in demand for the DRAM in the AI server and Data Center
  - A large number of memory products, such as DIMMs, need to be installed in a limited space.
  - As the demand for increased DRAM capacity continues to grow, the number of DRAM packages mounted on a single DIMM has been increasing.

* DRAM: Dynamic Random Access Memory
* DIMM: Dual In-line Memory Module

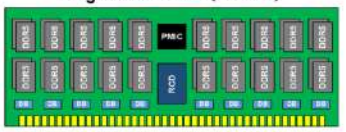


[Ref] A. Gholami, Z. Yao, S. Kim, C. Hooper, M. W. Mahoney and K. Keutzer, "AI and Memory Wall," in *IEEE Micro*, vol. 44, no. 3, pp. 33-39, May 2024.

PMIC in DDR5 DIMM

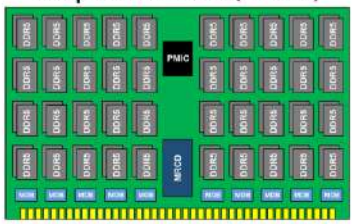
- From the DDR5 DIMM, the PMICs have begun to be directly mounted on the PCB of the DIMM for a more stable power supply.
  - The number of DRAM packages ↑ → Power consumption of the modules ↑
  - The MRDIMM doubles the data transmission channels and consequently doubles the data transfer rate compared to the RDIMM.

Registered DIMM (RDIMM)



* RCD: Rank Registering Clock Driver
* DB: Data Buffer

Multiplexed Rank DIMM (MRDIMM)



* MRCD: Multiplexed Rank Registering Clock Driver
* MDB: Multiplexed Rank Data Buffer

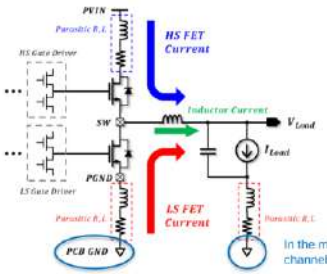
	Density	PMIC	Channels	Total Output Current
RDIMM	128 GB (2Rx4)	PMIC5000 (or Big PMIC)	Four (1.1 or 1.8 V)	Up to 20 A
MRDIMM	256 GB (4Rx4)	PMIC5020 (or Extreme PMIC)	Four (1.1 or 1.8 V)	Up to 30 A

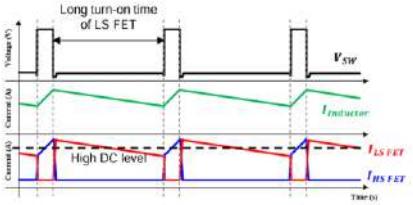
Power Ground (PGND) Current of PMIC

- During converting 12 V to 1.1 V (or 1.8 V) with the PWM or CCM, approximately 90% of the total load current flows to the PGND due to a long turn-on time of the low-side FET.

* PWM: Pulse Width Modulation
* CCM: Continuous Conduction Mode

Synchronous Buck Converter



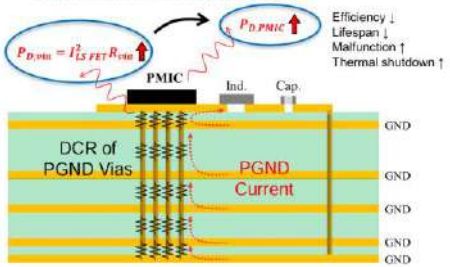


In the multi-channel PMIC, the synchronous buck converters of all channels share a common power ground.

Heat Generation due to DCR of PGND Vias

- In terms of thermal issues, it is necessary to improve the PCB layout by modifying the PGND pattern of the PMIC or adding ground vias.
  - Although a large amount of current flows to the PGND, the PGND pad of the PMIC on the RDIMM is not connected to the ground plane on the same layer but is instead connected to the ground plane on the next layer only through ground vias.
  - Due to the size limitations of the PGND pad for the PMIC and signal lines on the other layers, an insufficient number of PGND vias are embedded.
  - The ground current can flow intensively through only the PGND vias, resulting in heat generation due to the DC resistance (DCR) of the vias.
  - In next DIMM products including MRDIMM, the current capacity of the PMIC is expected to gradually increase.

The temperature rises due to via heating can diminish the heat dissipation efficiency, thereby potentially increasing the operating temperatures of the PMIC and power inductors.



3. DesignCon 2025 자료 소개

3-30 : Thermal Analysis and Optimized Design for Power Ground Vias of PMIC in DDR5 DIMM

➢ PCB 온도에 미치는 패턴 및 비아의 영향

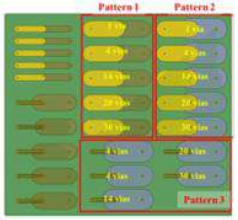
- 실측 및 Ansys Q3D & Icepak을 통한 Thermal Analysis 진행
- Pattern 1 : Top & Bot Layer에 넓은 Trace를 가지는 경우
- Pattern 2 : Top Layer와 인접한 내부 Layer에 넓은 Trace를 가지는 경우
- Pattern 3 : Top Layer는 DDR5 DIMM의 PGND 패드와 유사한 패턴, 내부 Layer에 넓은 Trace를 가지는 경우

Temperature Test PCB

- Three patterns with different copper patterns and the number of vias
  - The Pattern 1 consists of wide traces on both top and bottom layers. (# of vias: 1, 4, 14, 20, 30)
  - The Pattern 2 includes wide traces on both the top layer and an adjacent inner layers. (# of vias: 1, 4, 14, 20, 30)
  - In the Pattern 3, the top layer features a pattern similar to the PGND pad of the DDR5 DIMM's top layer, while the inner layer contains a wide trace. (# of vias: 4, 4 (center), 14, 20, 30)

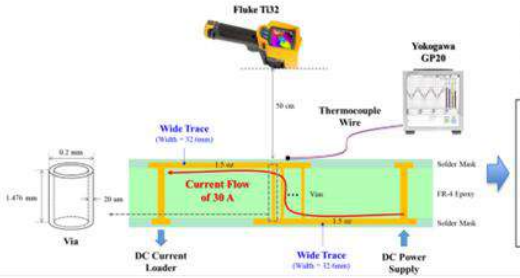
Real PCB

Simulation Model of PCB



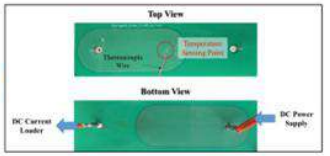
Pattern 1 – Top: Wide Trace, Bottom: Wide Trace

- Temperature measurement setup
  - Paperless recorder (Yokogawa GP20) and thermocouple wire (TT-T-30-K)
  - Infrared camera (Fluke Ti32)



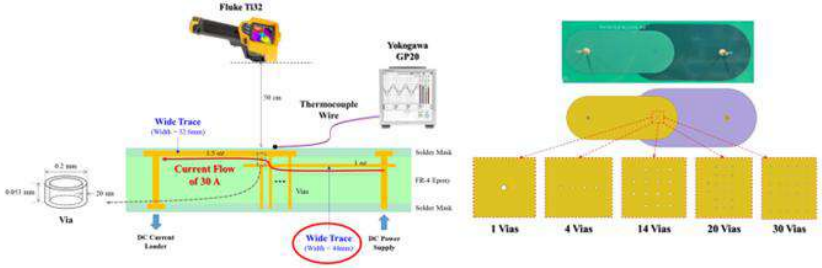
< Thermal Conductivity >

- FR-4 epoxy = 0.294 W/m/°C
- Solder mask = 0.26 W/m/°C



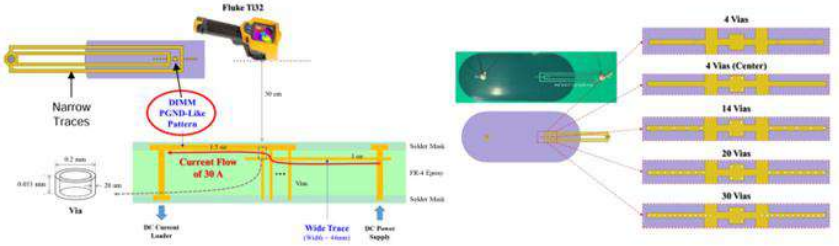
Pattern 2 – Top: Wide Trace, Inner: Wide Trace

- Temperature measurement setup and five cases of the Pattern 2
  - For the DC current of 30 A, when the conductor thickness is 1 oz and the inner conductor width is 44 mm, the temperature rise is approximately 5 °C, which is calculated from the following equation.



Pattern 3 – Top: DIMM PGND-Like Pattern, Inner: Wide Trace

- Temperature measurement setup and five cases of the Pattern 3
  - The Pattern 3 has a DIMM PGND-like pattern on the top layer and the thickness of 1 oz with four narrow traces.
  - The pattern on the top layer was designed in consideration of the die placement of the four buck converters in the PMIC of DDR5 DIMMs, in order to mimic the current flow of the PGND merging from four directions.
  - Due to the small size of the DIMM PGND-like pattern, the traces that allow current to flow out should be quite narrow.



3. DesignCon 2025 자료 소개

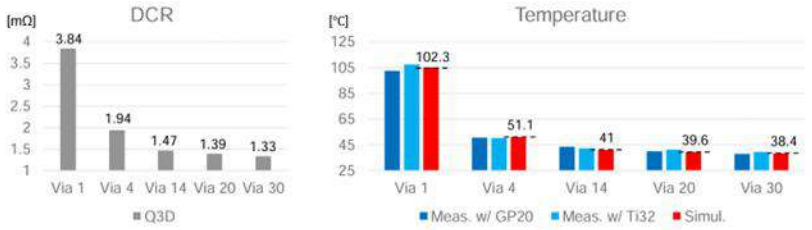
3-30 : Thermal Analysis and Optimized Design for Power Ground Vias of PMIC in DDR5 DIMM

➢ PCB 온도에 미치는 pattern 및 vias 영향

- 실측 및 Ansys Q3D & Icepak을 통한 Thermal Analysis 진행
- Via 수가 증가함에 따라 DCR이 PCB 온도가 줄어 들음을 확인
- Pattern 3: 좁은 trace에서 발생하는 열 > Via에서 발생하는 열, Via 수가 온도 차이에 영향을 확인

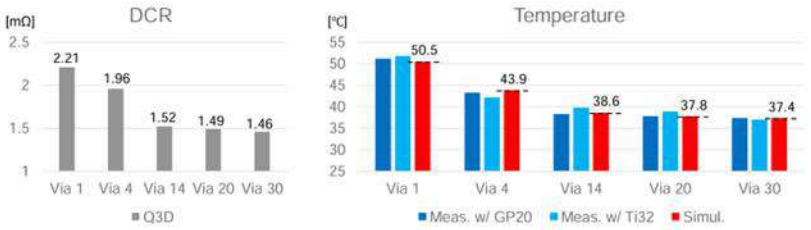
Pattern 1 – Top: Wide Trace, Bottom: Wide Trace

- Simulated DCR and temperature comparison between the measurement and simulation
  - The DCRs mean the resistance from the source port to the sink port. The difference in the DCRs is only due to the variation in the number of vias.
    → As the number of vias increases, the DCR decreases, leading to a reduction in the PCB temperature.
  - The temperature results of the measurement and simulation exhibit an error below 5% across all cases.
    → The measured and simulated temperature results can be considered reliable data.



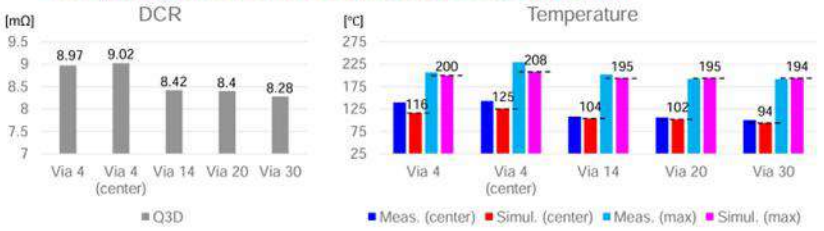
Pattern 2 – Top: Wide Trace, Inner: Wide Trace

- Simulated DCR and temperature comparison between the measurement and simulation
  - Compared to the Pattern 1, the Pattern 2 has a shorter via length, which reduces the DCR of the vias.
    → The heat generated by the vias decreases, leading to a lower PCB temperature.
    → The temperature difference between two patterns is more significant when the number of vias is smaller.
  - As the number of vias increases, the DCR decreases, leading to a reduction in the PCB temperature.



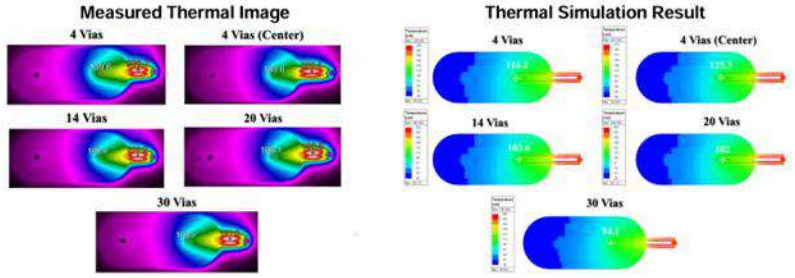
Pattern 3 – Top: DIMM PGND-Like Pattern, Inner: Wide Trace

- Simulated DCR and temperature comparison between the measurement and simulation
  - The measured and simulated temperature results for the five cases of the Pattern 3 have a slight discrepancy. (The absolute value of the temperature was too high, and it is presumed that the discrepancy occurs because the accuracy of measurements with the infrared camera is relatively lower than that of measurements with contact method.)
  - In this structure, the discrepancy in terms of the DCR or temperature is not significant when more than 14 vias are added in comparison to the number of vias added. If the number of vias is limited due to the structure of the product board, it seems necessary to insert at least 14 vias to reduce the impact of heat generation caused by the DCR.



Pattern 3 – Top: DIMM PGND-Like Pattern, Inner: Wide Trace

- Measured and simulated thermal images of the five cases
  - The heat generated by the narrow traces is more dominant than that generated by the vias, and the highest temperature is observed at the midpoint of the traces.
  - The heat generated by the vias still has an impact, resulting in temperature differences depending on the number of vias.



3. DesignCon 2025 자료 소개

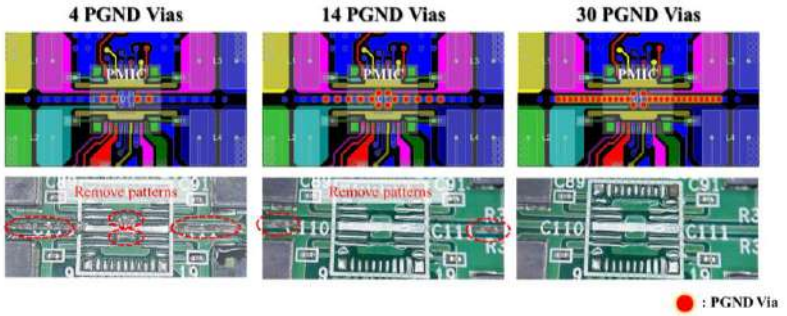
3-30 : Thermal Analysis and Optimized Design for Power Ground Vias of PMIC in DDR5 DIMM

➢ PMIC의 PGND Via의 열 분석

- PGND 비아 수를 늘리면 PMIC 온도가 감소
- PMIC에 최대 30개의 PGND 비아를 추가하는 것이 PMIC 온도 감소에 효과적

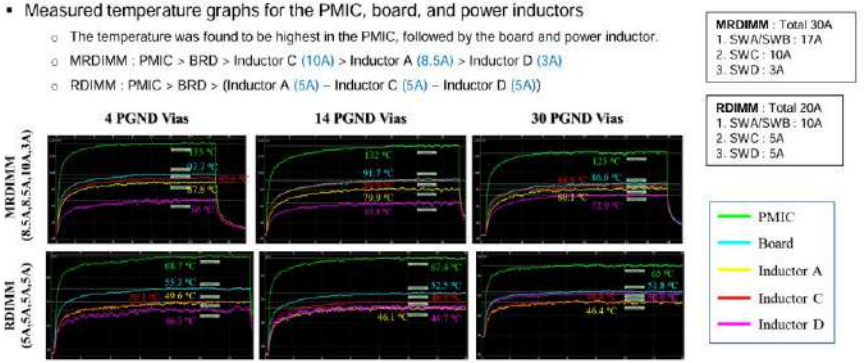
PGND Patterns of PMIC EVB

- Three patterns of the PMIC EVB according to the number of the PGND vias



Temperature Measurement Results

- Measured temperature graphs for the PMIC, board, and power inductors
  - The temperature was found to be highest in the PMIC, followed by the board and power inductor.
  - MRDIMM : PMIC > BRD > Inductor C (10A) > Inductor A (8.5A) > Inductor D (3A)
  - RDIMM : PMIC > BRD > (Inductor A (5A) – Inductor C (5A) – Inductor D (5A))

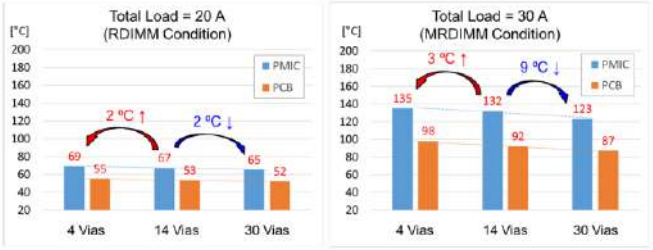


MRDIMM : Total 30A
1. SWA/SWB : 17A
2. SWC : 10A
3. SWD : 3A

RDIMM : Total 20A
1. SWA/SWB : 10A
2. SWC : 5A
3. SWD : 5A

Temperature Measurement Results

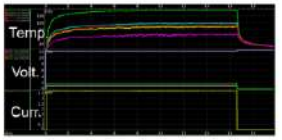
- Saturated temperatures for the PMIC and board
  - For both the PMIC and board, higher total load current results in higher temperatures, while an increased number of PGND vias leads to lower temperatures.
  - Since increasing the number of PGND vias up to 30 provides a temperature reduction effect on the PMIC, it is advisable to insert as many vias up to 30 as possible if feasible.



Efficiency of PMIC

- Efficiency according to the number of PGND vias
  - Reducing the number of PGND vias increases the temperature of the PMIC, thereby decreasing its efficiency.
  - $P_{IN} = V_{IN} \times I_{IN}$
  - $P_{OUT} = V_{DD} \times I_{DD} + V_{DDQ} \times I_{DDQ} + V_{PP} \times I_{PP}$
  - $P_D = P_{IN} - P_{OUT}$
  - $\eta = \frac{P_{OUT}}{P_{IN}} \times 100\%$

Measured Temp. & Volt. & Curr.



	Full Load Condition of RDIMM (SWAB = 10 A, SWC = 5 A, SWD = 5 A)			Full Load Condition of MRDIMM (SWAB = 17 A, SWC = 10 A, SWD = 3 A)		
# of PGND Via	Via 4	Via 14	Via 30	Via 4	Via 14	Via 30
P_{IN}	29.1 W	29 W	28.9 W	44.5 W	43.9 W	43.8 W
P_{OUT}	25.24 W	25.23 W	25.16 W	34.61 W	34.5 W	34.48 W
P_D	3.86 W 0.26% ↓	3.77 W 0.06% ↑	3.74 W	9.89 W 0.81% ↓	9.4 W 0.13% ↑	9.32 W
Efficiency	86.74 %	87 %	87.06 %	77.78 %	78.59 %	78.72 %

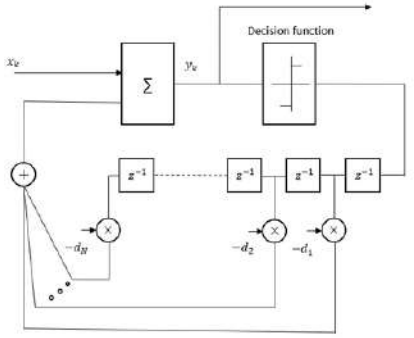
3-31 : Multiple Pulses-Based Decision Feedback Equalizer (MPDFE) for PAM4

➢ Introduction

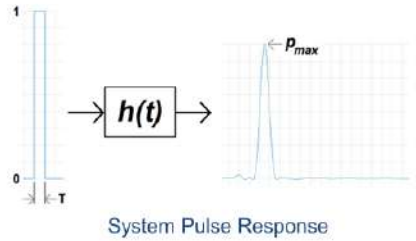
- 신호 속도 증가와 복잡한 변조 방식(예: PAM4)으로 인해 수신기에서 신호 보상이 어려워 짐
- 기존의 Decision Feedback Equalizer (DFE)는 단일 Linear Fit Pulse Response (LFPR)에 기반
  →PCIe 표준은 전송 속도 증가와 함께 DFE 탭 수가 증가하고, NRZ에서 PAM4로 변조 방식이 변경되는 추세를 보임
- 개선된 DFE 구조를 위해 다중 LFPR을 활용하는 새로운 DFE 구조인 MPDFE (Multiple Pulses-Based DFE)를 제안

TRADITIONAL DFE STRUCTURE

- There is a single set of DFE tap values.
- The tap values can be derived from the single LFPR.



LFPR DEFINITION

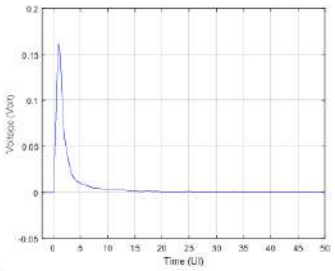


System Pulse Response

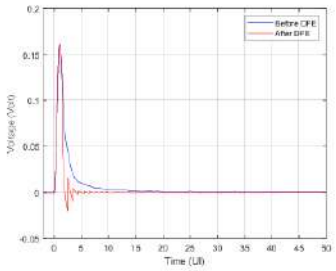
Linear Fit Pulse Response (LFPR):

Estimate of a system's pulse response, based on a sample of the system's output when transmitting a complex data pattern, using a least-squares technique

DFE taps determined from LFPR



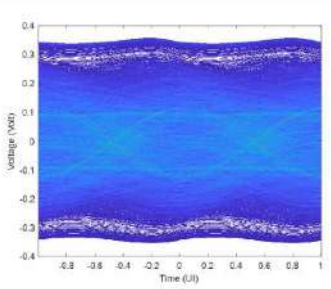
Single LFPR



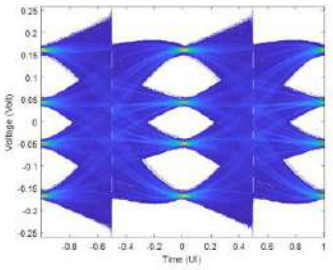
Pulse with DFE applied

The DFE tap values are determined to minimize the amplitudes of the post cursors samples at the UI centers.

DFE OPENS THE EYE DIAGRAM



Before DFE



After DFE

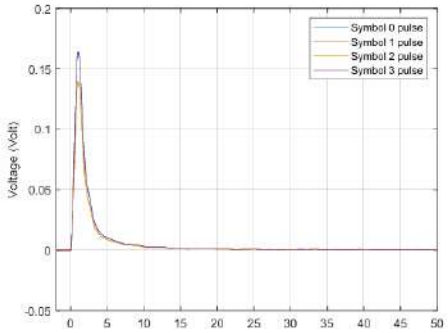
The DFE reduces the amplitudes of the post cursors samples at the UI centers.

3-31 : Multiple Pulses-Based Decision Feedback Equalizer (MPDFE) for PAM4

- DFE(Multiple Pulsed-Based DFE)
  - 기존 DFE는 단일 LFPR에서 파생된 단일 탭 값 세트를 사용
  - PAM4 신호는 각 symbol마다 서로 다른 normalized pulses를 가짐
  - MPDFE는 다중 LFPR을 사용하여 각 심볼에 대한 개별 LFPR을 추출하여 더 많은 신호 정보를 capturing
  - MPDFE는 지연 블록을 통과하는 심볼에 따라 미리 정의된 tap 세트에서 각 DFE tap을 선택

PAM4 MULTIPLE LFPR

- Hypothesis: The PAM4 transmitter physically produces symbols or symbol transitions using multiple circuits that may not match exactly.
- PAM4 multiple LFPR models the transmitter symbols.
- The mismatch between the normalized symbols can be observed.



PAM4 MULTIPLE LFPR DE-NORMALIZED

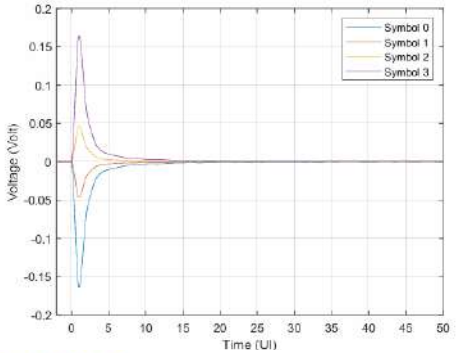
- The normalized PAM4 multiple LFPR can be denormalized:

$$p_{sym0\_un\_normalized} = -p_{sym0\_3}$$

$$p_{sym1\_un\_normalized} = -\frac{1}{3}p_{sym1}$$

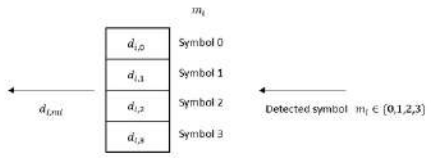
$$p_{sy\ \ \_un\_normalized} = \frac{1}{3}p_{sy}$$

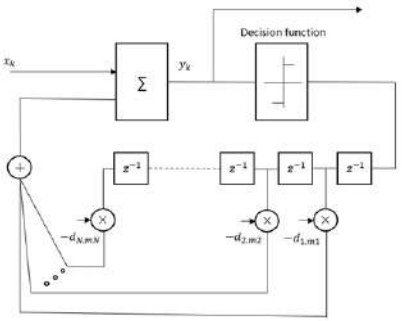
$$p_{sym3\_un\_normalized} = p_{sy\ \ \_3}$$



MPDFE STRUCTURE

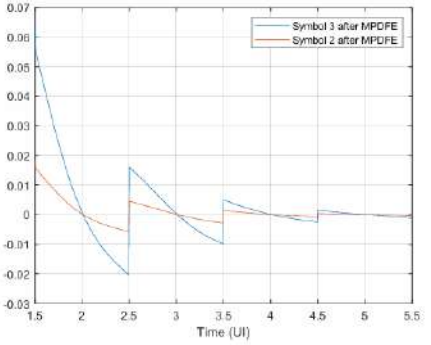
- Each DFE tap is chosen from a predefined set of taps based on the symbol passing through the delay blocks.
- The predefined set of taps is derived from multiple LFPR.





DFE BASED ON MULTIPLE LFPR

- Applying the MPDFE taps to the symbol pulses yields zero residuals at the UI centers of the post DFE pulses for the un-normalized symbol 3 and symbol 2.



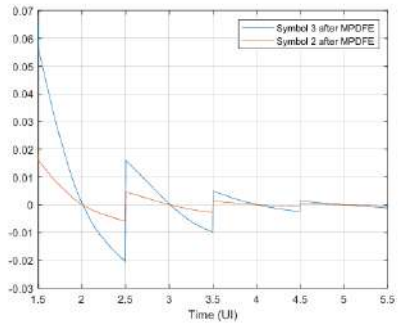
3-31 : Multiple Pulses-Based Decision Feedback Equalizer (MPDFE) for PAM4

➢ Results : MPDFE(Multiple Pulsed-Based DFE)의 장점

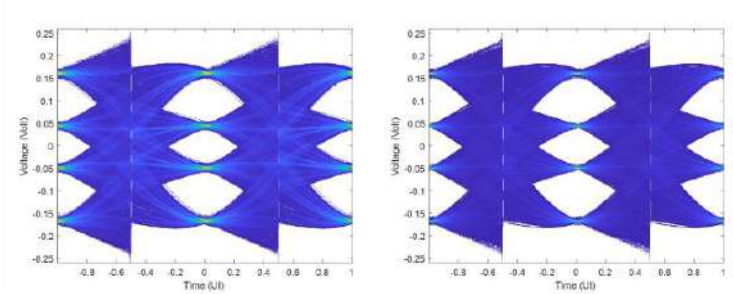
- 기존 DFE는 비정규화 심볼 펄스 적용 시 UI 센터에 잔류 신호 발생.
- 심볼 펄스 적용 시 UI 센터에 잔류 신호 없음.
- MPDFE의 Eye diagram은 기존 DFE보다 UI 센터 Trace 가늘고 Vertical eye opening가 큼.
- MPDFE는 기존 DFE와 유사한 계산 복잡도, MLSE(Maximum-likelihood sequence estimation)보다 훨씬 낮음.
- MPDFE는 비용 증가 없이 수신기 성능 향상 기술.

DFE BASED ON MULTIPLE LFPR

- Applying the MPDFE taps to the symbol pulses yields zero residuals at the UI centers of the post DFE pulses for the un-normalized symbol 3 and symbol 2.



DFE vs. MPDFE



DFE MPDFE

MPDFE eye diagram has thinner traces for the 4 symbol levels at the UI center and has greater vertical eye opening than DFE eye diagram.

COMPARE MLSE WITH DFE AND MPDFE

- The Maximum-likelihood sequence estimation (MLSE) equalizers provide optimal sequence estimation given the channel characteristics.
- MLSE equalizers are optimal if the channel characteristics are known or accurately estimated, and MLSE equalizers are long enough to fully cover the range of the channel response.

Equalizer type	Computational complexity
DFE	$M \times L$
MPDFE	$M \times L$
MLSE	M^L

Equalizer type	$L = 10$	$L = 20$	$L = 40$
DFE	40	80	160
MPDFE	40	80	160
MLSE	1.04E6	1.10E12	1.21E24

3-32 : Perspectives on Managing Intra-Pair Skew in Copper Cable Assemblies for High-Volume Deployments

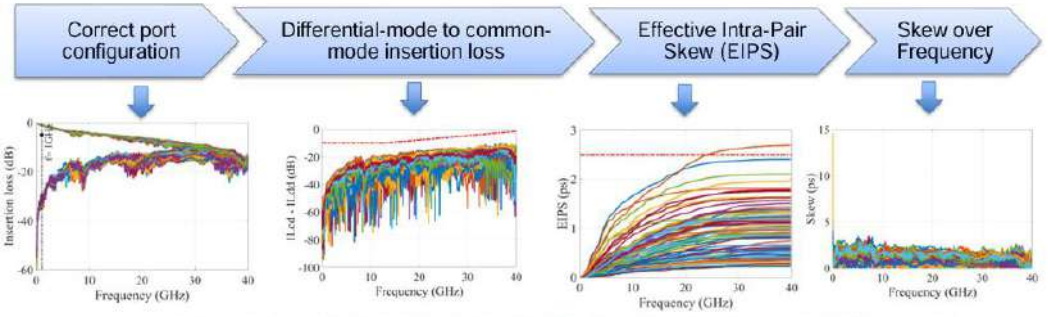
- Introduction
  - high-performance copper interconnects에 대한 시장 수요 증대, 하지만 performance variability and link performance degradation과 같은 과제 존재
  - 케이블의 물리적 변형에 의해 발생하는 Intra-Pair Skew는 성능에 중요한 영향을 미치는 요소

Motivation and goal

- Intra-pair skew impacts mode conversion and noise arising from mode conversion and crosstalk
- Propose a methodology to assess/control the intra-pair skew in cable-based topologies
- Holistic approach (not limited to a specific application/implementation)
- Saving time/cost in production line workflow

The multi-segment cable-based link used in this work

Skew assessment flow of a +112Gb/s cable assembly



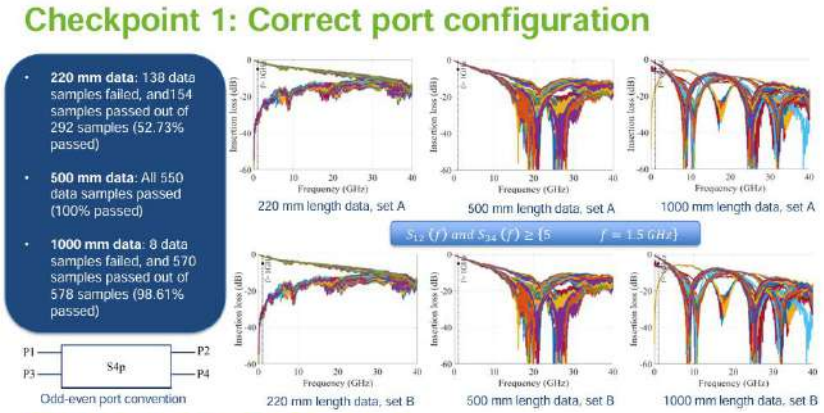
Amphenol's measured Paladin HD2® (PHD2) to PHD2 - 26 AWG topology data against different masks

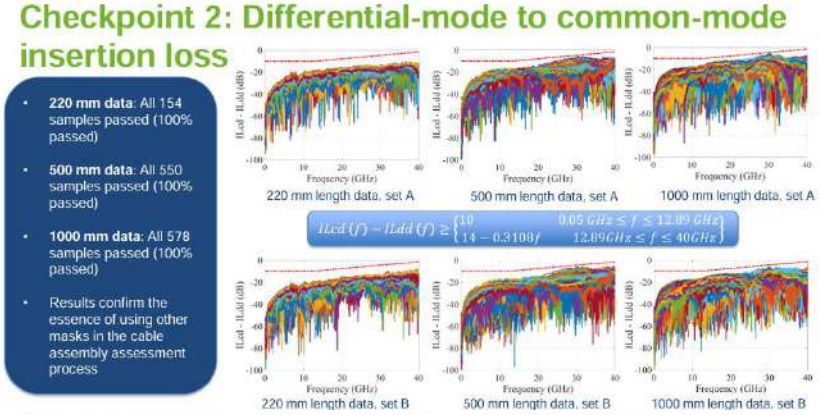
3. DesignCon 2025 자료 소개

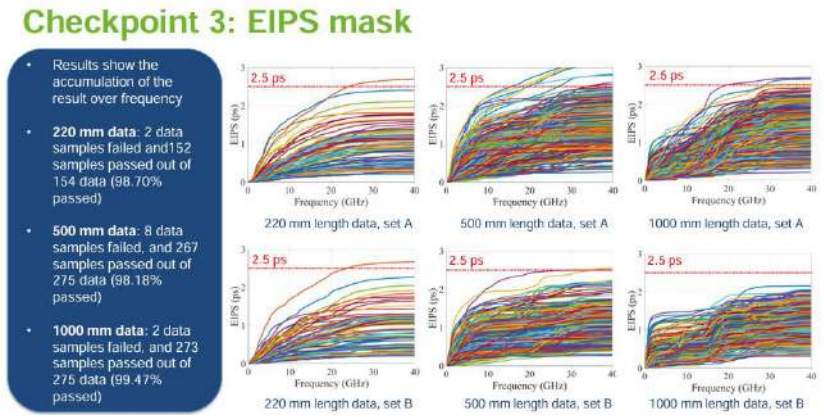
3-32 : Perspectives on Managing Intra-Pair Skew in Copper Cable Assemblies for High-Volume Deployments

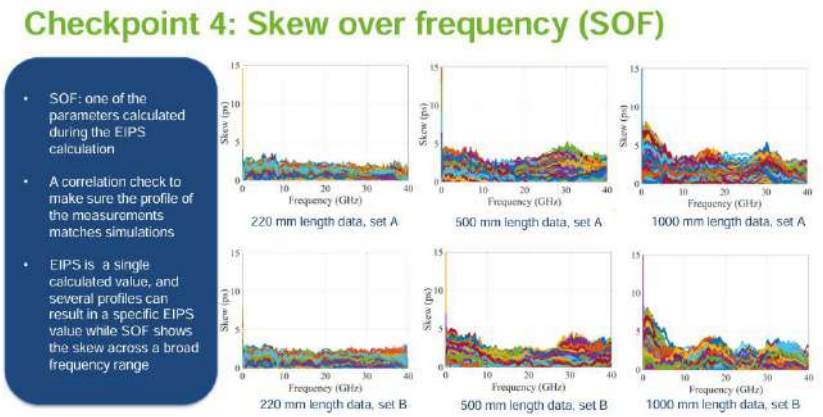
➢ Skew 평가 방법론 및 해결 방안

- verification of accurate port configuration, application of the SCD21-SDD21 mask, utilization of the EIPS (Effective Intra-Pair Skew) mask, and application of the SOF (Skew over Frequency) mask
- EIPS는 skew로 인한 SCD21 변화량과 random bit stream의 power spectral density (PSD)를 결합한 가중 함수를 통해 산출되며, SOF는 광범위한 주파수 대역에서 측정된 skew profile과 시뮬레이션 결과를 비교하여 상관성을 확인하는 데 활용









3-32 : Perspectives on Managing Intra-Pair Skew in Copper Cable Assemblies for High-Volume Deployments

➢ 결론

- Intra-pair skew performance of copper cable segments는 통계적으로 예측가능한 범위, EIPS 임계 값 설정을 통해 부적합 어셈블리를 효과적으로 선별 가능
- CTLE(Continuous-Time Linear Equalization) 및 FFE(Feed-Forward Equalizer)와 같은 equalization technologies은 케이블 skew의 주파수 의존적 특성을 활용하여 신호 품질 저하를 효과적으로 완화할 수 있음

Data / Checkpoint	220mm (ps)	500mm (ps)	1000mm (ps)
Median EIPS, set A	1.20	1.49	1.48
Avg. EIPS, set A	1.31	1.51	1.44
Std. Dev., set A	0.72	0.55	0.55
Max EIPS, set A	3.54	3.32	3.43
Min EIPS, set A	0.22	0.27	0.22
Median EIPS, set B	1.16	1.11	1.21
Avg. EIPS, set B	1.26	1.12	1.21
Std. Dev., set B	0.74	0.44	0.41
Max EIPS, set B	3.42	2.56	2.81
Min EIPS, set B	0.21	0.27	0.31

Table-2: Summary of EIPS statistics for the data set used in this study, across lengths.

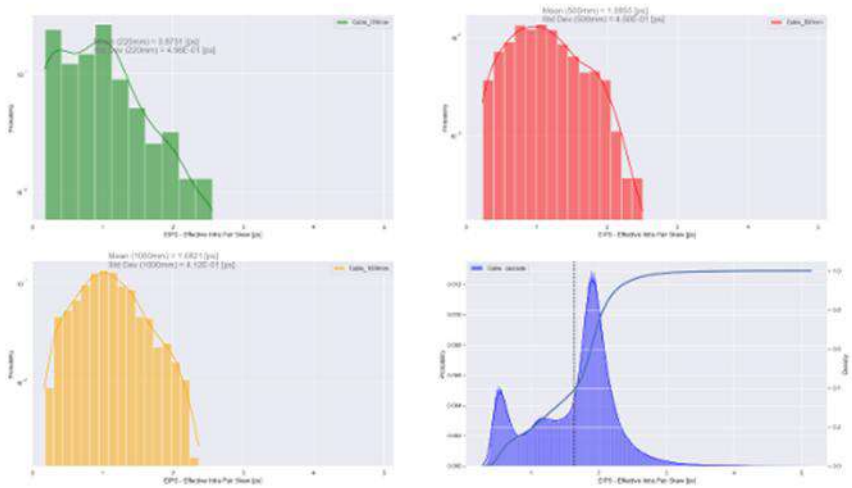


Figure-18: Cascaded Cable Skew (EIPS) distribution.

3-33 : Practical implementation of insertion loss correction and delay characterization of test fixtures used for 200 Gb/s per lane conformance

- Introduction – Test Fixtures and Insertion Loss
  - Ethernet PHY specifications은 transmission medium과 호환되는 신호를 생성
  - 고속 이더넷 conformance testing에는 test fixture가 필수적임
  - 실제 insertion loss와 기준 insertion loss의 차이를 보정해야 함

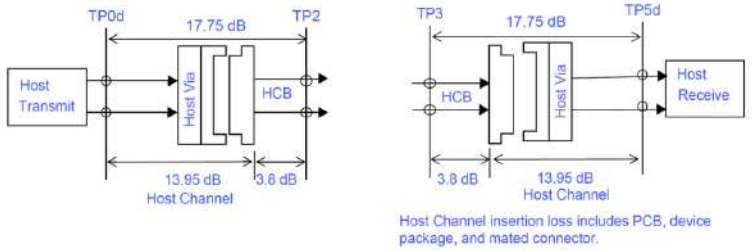


Figure 1—802.3dj/D1.3 CR Host Test Points TP2 and TP3 and reference IL at 53.125 GHz

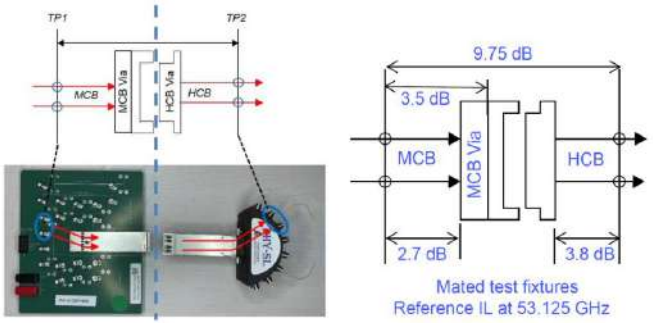


Figure 4—802.3dj/D1.3 Mated test fixture reference IL at 53.125 GHz

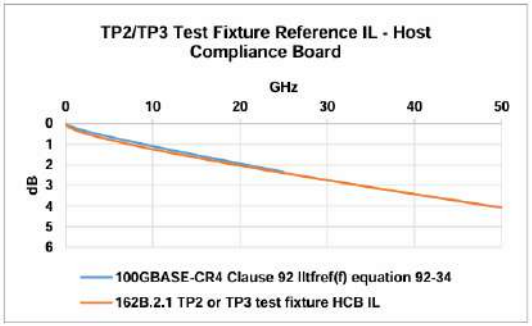


Figure 5—TP2/TP3 (HCB) reference insertion loss

IEEE 802.3 Projects	Clause/ Annex	Type	Gb/s	GBd	GBd/2	TP2/TP3 - HCB Reference Insertion Loss
802.3bj	92	100GBASE-CR4	25	25.78125/NRZ	12.8906	92.11.1.2 - EQ (92- 34) 0.01 ≤ f(GHz) ≤25 @ 12.8906 GHz - 1.35 dB
802.3by	110	25GBASE-CR	25	25.78125/NRZ	12.8906	110B.1.1- 92.11.1.2 - EQ (92- 34) 0.01 ≤ f(Ghz) ≤25 @ 12.8906 GHz - 1.35 dB
802.3bs	120E	200GAUI-4 C2M 400GAUI-8 C2M	50	26.5625/PAM4	13.28	120E.4.1- 92.11.1.2 EQ (92- 34) - 0.01 ≤ f(GHz) ≤26.5625 @13.28 GHz - 1.38 dB
802.3cd	136	50GBASE-CR 100GBASE-CR2 200GBASE-CR4 50GAUI-1 C2M 100GAUI-2 C2M	50	26.5625/PAM4	13.28	136B.1.1 and 110B.1.1 - 92.11.1.2 EQ (92- 34) – 0.01 ≤ f(GHz) ≤26.5625 @ 13.28 GHz - 1.38 dB
802.3ck	162	100GBASE-CR1 200GBASE-CR2 400GBASE-CR4 100GAUI-1 C2M 200GAUI-2 C2M 400GAUI-4 C2M	100	53.125/PAM4	26.56	162B.2.1 and 120G.5.4 162B.2 EQ 162B-1 - 0.01 ≤ f(GHz) ≤ 50 @ 26.56 GHz - 2.5 dB
802.3dj/D1.3	179	200GBASE-CR1 400GBASE-CR2 800GBASE-CR4 1.6TBASE-CR8 100GAUI-1 C2M 200GAUI-2 C2M 400GAUI-4 C2M 800GAUI-8 C2M 1.6TAUI-16 C2M	200	106.25/PAM4	53.125	179B.2.1 and 120G.5.4 179 B.2 EQ 179B-1 0.01 ≤ f (GHz)≤ 67 @ 53.125 GHz - 3.8 dB

Table 1 — IEEE 802.3 TP2/TP3 (HCB) reference insertion loss

3. DesignCon 2025 자료 소개

3-33 : Practical implementation of insertion loss correction and delay characterization of test fixtures used for 200 Gb/s per lane conformance

- Partial De-embedding for Insertion Loss Correction
  - De-embedding이란 test fixture의 영향을 제거하는 기술
  - Partial de-embedding은 2x-thru를 사용하여 일부분만 제거
  - 소프트웨어로 de-embedding plane 조절이 가능하며 사전 정보가 불필요
  - SFG solution과 synthetic transmission line solution 두 가지 방법을 사용

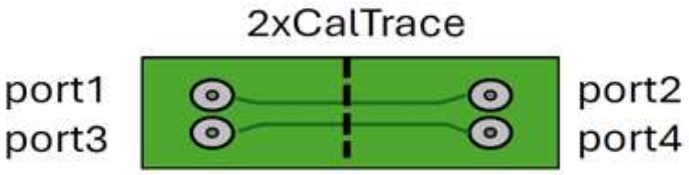


Figure 7— 2xCalTrace and de-embedding plane

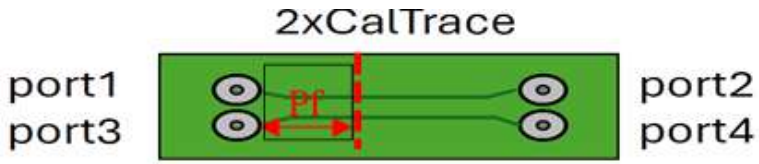


Figure 10— 2xCalTrace and bifurcation plane using partial de-embedding

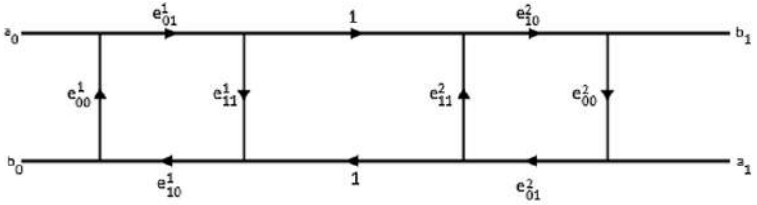


Figure 9—2x-thru signal flow graph

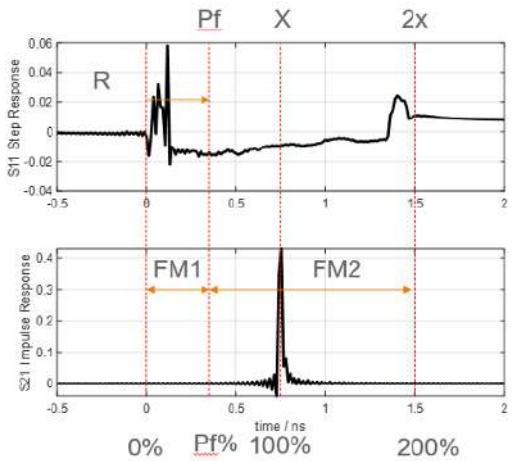


Figure 11 —A diagram showing the impedance of the 2x-thru (top) and the impulse response of the 2x-thru (bottom). The diagram shows the key points described in the text.

3. DesignCon 2025 자료 소개

3-33 : Practical implementation of insertion loss correction and delay characterization of test fixtures used for 200 Gb/s per lane conformance

- Validation and C2M Conformance Testing
  - Eye diagram과 Pulse Fit response 비교를 통해 유효성을 검증
  - Partial de-embedding은 artifact를 발생시키지 않음을 확인
  - 200 Gb/s C2M 환경에서 COM 분석을 수행하여 적용 가능성을 평가
  - Insertion loss 보정과 성능 개선 효과를 확인

Figure 17— Eye Diagram Comparison at TP1A – T1 De-embedding

Figure 22— Eye Diagram Comparison at TP4 – T1 & T2 De-embedding

Figure 30— PFR Comparison at TP1a (T1_QSFP-DD-400G-HCB$_{pdemb}$ vs QSFP-DD-HCB$_{ref}$)

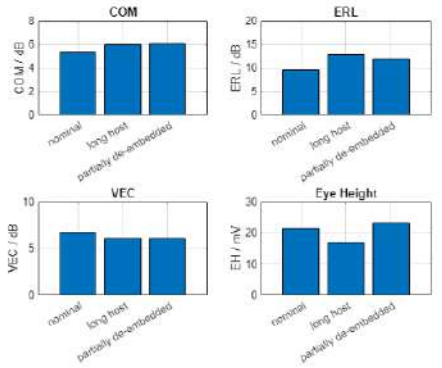


Figure 44— COM, ERL, VEC and Eye Height results of the nominal, long HCB, and partially de-embedded model.

3-34 : Information Classification: General

Transmitter Power Spectral Density Noise Impact for 200 Gb/s PAM 4 per lane

- Measuring SNDR and Impact of Channel Loss
  - SNDR(신호 대 잡음 및 왜곡 비율)은 일반적으로 테스트 지점에서 측정되는 송신기 성능을 특성화 하는 매개변수
  - 처음에는 SNDR이 채널 손실에 관계없이 일정하게 유지되어 측정 및 COM 사용이 간소화된다고 가정했지만, 측정 결과 신호 진폭이 노이즈보다 더 큰 영향을 받기 때문에 SNDR은 채널 손실이 증가함에 따라 감소
  - SNDR의 이 테스트 포인트 종속성은 송신기 노이즈 특성에 의존하는 COM(채널 작동 마진) 계산에 불확실성을 발생

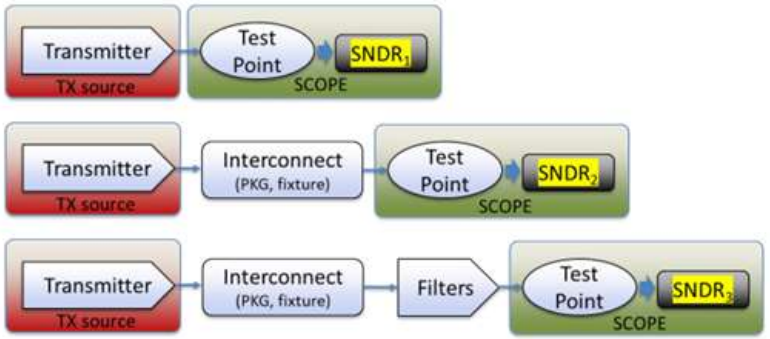


Fig. 4. Evolution of the assumptions for an accurate characterization of the SNDR.

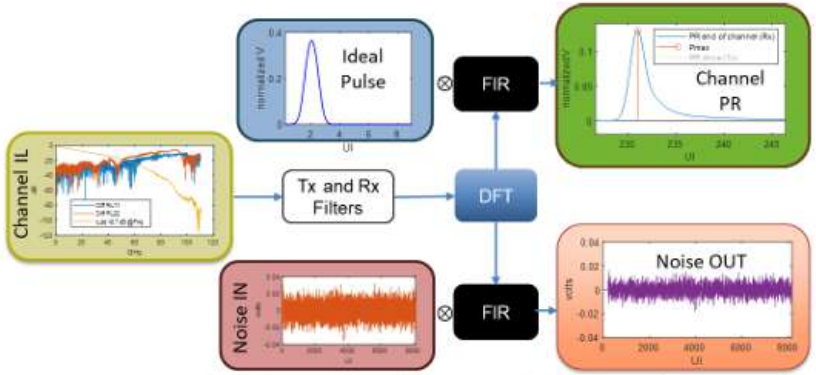


Fig. 5. Procedure for the assessment of the losses on the calculation of SNDR.

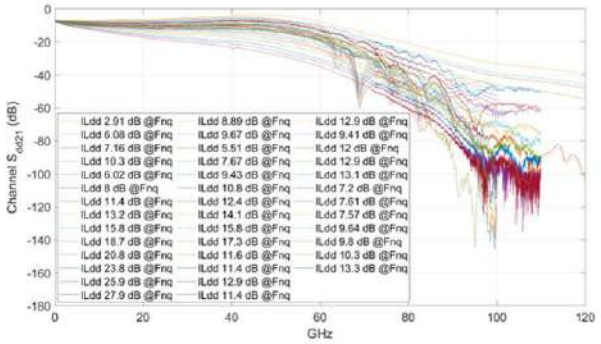


Fig. 6. Procedure for the assessment of the losses on the calculation of SNDR.

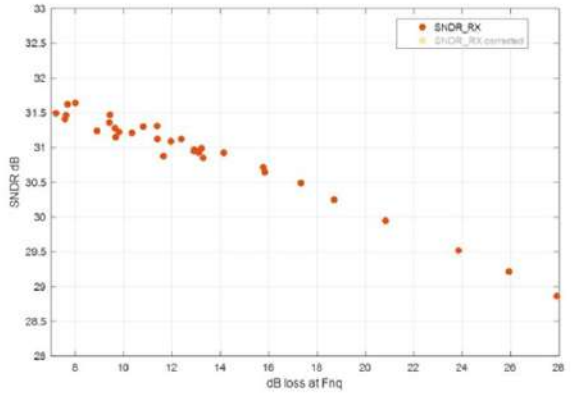


Fig. 7. SNDR value extracted at the end of the different channels in Fig. 6.

3-34 : Information Classification: General

Transmitter Power Spectral Density Noise Impact for 200 Gb/s PAM 4 per lane

- SNDR Correction and Role in COM
  - channel loss dependency을 해결하기 위해, SNDR 계산 시 신호 전력으로 power of the sampled pulse response을 사용하는 방법이 제안
  - 이러한 보정은 SNDR을 중간 채널에 더욱 일관적이고 독립적으로 만들어 COM의 정확성을 향상시키는 것을 목표
  - COM은 채널, 송신기 및 수신기 모델을 활용하는 채널 설계를 위한 SNR 관점

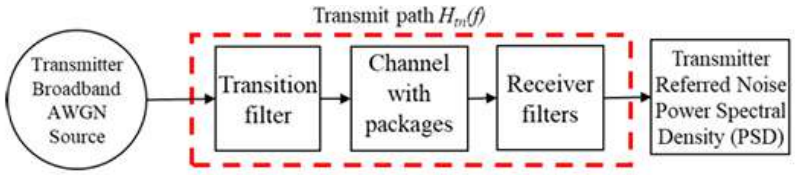


Fig. 8: Noise path simplification

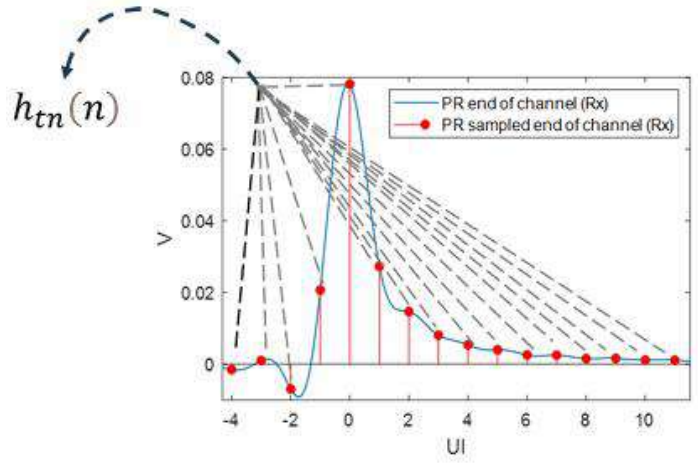


Fig. 9 Sampled System PR

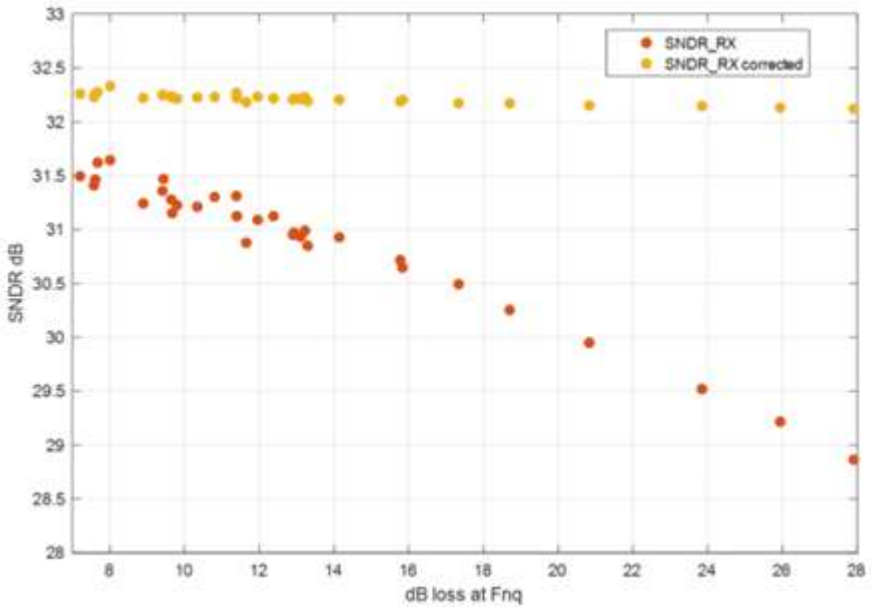


Fig. 10. Original and after correction SNDR.

3-34 : Information Classification: General

Transmitter Power Spectral Density Noise Impact for 200 Gb/s PAM 4 per lane

- Importance of Noise Spectrum and Conclusion
  - COM 성능은 동일 RMS 노이즈에도 스펙트럼 내용에 따라 영향을 받음
  - 낮은 주파수에 노이즈가 집중될수록 COM 값은 감소
  - COM에서 SNDR의 broadband Gaussian noise 가정은 시뮬레이션과 실제 측정 간의 불일치를 야기
  - high-speed data rates과 spectral efficiency을 위해 Transmitter noise spectrum (PSD) 고려
  - SNDR, COM, 적합성 테스트 표준에 transmitter noise spectrum을 통합하는 작업이 필요

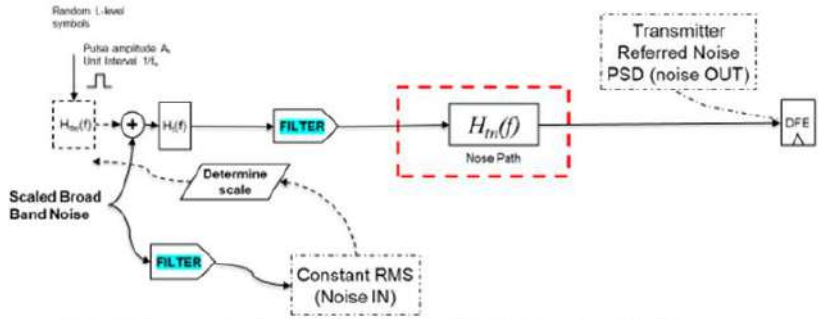


Fig. 11: Transmitter Output Noise Spectral filtering keeping RMS constant

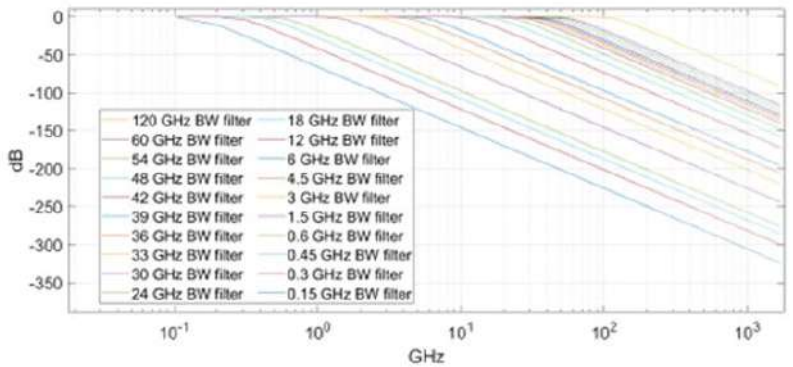


Figure 12: Butterworth Filter Noise Filter Response with Cutoff Swept from 150 MHz to 120 GHz

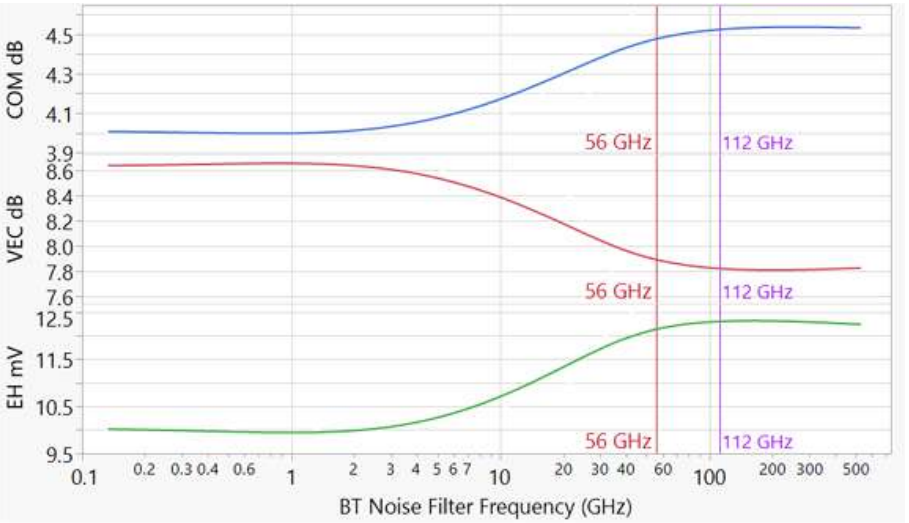


Figure 13 COM, VEC, and EH vs. Butterworth 3dB Cutoff Frequency

3. DesignCon 2025 자료 소개

3-35 : Channel Embedding/De-Embedding Methodology for Rx Stress Testing Using Fast Edge Tx Waveform of BERT

➢ Challenges in Receiver Compliance Testing

- 표준화된 고속 직렬 IO는 최대 채널 손실의 최악 조건으로 수신기 적합성 테스트를 정의
- BERT는 수신기 적합성 테스트의 신호 소스로 흔히 사용
- 하지만 BERT 대신 실제 실리콘 Tx를 사용하면 마진 문제가 발생하거나 실패할 수 있음
- BERT Tx와 실제 실리콘 Tx 간의 불일치 원인을 파악하고 해결책을 제시하는 것이 중요

Spec compliant test signal

*A 14ps/22ps TTC of HS9454-14/HL9454-22 by HYPERLABS was used as an example.

- A time transition converter (TTC*) has an effect of low-pass filter which slows down the Tx rise/fall times.
- The s-parameter of TTC was measured by the Keysight N1055A 50GHz TDR.
- The exported touchstone file (*.s4p) will be used for Infiniisim embedding function for the next slide.

Figure 2. Time-transition converter

Figure 3. differential return loss measurement of TTCs using Keysight N1055A 50GHz TDR

Figure 4. Measured differential return loss of TTCs

Quick recap on receiver compliance test

- Receiver test setup using BERT
  - Bit Error rate tester
    - Data rate (Frequency)
    - Pattern
    - Amplitude / Offset
  - Time Transition Converter (TTC)
  - ISI trace (or Variable ISI)
  - Rx replica trace (for BGA application)
  - Skew matched paired cables
  - External (Rx2Tx) loopback mode w/ Equalization (Adaptation)

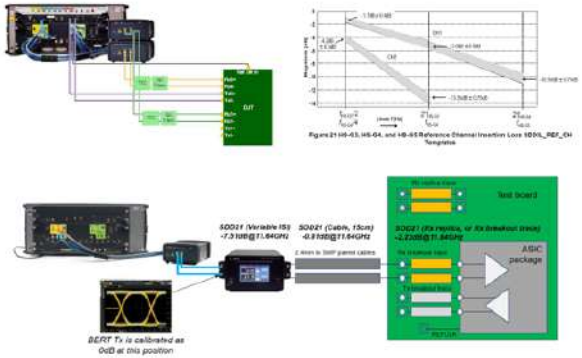


Figure 1. Example connection diagram of MIPI MPHY5.0 Rx CTS

3-35 : Channel Embedding/De-Embedding Methodology for Rx Stress Testing Using Fast Edge Tx Waveform of BERT

- Utilizing TTC and Simulation for Realistic Signals
  - TTC (Time Transition Converter)는 Tx 신호의 rise/fall 시간을 늦추는 저역 통과 필터 효과를 가짐
  - Keysight의 Infiniisim S/W는 TTC s-parameter 파일을 임베딩/디임베딩하여 원하는 토폴로지를 구성할 수 있음
  - 다수의 TTC를 직렬로 연결하여 다양한 채널 손실 조건(-2dB, -4dB, -6dB 등)을 시뮬레이션할 수 있음
  - Infiniisim 또는 ADS를 사용하여 TTC, 테스트 채널, Rx 패키지 등을 임베딩하는 AMI 시뮬레이션이 가능

AMI simulation using embedded test signals

- Another case study of Tx rise/fall time will be checked by SI simulation using measured waveforms.
- The transmitter will be BERT.
- Embedding TTC/test channel/Rx package can be done by Infiniisim S/W or ADS.

Figure 16. Tx_Waveform_AMI setup when embedding channel effects using Infiniisim S/W

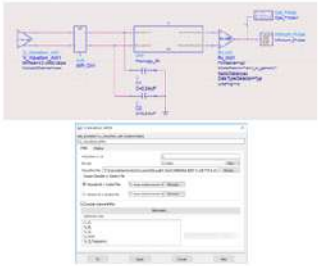


Figure 17. Tx_Waveform_AMI setup when embedding channel effects using ADS

MIPI reference EQ out with embedded test signal

- This example is to verify that the BERT Tx waveform *with triple cascaded TTCs* be conformed to the MIPI MPHY5.0 criteria of Test 1.1.7, which is HS-TX G5 Differential AC Eye.

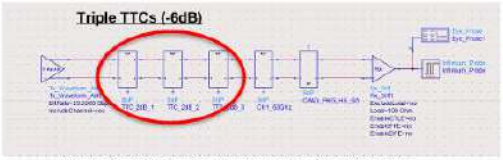


Figure 45. A MIPI reference channel 1 simulation setup using measured waveforms and MIPI reference EQ

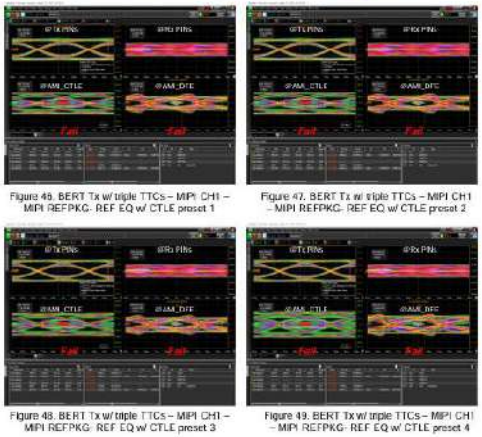


Figure 46. BERT Tx w/ triple TTCs – MIPI CH1 – MIPI REFPKG: REF EQ w/ CTLE preset 1

Figure 47. BERT Tx w/ triple TTCs – MIPI CH1 – MIPI REFPKG: REF EQ w/ CTLE preset 2

Figure 48. BERT Tx w/ triple TTCs – MIPI CH1 – MIPI REFPKG: REF EQ w/ CTLE preset 3

Figure 49. BERT Tx w/ triple TTCs – MIPI CH1 – MIPI REFPKG: REF EQ w/ CTLE preset 4

3-35 : Channel Embedding/De-Embedding Methodology for Rx Stress Testing Using Fast Edge Tx Waveform of BERT

- BERT-Silicon Tx Correlation and Target Channel Rx Testing
  - 실리콘 Tx의 rise/fall 시간이 BERT Tx보다 느린 경우가 많음
  - BERT Tx에 삽입 손실을 추가하여 실리콘 Tx와 유사한 rise/fall 시간을 만들 수 있음
  - 목표 interconnect channel로 Rx 테스트를 수행하기 위한 보정 절차가 필요
  - channel loss, CDR settings, and test patterns를 고려한 target channel 기반 Rx JTOL (jitter tolerance) 검증 필요

Tx eye comparison between BERT and silicon

- As shown with the case study of Figure 57, the Tx rise/fall time of BERT is the fastest one among the four candidates when setting the Tx EQ (de-emphasis/pre-shoot) as 0dB.
- This symptom of slow rise/fall time can be easily found in most silicon applications' Tx waveforms which data rate be equal or more than NRZ 20Gbps.

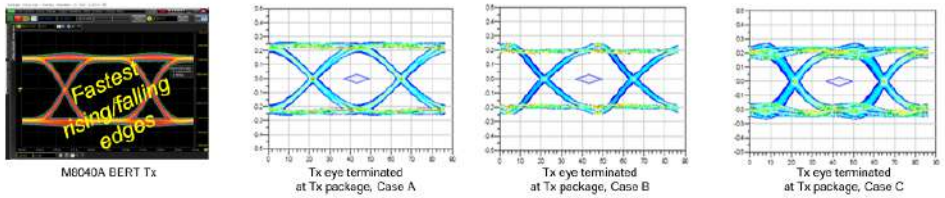


Figure 57. Tx eye performance comparisons at the location of Tx balls of BGA (@23.2960Gbps)

What to be considered when replacing BERT Tx to the silicon Tx

- By adding the -2dB TTC to the BERT Tx output, the waveform will be correlated to the silicon Tx output at BGA balls.
- *What to be noticed is that the device Rx needs to withstand total* ***-12.55dB@11.64GHz.***

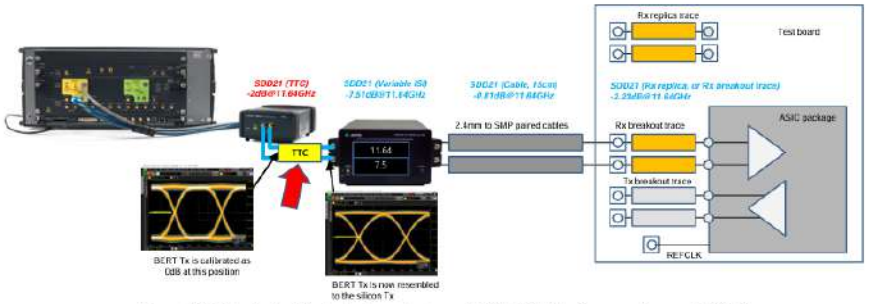


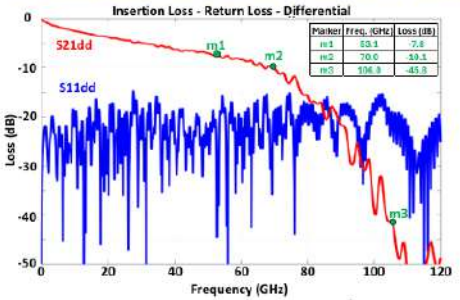
Figure 63. A typical calibrated channel setup of MIPI MPHY reference channel 1 (CH1)

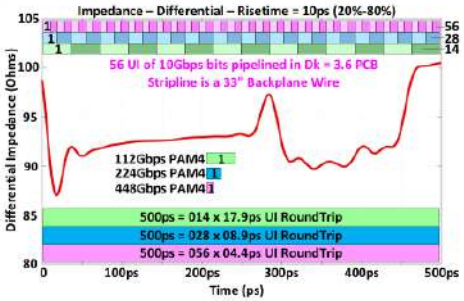
3. DesignCon 2025 자료 소개

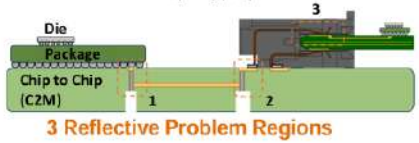
3-36 : Beyond 200G: Brick Walls of 400G links per Lane

- Brick Walls of 400G per Lane
  - AI/ML 애플리케이션은 200 Gb/s 이상의 레인당 데이터 속도를 요구
  - 400 Gb/s로의 전환은 재료, interconnect, 제조 방식 및 System topology의 발전을 필요
  - Insertion Loss 최소화 및 Impedance 제어는 고속 copper interconnect 설계의 주요 과제
  - 기존 QSFP/OSFP 커넥터는 고주파에서 공진 문제를 일으킬 수 있음

Traditional C2M Interface



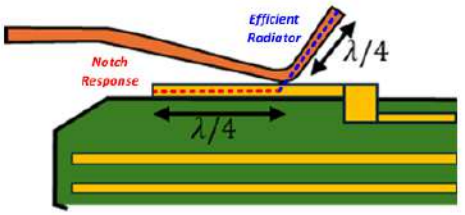


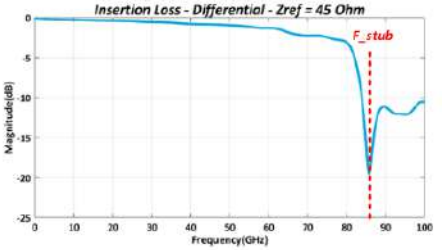


3 Reflective Problem Regions

- By 448 PAM4 UI = 4.4ps, physically short C2M topologies of inches in length have pipelined bit counts on the order of yesterday's rack scale backplanes.

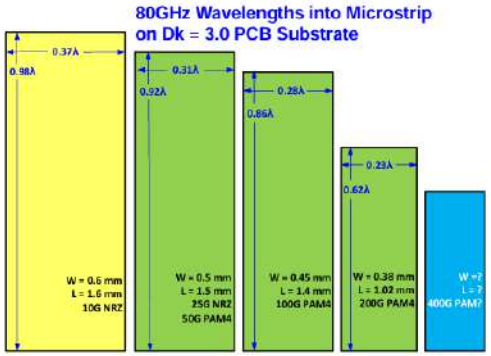
Edge Card Connector Beam To PCB Interface

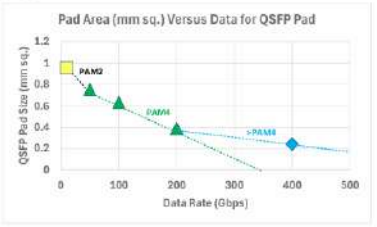




- Edge card connector beams require PCB pad and metal beam stubs to overcome mechanical tolerances and provide wipe.
  - These stubs limit achievable BW rolloff and create standing wave emitters that increase radiation and ultimately crosstalk
- Quarter wave stub brick wall from QSFP spring fingertip and PCB pad at ***F_stub***
- Shorter '*blue stub*' is occurring to the right of ***F_stub***

QSFP Pad Size versus datarate





- Simple scaling of the QSFP Pad to data rate suggests higher order modulation is required if edge card contact pitch and geometries are not physically shrunk.

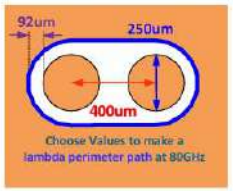
3. DesignCon 2025 자료 소개

3-36 : Beyond 200G: Brick Walls of 400G links per Lane

➢ Radiation and Resonance at High Frequencies

- 파장이 mm-wave 대역으로 줄어들면서 PCB 패턴이 주요 Radiation 및 Resonance의 원인이 될 수 있음
- PCB 접지면의 antipad는 slot안테나처럼 동작하여 신호 결합 및 재방사를 유발
- Strip line의 모드 경계가 파장에 가까워지면 방사가 발생

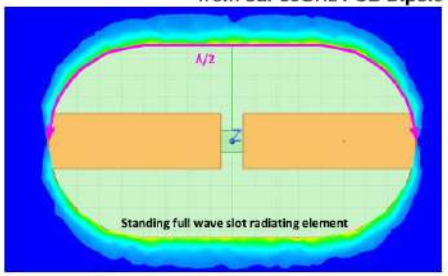
PCB Via Antipads as Slot Emitters



Feature	Technology		
	PTH	HDI	SLP
P (mm)	0.600	0.400	0.250
D (mm)	0.400	0.300	0.175
G (mm)	0.100	0.100	0.075
er	3.000	3.000	3.000
Path (mm)	3.085	2.371	1.521
Fr	56.15	73.06	113.87

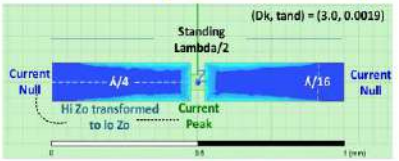
PTH = Single laminate PCB Technology
HDI = High density interconnect (stack laser drills)
SLP = Substrate like PCB

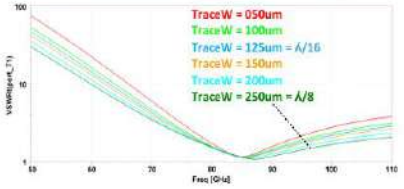
Excite the slot emitter by coupling to it from our 80GHz PCB Dipole Wires

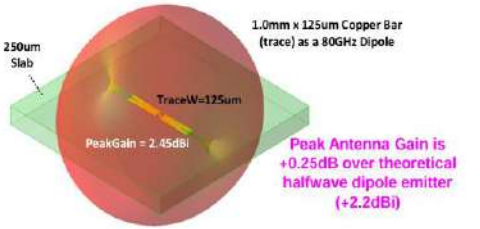


Halfwave resonance achieved between 'vertices' of the racetrack antipad

PCB Striplines as Dipoles

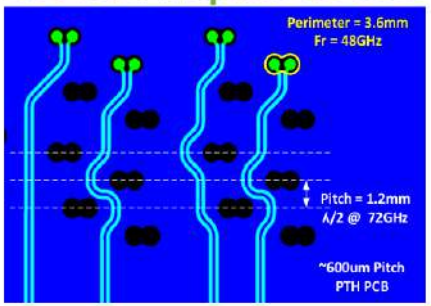




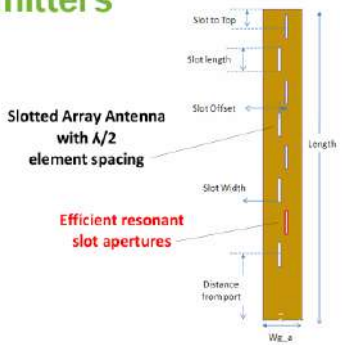


- Ask PCB interconnect radiation Questions.
  - When you act like a halfwave dipole…are you any good at it?
- By 250um trace width, standing half wave resonators have a VSWR=2 BW of 35% at ~2.5dBi antenna gain!

PCB Via Antipads as Slot Emitters

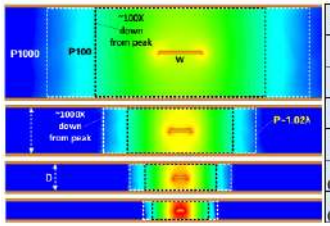


- Constructive interference from multiple emitters is possible inside PCB component footprints when the signaling pitch exceeds a half wavelength.



- Principle is exploited for high gain directional emitters in leaky waveguide arrays.

Modal Perimeter



Feature	Description
D (mm)	Ground plane to ground plane spacing
W (mm)	Stripline trace width for 50 Ohms SE
P100 (mm)	Modal perimeter path length in mm at ~40dB down from peak E-field magnitude.
P1000 (mm)	Modal perimeter path length in mm at ~60dB down from peak E-field magnitude.
P100 (80GHz λ)	P100 in fractions of 80GHz wavelength
P1000 (80GHz λ)	P100 in fractions of 80GHz wavelength

D (mm)	W (mm)	P100 (mm)	P1000 (mm)	P100 (53GHz λ)	P1000 (53GHz λ)	P100 (80GHz λ)	P1000 (80GHz λ)	P100 (106GHz λ)	P1000 (106GHz λ)
0.500	0.250	2.94	3.99	0.89	1.20	1.34	1.81	1.77	2.40
0.250	0.125	1.71	2.25	0.51	0.68	0.78	1.02	1.03	1.35
0.150	0.075	1.11	1.45	0.33	0.44	0.50	0.66	0.67	0.87
0.100	0.050	0.98	1.05	0.30	0.33	0.45	0.48	0.59	0.63

Decreasing Line Width

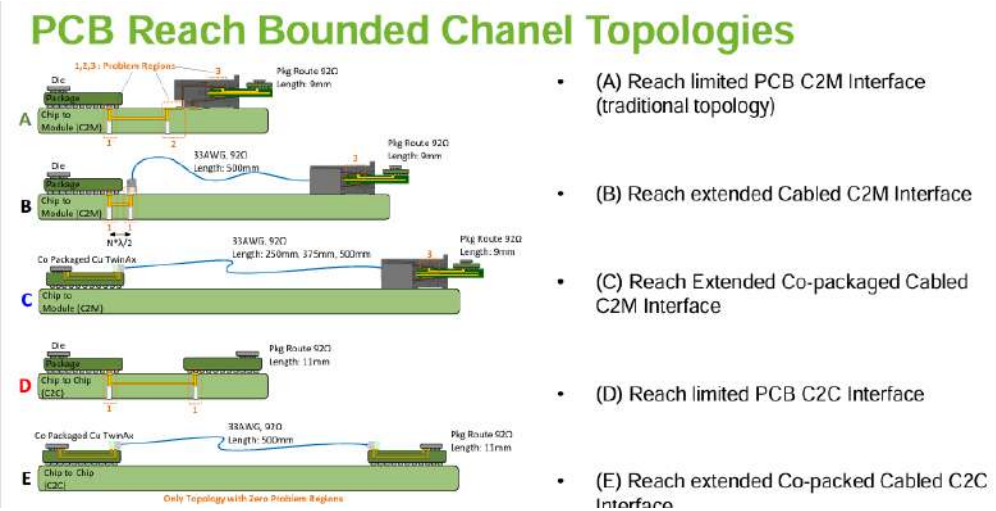
Perimeter Scale	Domain
> 1.00λ	Highly Radiative
0.5λ - 0.99λ	Leaky
< 0.5λ	Interconnect

- Concept of a stripline modal perimeter requires specifying a field strength rolloff due to open side boundaries.
- Measure the stripline modal perimeter for E-field 40dB and 60dB down from peak.
  - H-field produces identical results
- Terminating the stripline in Z-axis interconnect becomes highly radiative when the modal extents exceed wavelength dimensions.
  - Implies a forced space transformation

3. DesignCon 2025 자료 소개

3-36 : Beyond 200G: Brick Walls of 400G links per Lane

- Towards 400G and Beyond
  - 높은 레벨의 변조 방식 (PAM6 등)은 424 Gb/s가 한가지 방법이 될 수 있음
  - co-packaging twinaxcable and silicon topology는 Channel Loss와 Radiation 문제를 완화 가능
  - 212 Gb/s PAM4 이상으로 동작하는 통신 채널을 구현하기 위해 하드웨어 및 소프트웨어 양면에서 추가 연구가 필요



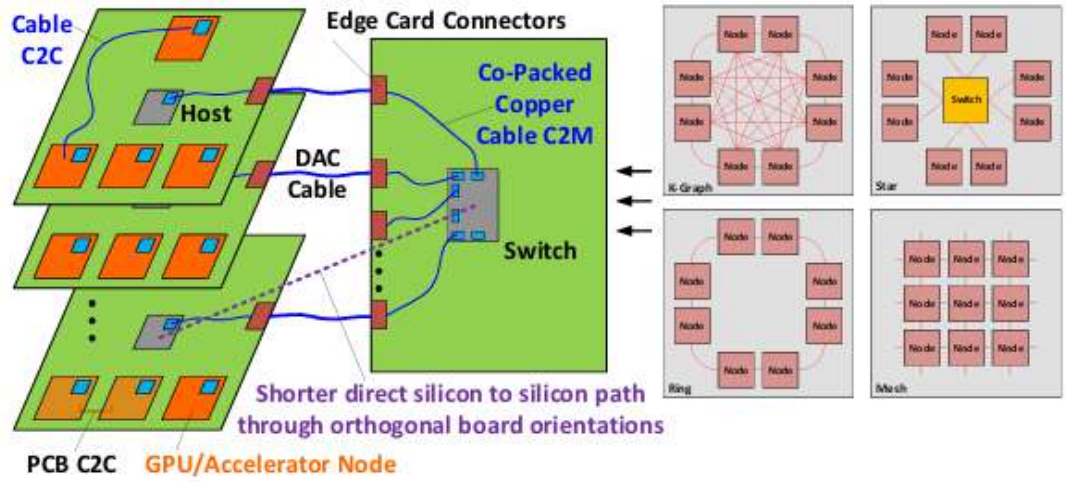


Fig. 3.2. Orthogonal Board System Concept

3-37 : Cascaded Package to PCB Channel Simulation Method Considering Different High-speed 3D Interconnect Models Extended to Higher Bandwidth up to 75 GHz

➢ Overview of High-Speed Channel Simulation and Cascading Methodology

- 고속 채널의 전체 시뮬레이션은 복잡성과 긴 시뮬레이션 시간으로 인해 어려움이 큼
- 3D FEM 시뮬레이션으로 전체 채널 분석은 비현실적인 해결책
- Cascade 방법론은 채널을 분할하여 개별적으로 시뮬레이션하고 결과를 결합하여 전체 채널을 평가
- Cascade 방법론은 최대 75 GHz 이상의 고대역폭 채널 시뮬레이션을 지원하여 고속 데이터 전송률 평가에 적합

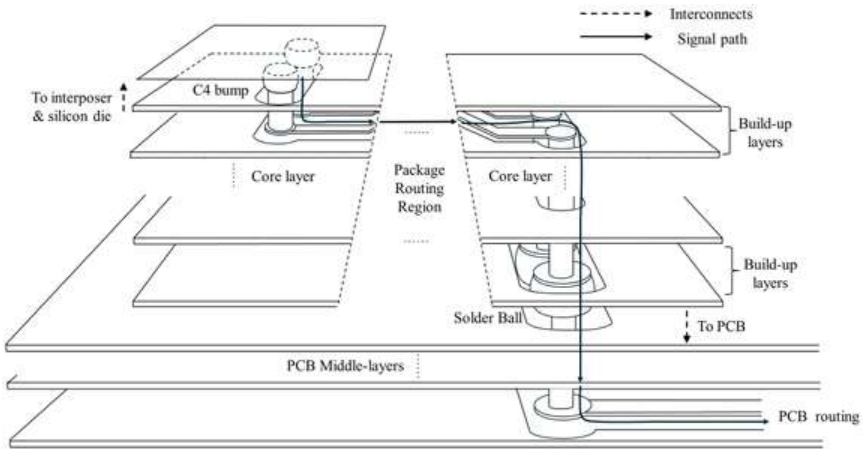


Fig. 1. An example of high-speed digital channel. The signal goes through from silicon die/interposer and t the package substrate and then to the PCB. C4 bump and BGA solder ball work as the interconnect betwee die, package substrate and PCB

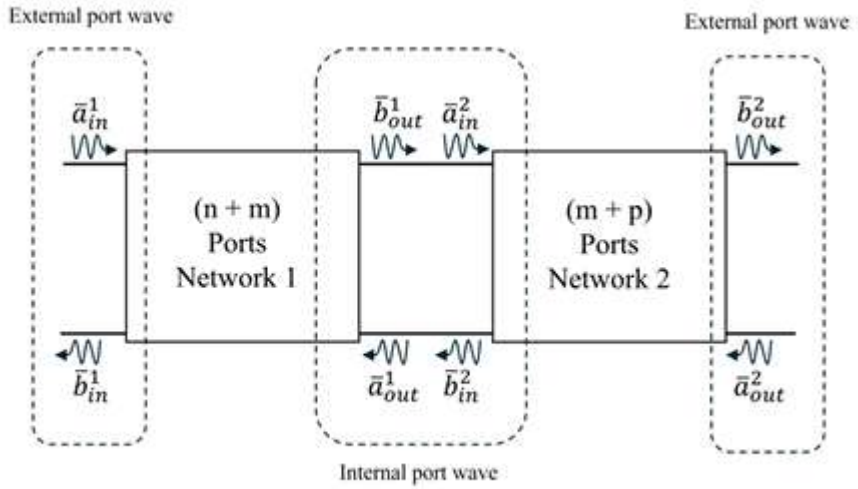


Fig. 2. Diagram for Cascading an (n + m) port network to an (m + p) port network.

3-37 : Cascaded Package to PCB Channel Simulation Method Considering Different High-speed 3D Interconnect Models Extended to Higher Bandwidth up to 75 GHz

- Inter-Connection Cascading for Discontinuous Interfaces
  - C4 bump와 solder ball은 다른 임피던스를 가지므로 연결 지점에서 파형 불연속성을 야기하여 cascade 정확도를 저해
  - 단순히 분리하여 cascade 하는 것은 이러한 불연속성을 무시하여 signal integrity simulation의 부정확성을 초래
  - Die, Package substrate, PCB 간의 연결을 정확하게 모델링을 고려 해야함

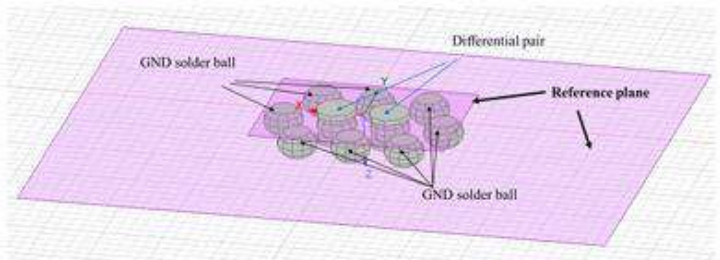


Fig. 3. Simplified solder ball-reference plane structure. A differential pair of signal solder balls surrounded by 8 GND solder balls. Top and bottom are the reference planes.

Fig. 4. Simulated wave discontinuity at the top/bottom edge on the differential signal solder balls at 75 GHz for (a) E-field, (b) H-field.

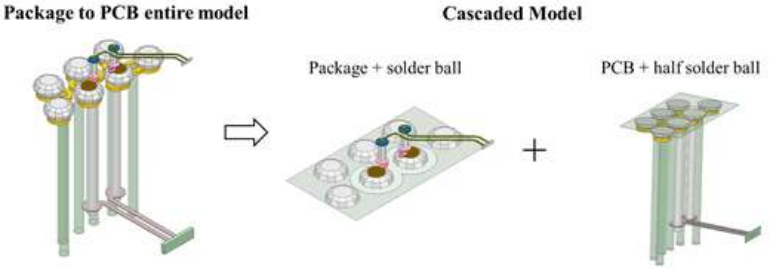


Fig. 6. Proposed cutting and cascading methodology for inter-connection. Cut at the half – solder ball to minimize the wave discontinuity.

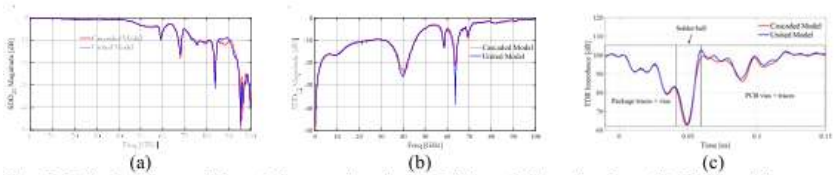


Fig. 7. United and cascaded model comparison for (a) Differential insertion loss, (b) Differential return loss, (c) TDR impedance when rise time is 6.25 ps. Results show good match in frequency domain for both differential insertion loss return loss up to 85 GHz. Slight but negligible impedance mismatch shows at the solder ball.

3-37 : Cascaded Package to PCB Channel Simulation Method Considering Different High-speed 3D Interconnect Models Extended to Higher Bandwidth up to 75 GHz

➢ Applications of Intra-Connection Cascading and Summary

- Package substrate 내부의 Trace, via 등 각 서브 디자인 내의 연결을 단순화하여 시뮬레이션 효율성을 높임
- Cascade 방법은 대규모 모델 시뮬레이션의 메모리 요구량을 줄이고, 빠른 평가, 고속 채널 시뮬레이션, 효율적인 문제 해결을 지원하지만, 불연속 지점에서 부적절한 절단은 부정확한 결과를 초래할 수 있음을 유의

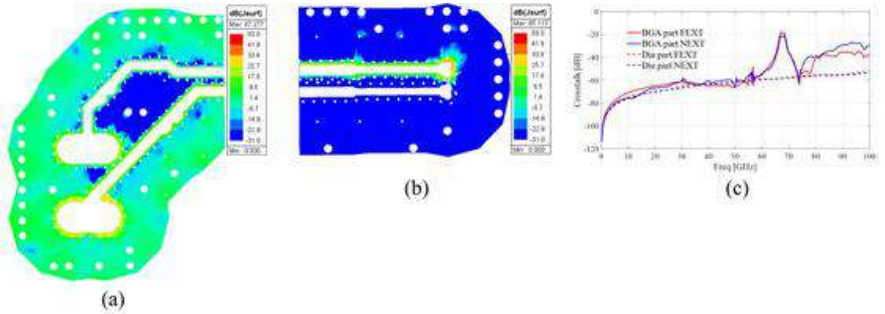


Fig. 16. Cut the design into solder ball part and die part separately to do crosstalk troubleshooting. (a) Complex value of surface current plot on the solder ball part at 66.8 GHz (source excitation at solder balls) (b) Complex value of surface current plot on the die part at 66.8 GHz (source excitation at die) (c) FEXT plot and NEXT for both solder ball and die in frequency domain

TABLE II. TIME AND MEMORY USAGE FOR BOTH METHODS

Method	Time	Max. Memory Usage
3D full-wave whole channel simulation	More than 75 h	388 GB
3D full-wave simulation on C4 bump part	15 h 6 min	131 GB
3D full-wave simulation on middle part	15 h 44 min	170 GB
2D cross-section anaylsis on middle part	6 min	60 MB
3D full-wave simulation on solder ball part	6 h 18 min	84.4 GB

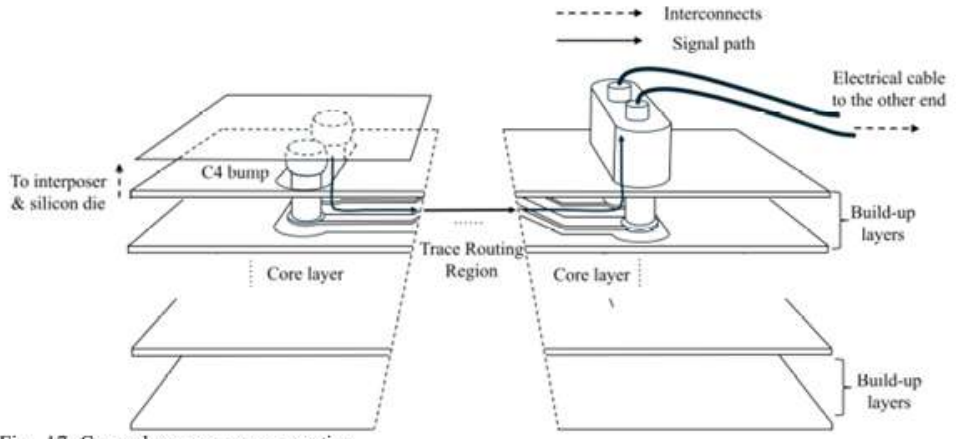


Fig. 17. Co-package copper connection.

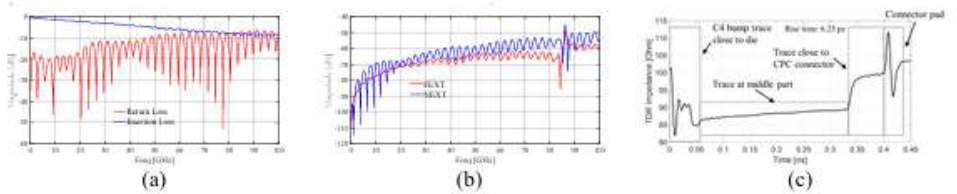


Fig. 18. Evaluation on the co-package copper application from die to CPC connector at one end regarding (a) Insertion and return loss. (b) FEXT and NEXT, (c) TDR impedance when rise time is 6.25 ps.

3-38 : Differential Skew Mitigation Technique Results

- Differential Skew Mitigation in High-Speed Interconnects
  - 고속 인터페이스(112 Gbps PAM4, PCIe Gen 7)는 strict channel skew tolerance를 가짐
  - Fiber weave skew는 PCB 재료의 비균질 유전율로 인해 발생하며 effective dielectric constant differences between differential lines를 유발
  - 기존의 스큐 완화 기술(image rotation, angled routing)은 cost increase, routing complexity, or space constraints와 같은 단점
  - aligning the trace pitch to the underlying glass fabric fiber-weave pitch하는 skew 완화 기술소개

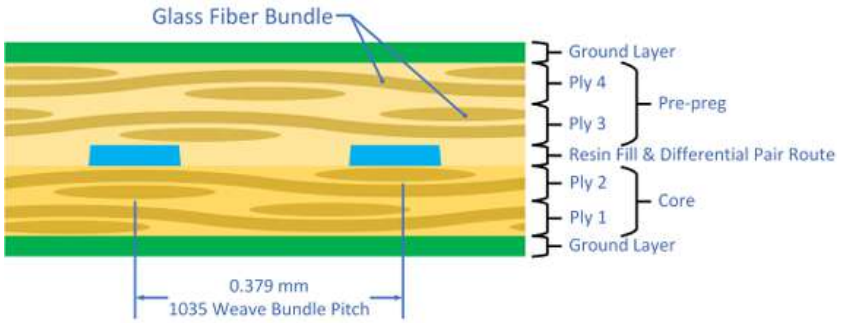


Figure 1: PCB Stackup Cross-Section Showing Fiber Bundles

Glass Style	Reference Thickness	Weave Pitch		
		Warp	Weft	Average
1035	0.028 mm	0.385 mm	0.373 mm	0.379 mm
1078	0.043 mm	0.469 mm	0.469 mm	0.469 mm

Table 1: Glass Weave Properties (IPC-4412C, Appendix B, Table B-1)

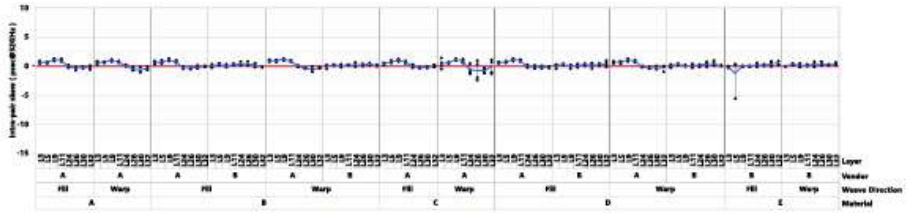


Figure 7: Differential Skew at 85 Ω on 5-inch Delta-L Coupon.

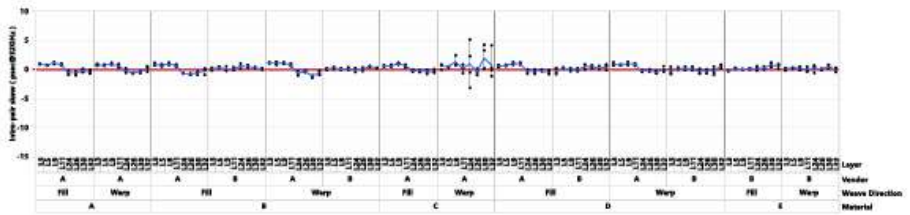


Figure 8: Differential Skew at 85 Ω on 10-inch Delta-L Coupon.

3-38 : Differential Skew Mitigation Technique Results

➢ Weave Pitch Alignment Technique and Test Setup

- Differential pitch equal to weave pitch는 더 넓은 트레이스 폭을 가능하게 하여 loss reduction에 유리
- 1035 glass weave는 high resin content, smaller pitch, availability from various vendors 등의 이점을 가지므로 선택
- Delta-L coupons을 사용하여 다양한 PCB 재료와 제작 업체의 skew 및 insertion loss를 측정

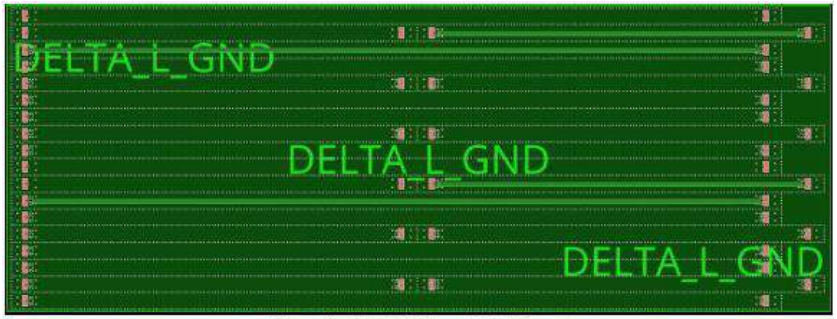


Figure 2: Delta-L Differential Pair Layout

Fabrication Vendor	Material Vendor	Material Model	Panels
A	Same material vendor	B	4
		C	4
		D	4
	A	A	4
B	B	B	4
	D	D	4
	E	E	4

Table 2: Material Matrix

HSIO Layers (8)	Orientation (2)	Delta-L per Panel	Panels	Measurements per Material-Fab
L3, L5, L9, L11 L24, L26, L30, L32	Warp Weft	16	4	64

Table 3: Coupon Quantities for Each Material

Fabrication Vendor A			
Material	**Lamination**	**Glass Type**	**Thickness**
A	Core	1035x2 RC68	0.10 mm
	Prepreg	1035x2 RC74	0.12 mm
B	Core	1035x2 RC66	0.10 mm
	Prepreg	1035x2 RC75	0.12 mm
C	Core	1078x1 RC74*	0.10 mm
	Prepreg	1035x2 RC76	0.12 mm
D	Core	1035x2 RC67	0.10 mm
	Prepreg	1035x2 RC75	0.12 mm

Table 4: Fabrication Vendor A Stackup Details

3-38 : Differential Skew Mitigation Technique Results

- Measurement Results and Conclusion
  - Routes with 1035 weave aligned는 ±2 ps 미만의 skew를 보임
  - Routes using 1078 weave는 최대 7-8 ps 의 skew 분포

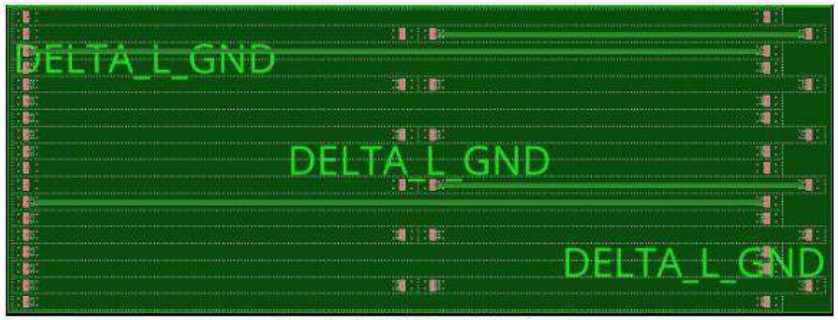


Figure 2: Delta-L Differential Pair Layout

Fabrication Vendor	Material Vendor	Material Model	Panels
A	Same material vendor	B	4
		C	4
		D	4
		A	4
B	B	B	4
	D	D	4
	E	E	4

Table 2: Material Matrix

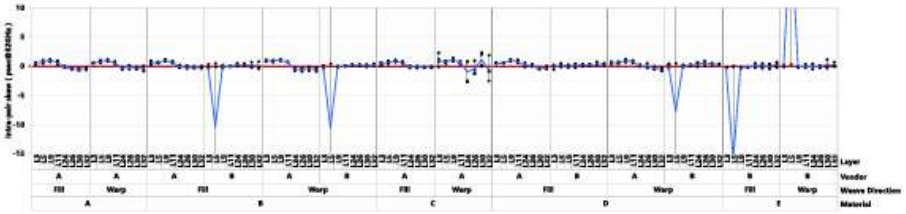


Figure 9: Differential Skew at 90 Ω on 5-inch Delta-L Coupon.

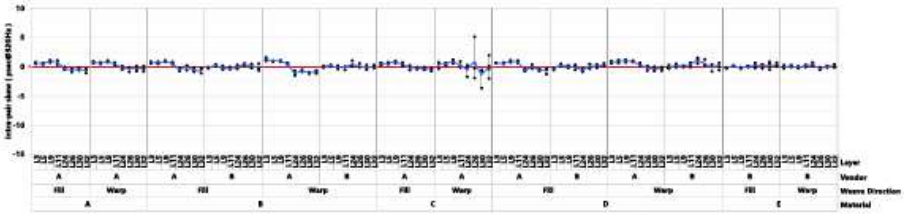


Figure 10: Differential Skew at 90 Ω on 10-inch Delta-L Coupon.

3. DesignCon 2025 자료 소개

3-39 : How understanding anisotropic materials and tolerances could increase performance at 112/224Gbps and beyond

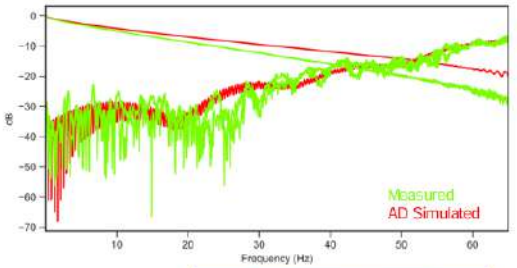
➢ Discrepancy Between As-Designed and As-Fabricated Hardware

- As Designed 정보는 통상적인 가정(datasheet, 경험, ECAD 레이아웃, PCB 제조사 stackup 등)에 기반
- As Fabricated 하드웨어는 에칭, 선폭 및 간격, 레이어 정합 등의 기하학적 불확실성을 포함
- As Designed과 As Fabricated 간의 차이는 insertion loss 마진에 영향을 미치며, PCB material anisotropy를 중요하게 고려
- As Designed와 As Fabricated 간의 차이점, anisotropy의 영향, AI 기반 재료 식별, 설계 공차에 따른 전기적 성능 변화를 분석함

AS DESIGNED (simulated) VS AS FABRICATED (measured)

- Sample correlation for 70GHz Platform
- Simulation done based on best available information for sign-off in a typical design process
- Very good correlation on return loss
- Insertion loss suffers due to uncertainty mostly in surface roughness
- How much insertion loss margin are you willing to allocate to such gap in your system budget?

8" Stripline, Full Path

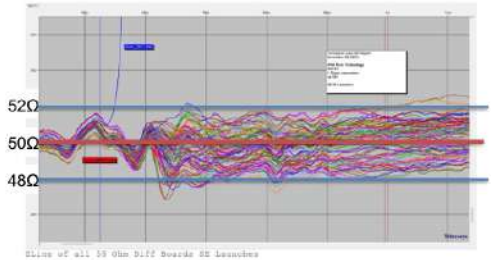


Hausdorff Figure of Merit			
	0-10GHz	0-35GHz	0-50GHz
S	62.4	61.8	63.3

DIGITAL TWIN CHALLENGES

- It is unrealistic to assume what we simulate and what we fabricate are identical
- Digital Twin is challenged by 3 factors
  1. As Designed inputs different from as fabricated board
  2. Distribution of parameter variation not captured
  3. Many physical effects are not modeled
- Matching a specific channel we term **microscopic SI**, the variation in distribution of the channels is what we term **macroscopic SI**

Measured TDR of multiple launches on platform

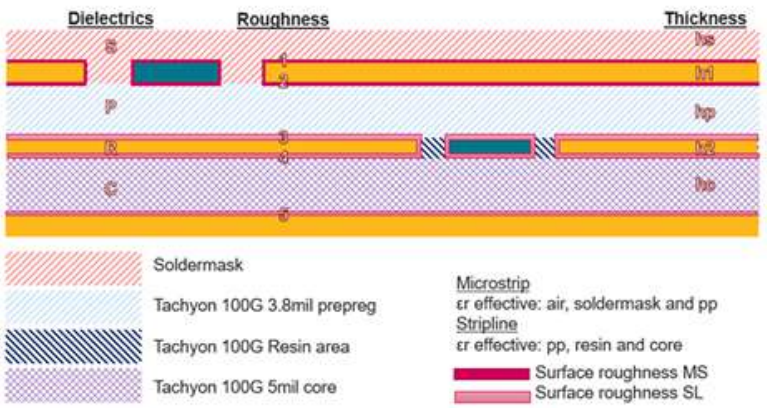


3-39 : How understanding anisotropic materials and tolerances could increase performance at 112/224Gbps and beyond

➢ Impact of Manufacturing Variations and Material Properties

- 디지털 트윈은 As Designed 입력과 As Fabricated 보드의 차이, 파라미터 변화 분포 미반영, 물리적 효과 모델링 부족으로 인해 어려움을 겪음
- 데이터시트에서는 하나의 symmetric Dk 값을 가정하지만, PCB는 면 Dk와 수직 Dk의 단축 이방성을 가짐
- 비아는 상당한 수직 전기장을 가지므로 수직 Dk 값이 면 Dk 일반적으로 높다는 점이 중요
- 재료 식별은 플랫폼 측정을 기반으로 싱글 엔드 전송 라인을 사용하며, 코어, 표면 거칠기 등 고려

MATERIAL FITTING ASSUMPTIONS



- Cross-section
  - Assumed height from x-section report (test strip)
  - Separated core and prepreg Dk
  - Different surface roughness for outer layers vs inner layers but not distinguishing between drum/rough sides
- Materials
  - Djordjevic Sakar 1GHz, Df from datasheet. Bulk isotropic
  - Huray Cannonball
- Optimize parameters to measured complex IL to 50GHz for both SL and MS simultaneously

3. DesignCon 2025 자료 소개

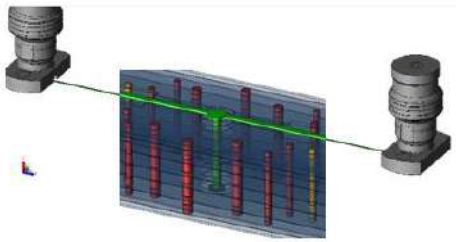
3-39 : How understanding anisotropic materials and tolerances could increase performance at 112/224Gbps and beyond

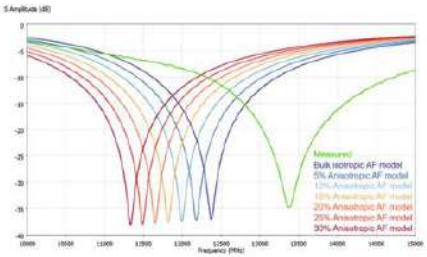
➢ Material Identification and Anisotropy Effects

- 비등방성은 면내 커패시턴스를 증가시켜 누화를 증가시키므로, 등방성 Dk만 사용하면 Crosstalk를 놓칠 수 있음

ANISOTROPIC RESONATOR

- Via hanging off trace has been discussed as a potential way to identify anisotropy*





Resonance frequency from bulk isotropic material fit was off by 1 GHz from measured (12.4 vs 13.4 GHz)

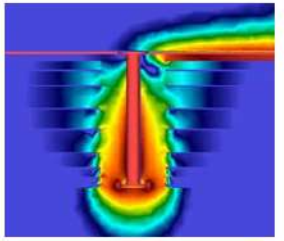
- Both isotropic Dk and anisotropic Dk pulls resonance further away roughly by 1.5% per 5% increase
- Macroscopic SI factors influence the resonant frequency

* S. McMorrow, E. Syre, . C. Nwachukwuzun and . D. Blackenship, "Anisotropic Design Considerations for 28GBs Via to stripline transitions," in *Designcon 2017*, Santa Clara, 2015.

VARIATION WITH GEOMETRY

- Why is the bulk Dk model so far off (1 GHz)?
  - A field plot shows significant field density around bottom pad and plane clearances – extra capacitive loading…
- We can explore sensitivity of the manufacturing variation using a digital twin
- With typical production tolerance on pad, clearance and drill we see more change with geometry than by Λ (only 0.2 GHz shift with 5% anisotropy)

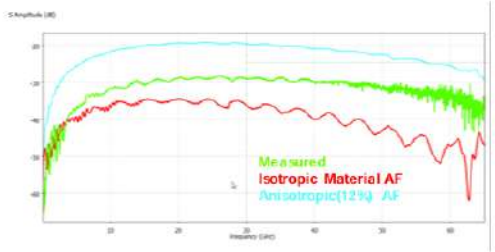
Electrical Field at resonance



	Nominal	Antipad low bound	Antipad high bound	Drill offset	Pad on outer layers low bound	Pad on outer layers high bound
Resonance freq[GHz] (sim)	12.37	11.79	13.26	~12.3	12.75	11.97
Δ to nominal simulation case GHz	0	-0.58	0.89	-0.04 to -0.07	0.38	-0.4
Δ to nominal simulation case %	0	-4.7	7.2	-0.3 to -0.6	3.1	-3.2

ANISTROPY AND FAR END CROSSTALK (S41)

- Anisotropy increases the in-plane capacitance – so increases crosstalk
  - Using only an isotropic material Dk underestimated the crosstalk
  - Also sensitive to inhomogeneous Dk, less to geometry
  - Fruitful area for future exploration



Hausdorff Figure of Merit			
	0-10GHz	0-35GHz	0-50GHz
S	95.2	94.3	92.5

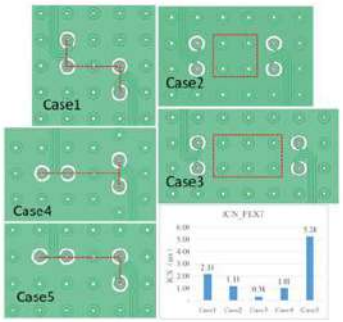
Hausdorff Figure of Merit			
	0-10GHz	0-35GHz	0-50GHz
Isotropic (AF)	90.3	87.6	88.5
Anisotropic 12% (AF)	78.2	59.4	65.8

3-40 : Innovative Design of 224G BGA Pinmap and Via Structure

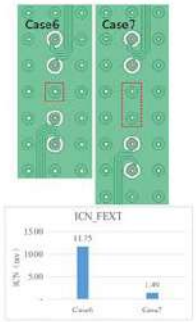
➢ Challenges and Initial Solutions
- High-speed serial signal rate가 224Gbps에 도달, 448Gbps로 발전 중
- Data rate 증가로 system channel의 higher bandwidth와 lower crosstalk 요구
- Traditional BGA design은 bandwidth 한계와 crosstalk 문제에 직면

Classifications of FEXT (Far-End Crosstalk)

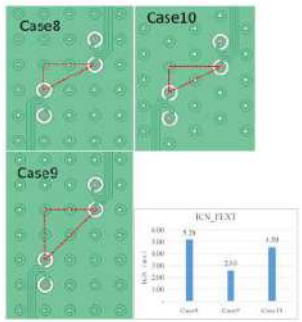
- Based on the different relative positions of the two differential vias, crosstalk can be classified into three categories (pitch = 0.8mm, diameter of via = 0.15mm)



Two differential vias in the same row



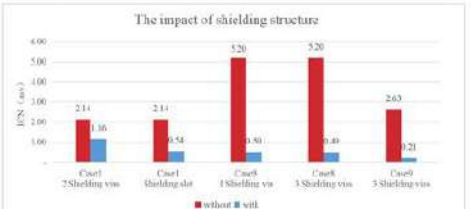
Two differential vias in the same column

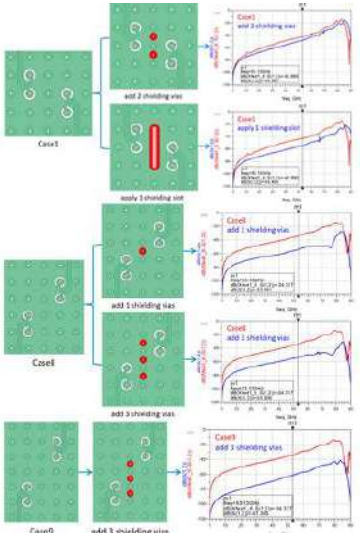


Two differential vias in diagonal positions

Impact of Shielding Structures

- Shielding Structures: (Case1)
  - Though shielding slot gives better improvment than shielding vias
  - Shielding vias is prefered due to less process difficulties
- Number of Shielding Vias: (Case8, Case9)
  - Adding one shielding via improves the ICN nearly as much as adding three
  - Shielding vias should be prioritized on the shortest coupling path





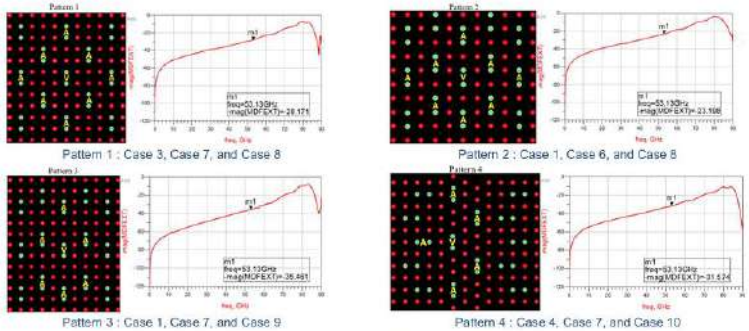
3-40 : Innovative Design of 224G BGA Pinmap and Via Structure

- Innovative BGA Pinmap Design
  - P/N 신호 간 거리 및 signal/ground via 간 거리가 감소하면 bandwidth 증가
  - 다양한 BGA via 배열 (same row, column, diagonal)에 대한 crosstalk 분석 진행
  - Shielding ground via 및 slot 구조는 crosstalk 감소에 significant한 개선 효과
  - Via-pad offset을 적용한 novel BGA via pattern은 high bandwidth, low crosstalk, high density 달성

Combinatorial Approach

* V: Victim pair
* A: Aggressor pair

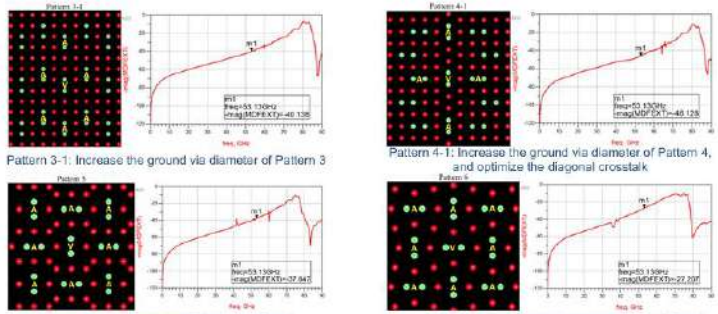
- Based on the study in previous slides, various BGA via patterns are analyzed using a combination approach
- The PS-FEXT (Powersum Far-End Crosstalk) of Pattern 3 and Pattern 4 is relatively small



Pattern 1 : Case 3, Case 7, and Case 8
Pattern 2 : Case 1, Case 6, and Case 8
Pattern 3 : Case 1, Case 7, and Case 9
Pattern 4 : Case 4, Case 7, and Case 10

Optimization

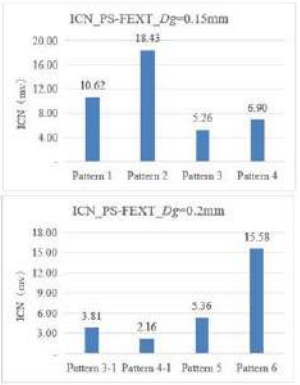
- Two approaches: (1) increse the diameter of ground vias from 0.15mm to 0.2mm; (2) optimize the via pattern
- For Case4 with significant crosstalk advantages, supplementary analysis is conducted in an orthogonal manner



Pattern 3-1: Increase the ground via diameter of Pattern 3
Pattern 4-1: Increase the ground via diameter of Pattern 4, and optimize the diagonal crosstalk
Pattern 5: The first orthogonalization of Case4
Pattern 6: The second orthogonalization of Case4

ICN_PS-FEXT of BGA Via Patterns

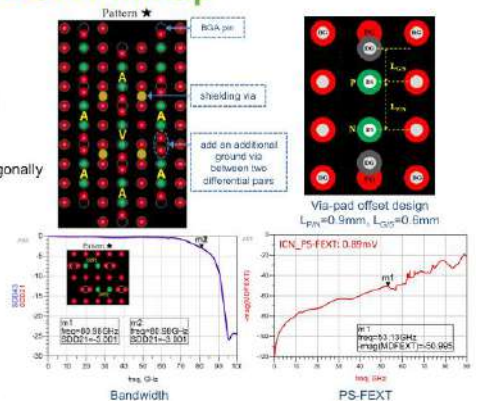
- After increasing ground vias diameter and optimizing differential vias arrangement, the crosstalk of Pattern 3-1 and Pattern 4-1 has significantly improved
- In the orthogonal design, the diagonal crosstalk of Pattern 6 is larger than that of Pattern 5



* PS-FEXT: Powersum Far-End Crosstalk
* *Dg*: Diameter of GND Vias

A Recommended Novel BGA Pinmap

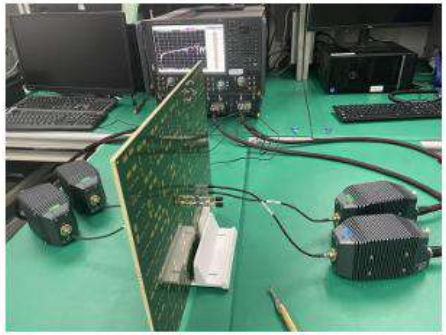
- Pattern★: Apply Via-pad Offset Design
  - White circles indicate BGA pins
  - Add a ground via in the same column after offsetting
  - Use Case 1 between the same rows
  - Add a shielding via on the shortest coupling path diagonally
- Achieve A Balanced Performance:
  - High bandwidth: 80.98GHz
  - Low crosstalk: 0.89mV
  - High signal via density: Number of differential pairs in 10 rows x 10 columns is 15
  - Good soldering reliability: Pitch of BGA pin is 0.9mm



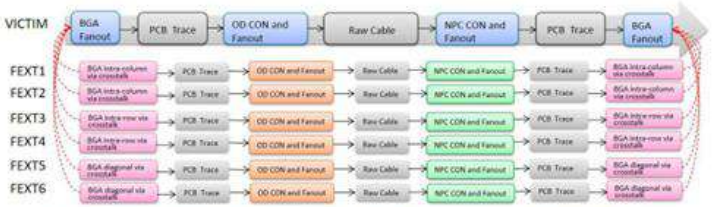
3-40 : Innovative Design of 224G BGA Pinmap and Via Structure

➢ Innovative Via Structure for Higher Speeds

- Future 448Gbps 이상의 system은 bandwidth 및 impedance continuity의 추가적인 향상 요구
- Innovative via structure는 ground via와의 거리를 줄이고 flexible한 impedance tuning 가능
- 본 구조는 bandwidth (최대 92GHz) 향상 및 impedance continuity와 reliability 개선
- 224Gbps system에 BGA pinmap 적용 결과, crosstalk ICN 약 97% 감소 및 COM 약 17% 증가 달성



Test topology and configuration

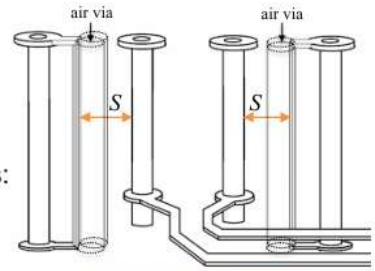


A 224G system ball to ball passive link with an insertion loss of 28 dB

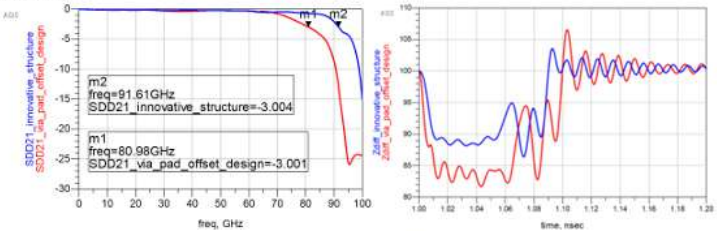
	Conventional	Pattern ★	Improvement percentage
ICN_PSFT (only BGA)	31.38mv	0.89mv	97.2%
ICN_PSFT (28dB attenuate)	1.54mv	0.04mv	97.4%
COM	2.93dB	3.45dB	17.7%

An Innovative Via Structure

- In the PCB process, the ground-to-signal via spacing, is restricted by the CAF process, cannot be reduced all the way, limiting via-pad offset structure bandwidth
- An Innovative Via Structure for 448Gbps and Higher Data Rates:
  - Reduce the distance between the ground vias and the signal via walls
  - Enhance PCB CAF performance: Air vias for isolation
  - Increase the signal via pitch can further enhance solder reliability
  - Adjust distance *S* to modify signal via impedance
  - Compatible with traditional processes
- Improvements:
  - Bandwidth: 80.98GHz → 91.61GHz
  - TDR: 85Ω → 90Ω
  - ERL: 20dB → 23dB



The innovative via structure



3-41 : Insertion Loss of Mechanically Roughened Conductors

- Introduction & Test Structure
  - 과도한 전송 선로 손실의 두 가지 가설: Conductor roughness, lossy dielectric coatings.
  - Conductor roughness 가설: 표면 불규칙성이 전자 전파 경로를 길게 만듦.
  - Lossy dielectric 가설: 얇은 유전체 코팅이 삽입 손실을 증가시킴.
  - 화학적 처리 없이 기계적 방법으로만 변화시킨 도체 거칠기가 삽입 손실에 미치는 영향 평가

Figure 1: Copper wire being rolled in a jeweler's rolling mill.

Figure 4: Conductor cross sections for the Smooth (left) and Diamond (right) conductors.

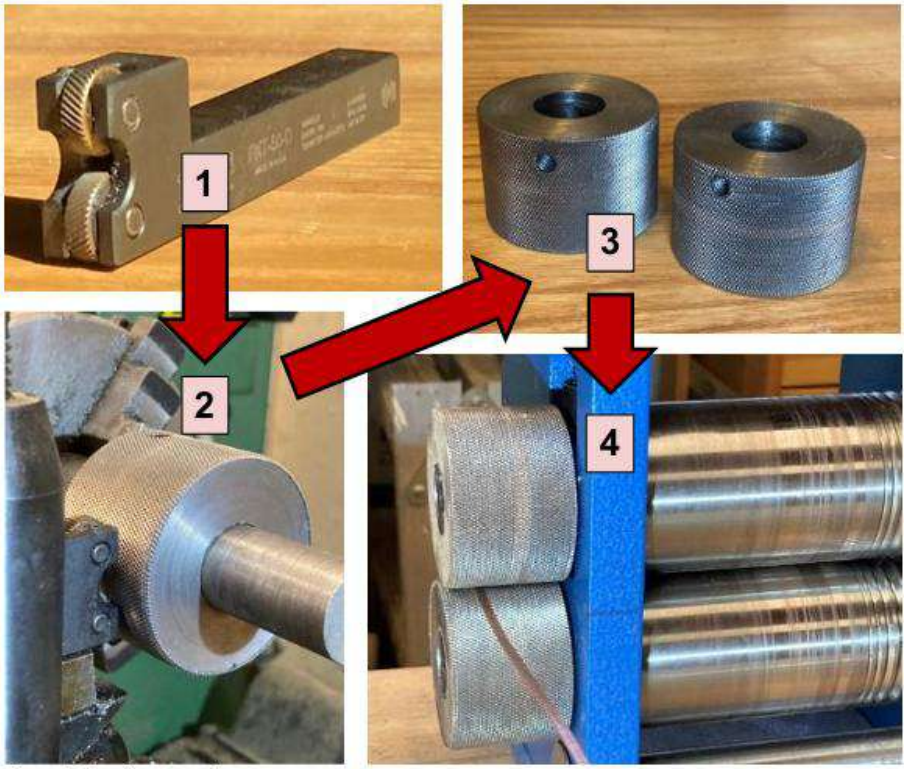


Figure 2: Conductor roughening process.

3-41 : Insertion Loss of Mechanically Roughened Conductors

- Measurements & De-embedding
  - 측정 주파수 범위: 30kHz – 1.5GHz 및 10MHz – 40GHz.
  - Test structure: 화학적 처리를 최소화한 Stripline 구조.
  - 디임베딩 목적: 측정 포트의 임피던스 부정합 및 지연 등의 영향 제거.
  - 주요 디임베딩 요소: Connector delay, launch inductance, launch capacitance, mounting nut cavity

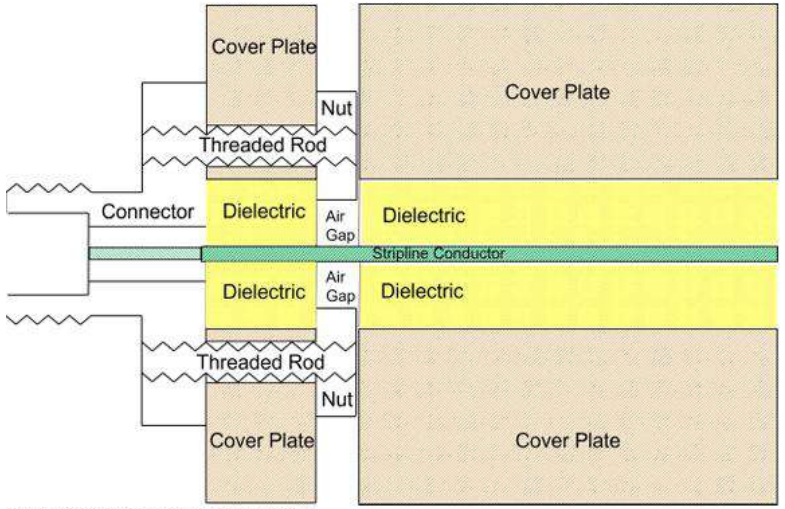
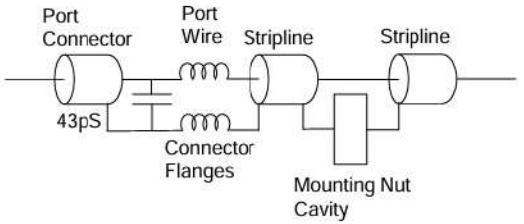


Figure 7: Coaxial connector edge mounting

Measurement Port Equivalent Circuit



Method:

1. Adjust port model to match beginning of TDR trace.
2. Convert S parameters to generalized matrix (ABCD) matrices.
3. Multiply by inverse ABCD matrix of port model.
4. Convert back to S parameters.

Test Conductor	Port	Delay adjustment	Inductance	Capacitance
Smooth	1	-2.29E-12	1.60E-10	0.00E+00
	2	0.00E+00	3.80E-10	0.00E+00
Diamond	1	0.00E+00	4.10E-10	0.00E+00
	2	-7.00E-13	2.70E-10	0.00E+00
Cross Direction	1	0.00E+00	5.70E-10	0.00E+00
	2	7.50E-13	5.60E-10	0.00E+00
Propagation Direction	1	-5.60E-12	3.70E-10	1.50E-13
	2	-7.60E-13	3.30E-10	0.00E+00

3-41 : Insertion Loss of Mechanically Roughened Conductors

- Conclusions & Recommendations
  - 측정된 삽입 손실: 매끄러운 구리 도체 예상 손실의 약 2배
  - 기계적 거칠기의 영향: 다양한 패턴 간의 삽입 손실 차이는 크지 않음
  - Work hardening 가능성: Rolling 과정에서 발생한 Work hardening이 손실 증가의 원인일 수 있음
  - 권장 사항: 고속 데이터 전송 선로에 Rolled, annealed copper 사용 및 PCB 제조 시 화학 물질 관리 중요

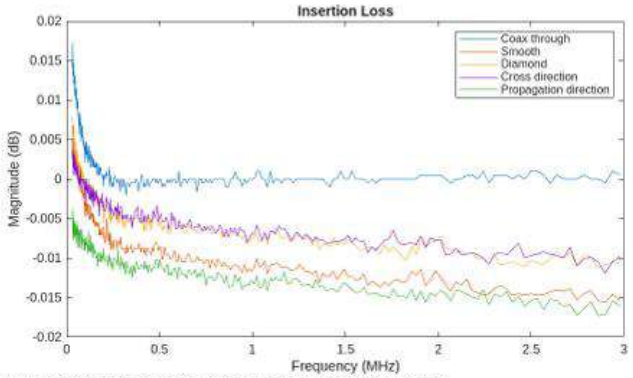


Figure 10: Magnified view of low frequency insertion loss, starting at 30kHz

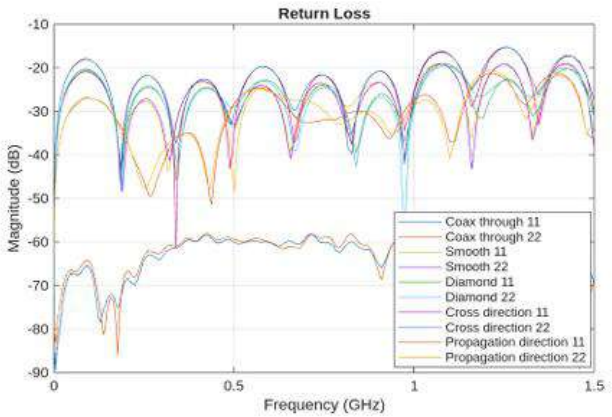
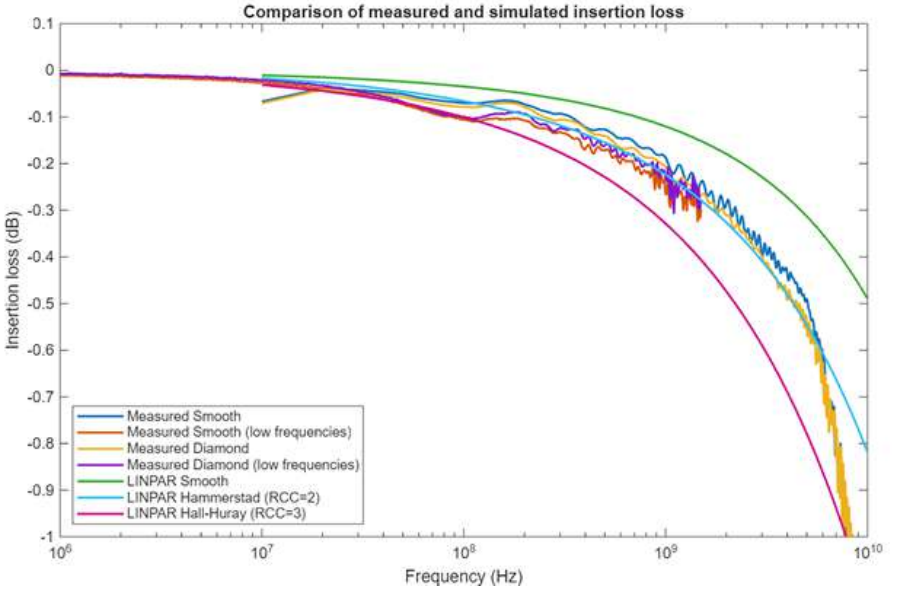


Figure 11: Low frequency return loss

Measured Data vs. Conductor Roughness Calculations



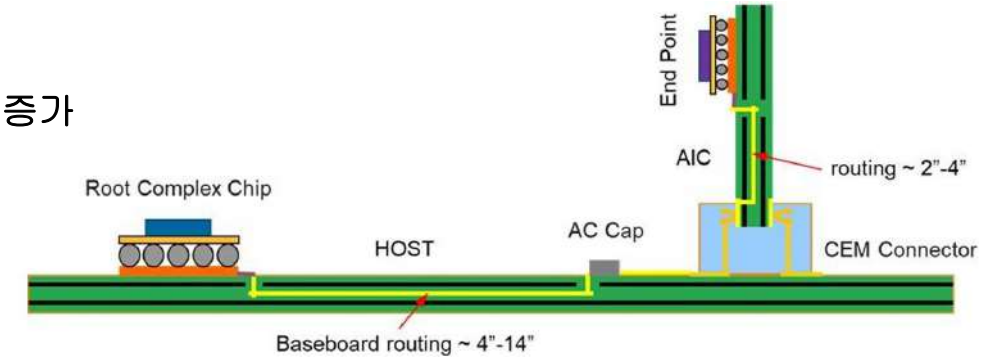
3-42 : PATH TO PCIE GEN 7.0: CHALLENGES AND DESIGN CONSIDERATIONS FOR NEXT GENERATION INTERNAL CABLING (1/2)

PCIe Gen 7.0의 필요성

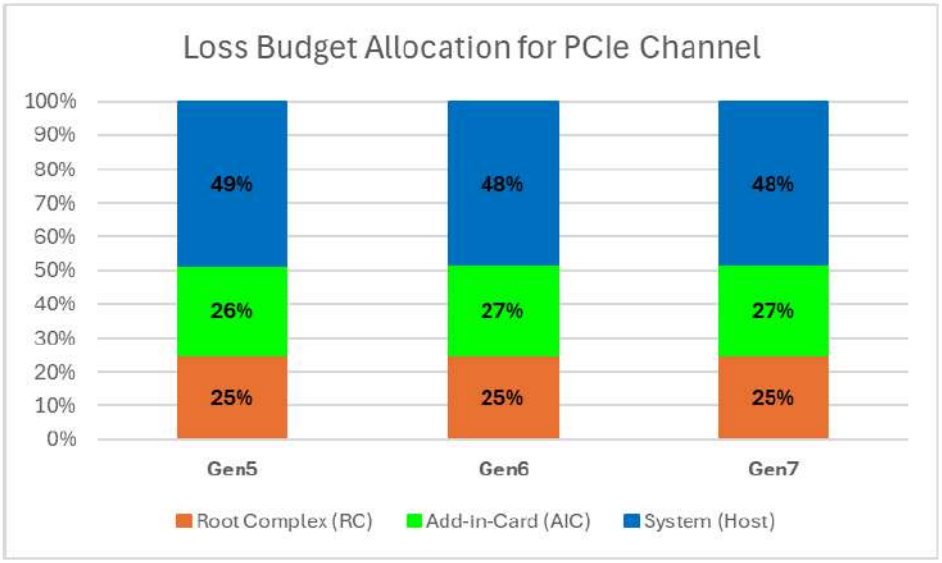
- AI/ML, HPC에서 높은 대역폭과 낮은 지연시간 요구
- 128GT/s (PAM4 신호 방식), 기존 NRZ 대비 속도 2배 증가
- 신호 무결성 유지 필요 (BER<1e-06)

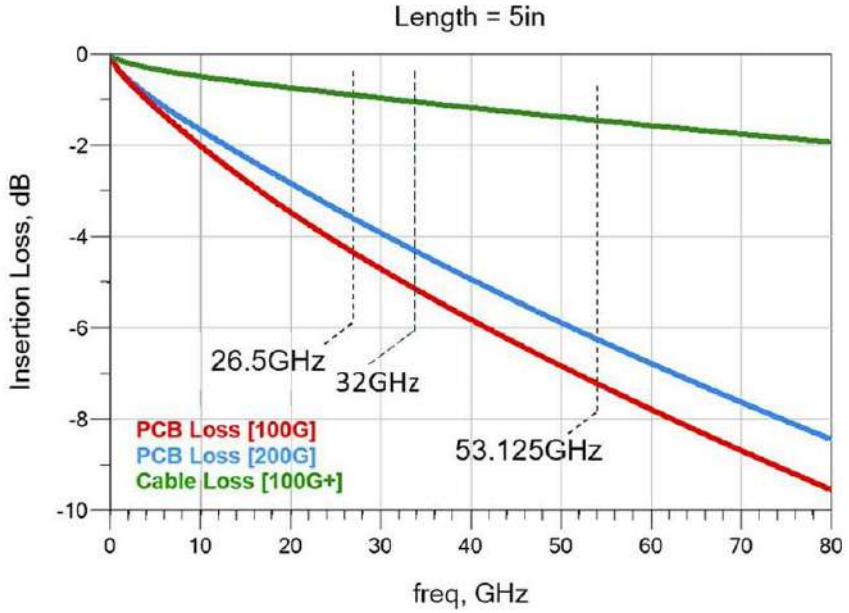
설계 고려사항

- 신호 열화 요소
  - 온칩 기생 효과, 반사, 비아 손실, 크로스톡
- 내부 케이블 중요성
  - PCB 대비 낮은 신호 손실



[PCIe Pad to Pad Channel]

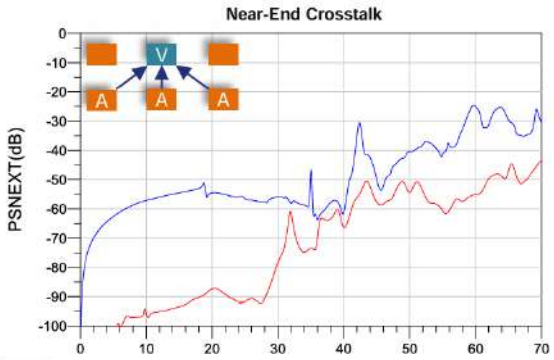


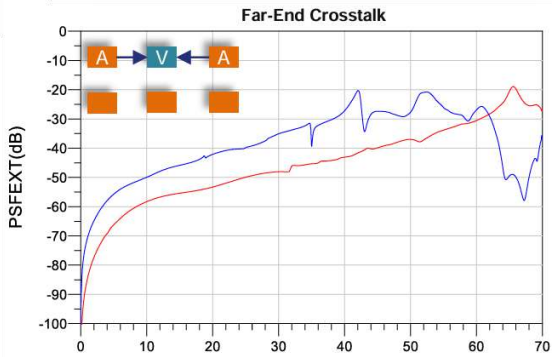


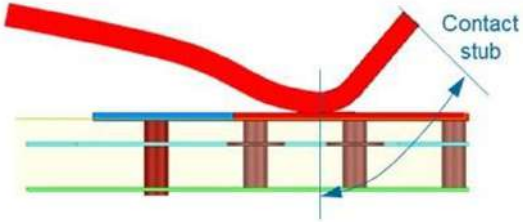
3-42 : PATH TO PCIE GEN 7.0: CHALLENGES AND DESIGN CONSIDERATIONS FOR NEXT GENERATION INTERNAL CABLING (2/2)

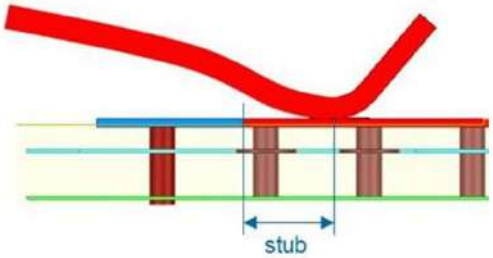
Signal Integrity(SI)의 주요 문제

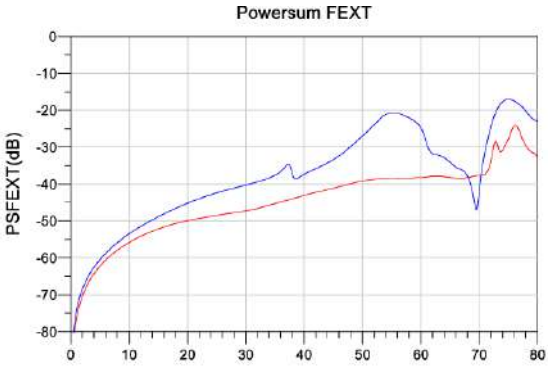
- PAM4 크로스톡 문제
  - 기존 PCIe Gen 6 설계의 차폐 및 접지 부족
- 접지 공진 문제
  - 반사 신호에 의해 공진 현상 발생
- PCB 기반 인터페이스 한계
  - PCB 패드 스텁 > 신호 반사 및 삽입 손실 증가

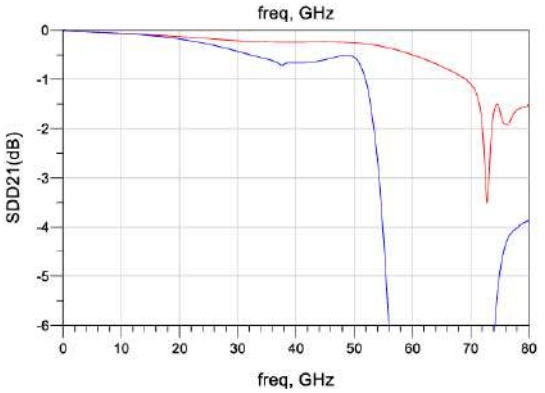








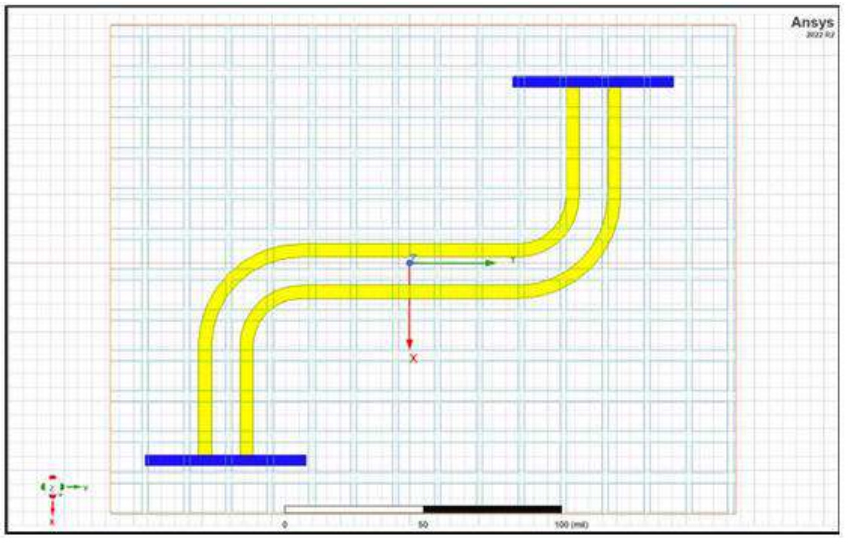


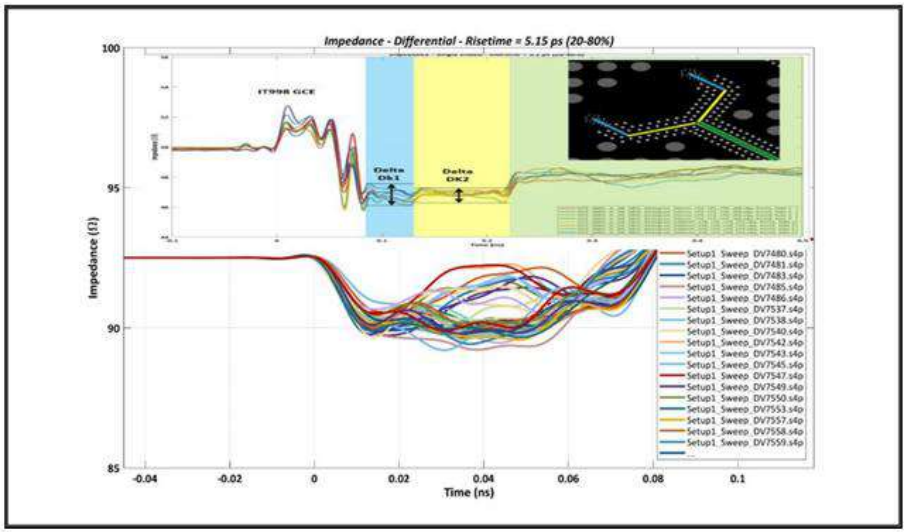


3-43 : Reduced Order Geometric Macro Model of PCB Fiberglass Spatial Variation for Skew and Impedance Prediction (1/2)

PCB 유리섬유(Fiber Weave) 구조

- Warp 방향은 섬유가 더 조밀하고 Fill 방향은 균일하게 퍼지는데, 이로 인해 X,Y 방향에 따라 유전율(Dk) 및 신호 속도가 달라서 차동 신호 간 Skew 발생
- 유리섬유 영역을 나누고, 각각의 구간의 평균 유전율을 계산하여 TDR/Skew 시뮬레이션 수행

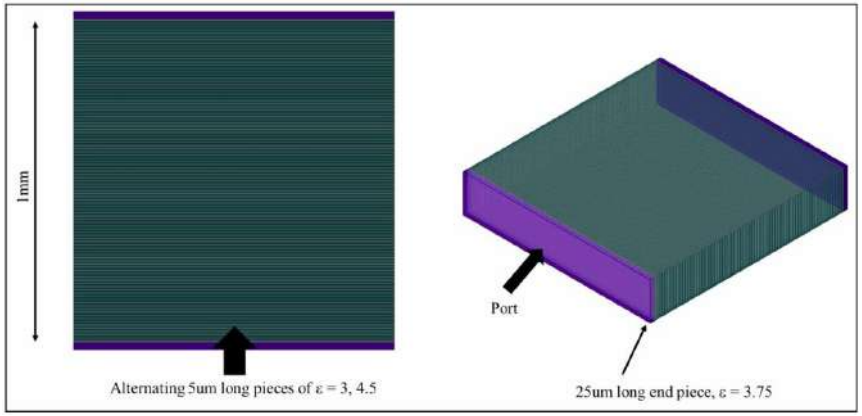


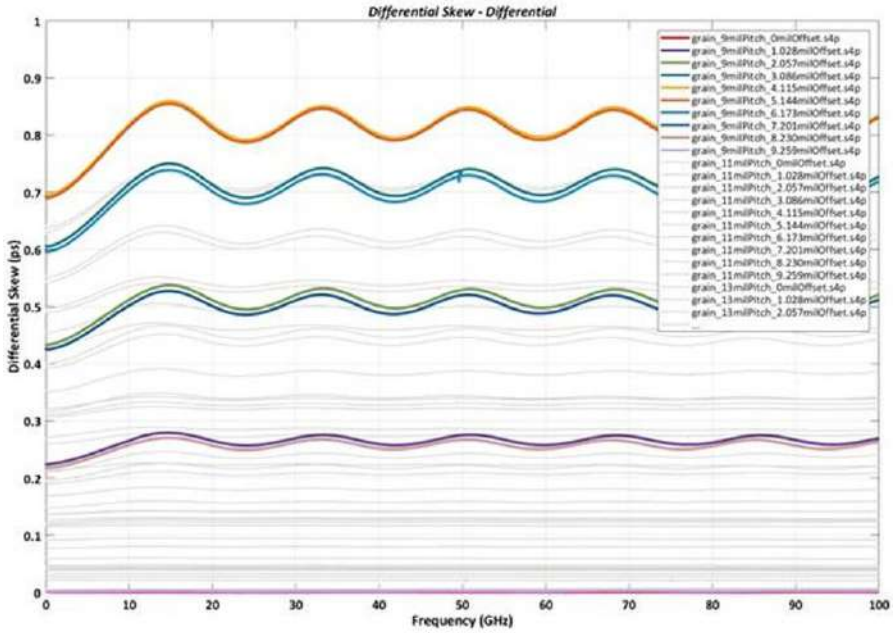


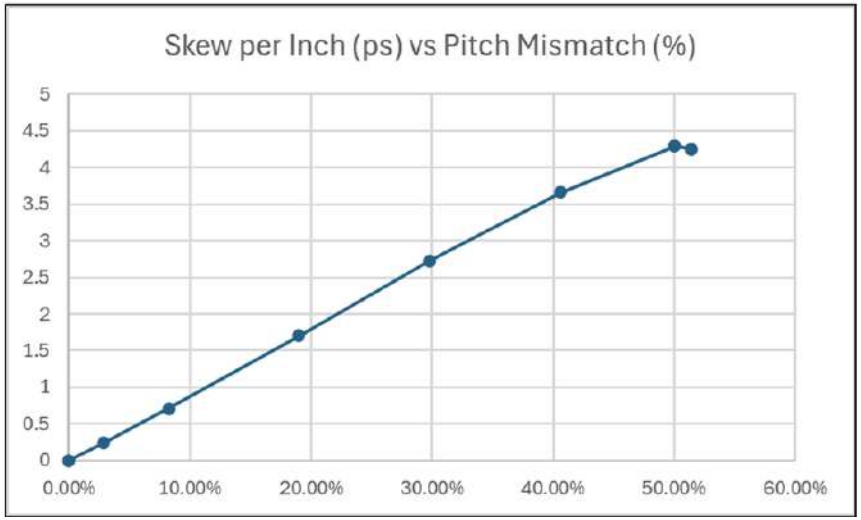
3-43 : Reduced Order Geometric Macro Model of PCB Fiberglass Spatial Variation for Skew and Impedance Prediction (2/2)

유리섬유 모델링(Elliptical Fiber Bundle + Waveguide 기반

- 각 섬유 다발을 타원형으로 모델링하여 유효 유전율 도출
- 두 가지 방향으로 계산 : 횡방향(유전율 평균 모델), 종방향(위상 지연 평균)
- Skew와 Pitch Mismatch 관계를 통해 worst-case 예측 가능







3-44 : How Interconnects Work: Crosstalk Anatomy and Quantification (1/5)

크로스톡(Crosstalk)

- Signal degradation의 원인
  - 유전체 및 도체의 흡수 및 분산 손실
  - 임피던스 불일치, 패키지 불연속성에 따른 반사손실
  - 크로스톡

Crosstalk Types

- **Local coupling:**
  - Coupling in closely routed signal traces – the most common source of crosstalk
  - Local coupling between viaholes and between viaholes and traces due to proximity
  - Local couplings of traces through cutouts in reference planes
  - Common to differential mode interference and crosstalk due to modal transformations in differential pairs (bends, asymmetry in routing, fiber weave effect,…)
- **Distant coupling and multipath propagation:**
  - Through parallel planes (PDNs)
  - Through split-planes (slots)
  - Through surface dielectric layers (surface and leaky waves)
  - Through PCB enclosure (box resonances)

3-44 : How Interconnects Work: Crosstalk Anatomy and Quantification (2/5)

Crosstalk 정량화 방법

Power Sum XTalk (PSXT)

- Preliminary evaluation of xtalk can be done with **Power Sum Crosstalk (PSXT)** (OIF-CEI and IEEE 802.3 standards):

$$PSXT_i = 10 \cdot log\left(\sum_{j\in\Omega_{XT}}|S_{i,j}|^2\right)\ [\text{dB}]$$ - total PSXT (MDXT)

$$PSNEXT_i = 10 \cdot log\left(\sum_{j\in\Omega_{NEXT}}|S_{i,j}|^2\right)\ [\text{dB}]$$ - Near-End PSXT (MDNEXT)

$$PSFEXT_i = 10 \cdot log\left(\sum_{j\in\Omega_{FEXT}}|S_{i,j}|^2\right)\ [\text{dB}]$$ - Far-End PSXT (MDFEXT)

Insertion Loss to Crosstalk Ratio (ICR)

- **Insertion loss to crosstalk ratio or ICR metric** can be used to evaluate and quantify the impact of the crosstalk:

$$ICR_{i,j} = IL_{i,j} - PSXT_i\ [\text{dB}]$$ ICR at port *i*

$$IL_{i,j} = 20 \cdot log\left(|S_{i,j}(f)|\right)\ [\text{dB}]$$ insertion loss at port *i* (negative)

$$PSXT_i = 10 \cdot log\left(\sum_{j\in\Omega_{XT}}|S_{i,j}|^2\right)\ [\text{dB}]$$ power sum crosstalk at port *i* (negative)

Integrated Crosstalk Noise (ICN)

- **Integrated crosstalk noise (ICN)** metric accounts for the signal spectrum and filtering properties of a transmitter and a receiver as follows

$$\sigma_{XTK} = \sqrt{\sigma_{NEXT}^2 + \sigma_{FEXT}^2}$$

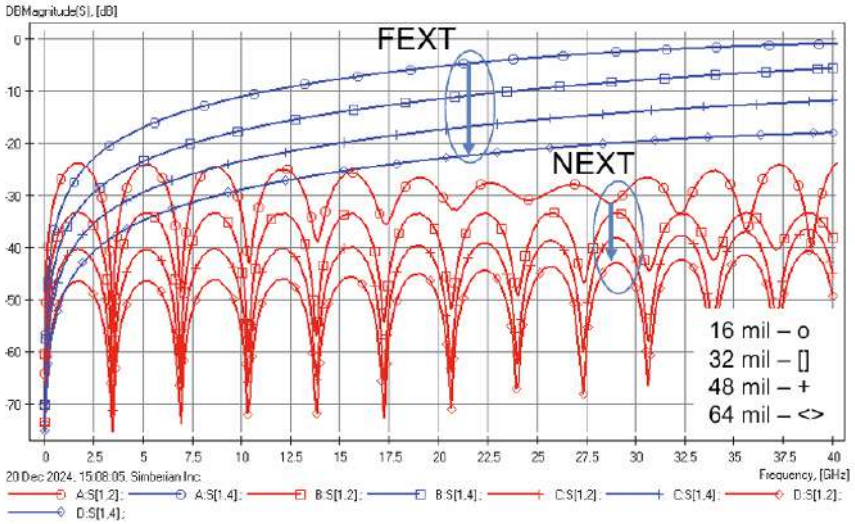
$$\sigma_{NEXT} = \sqrt{2 \cdot \Delta f \cdot \sum_k W_{nt}(f_k) \cdot NXT(f_k)}, \quad NXT(f_k) = \sum_{j\in\Omega_{NEXT}}|S_{i,j}|^2$$

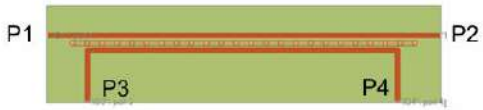
$$\sigma_{FEXT} = \sqrt{2 \cdot \Delta f \cdot \sum_k W_{ft}(f_k) \cdot FXT(f_k)}, \quad FXT(f_k) = \sum_{j\in\Omega_{FEXT}}|S_{i,j}|^2$$

3-44 : How Interconnects Work: Crosstalk Anatomy and Quantification (3/5)

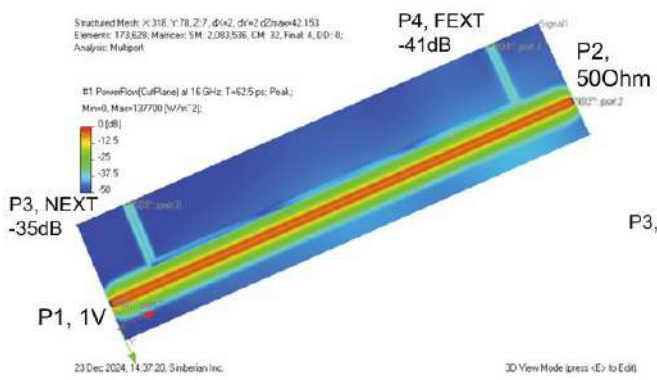
Crosstalk 저감 방법

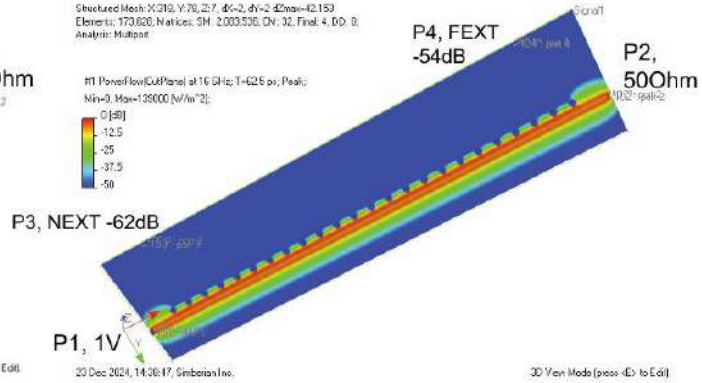
- Trace 간격 증가 및 커플링 길이 축소
- 가드 트레이스 및 via fence 삽입





Peak PFD at 16 GHz right below traces

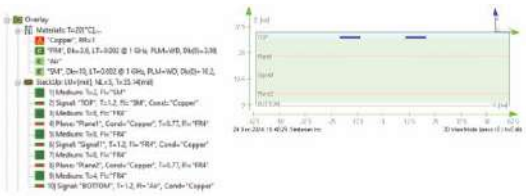


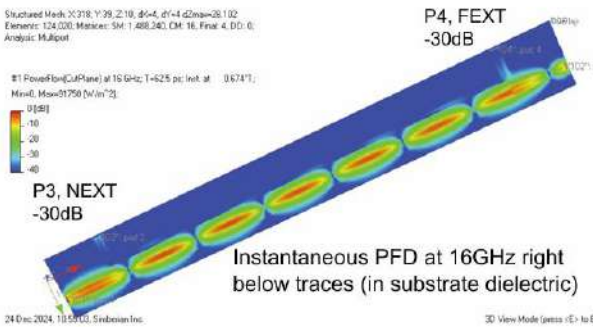


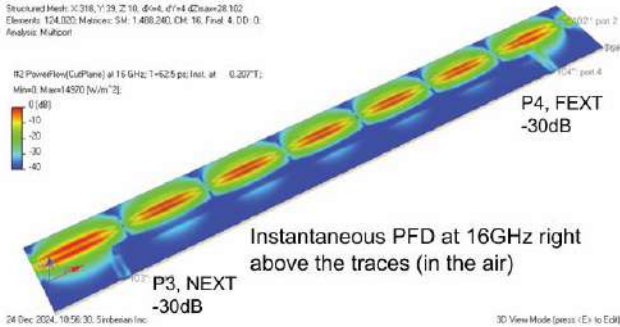
3-44 : How Interconnects Work: Crosstalk Anatomy and Quantification (4/5)

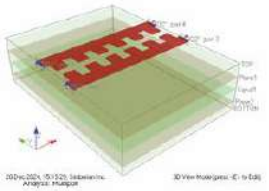
Crosstalk 저감 방법

- 크로스톡의 저감 기법
  - Coplanar 구조 및 탭 삽입 구조 사용
  - 오버레이 구조

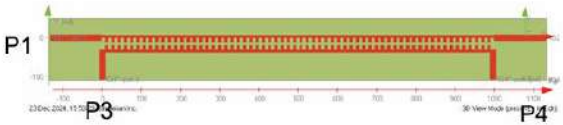


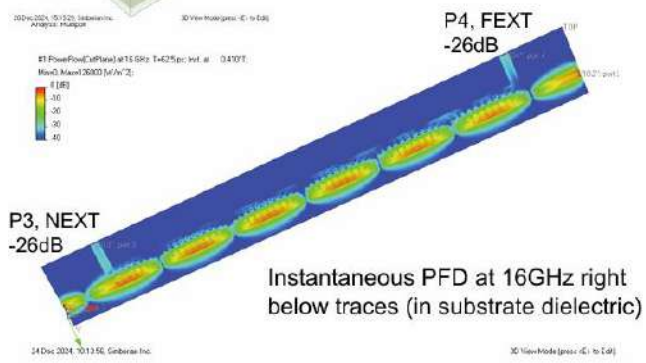


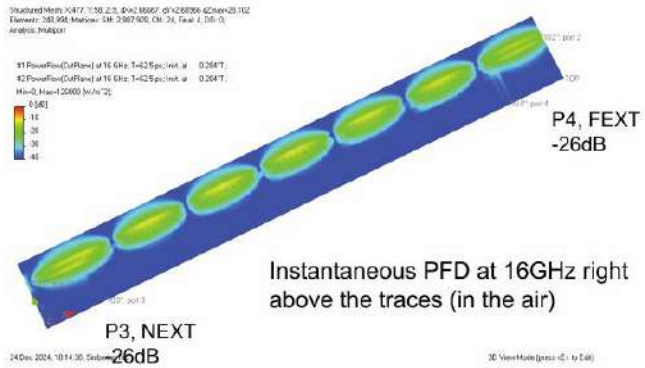




Tabbed: 8 mil traces,
24 mil apart, 8.5 by
7.5 mil tabs (40 mil
total width)







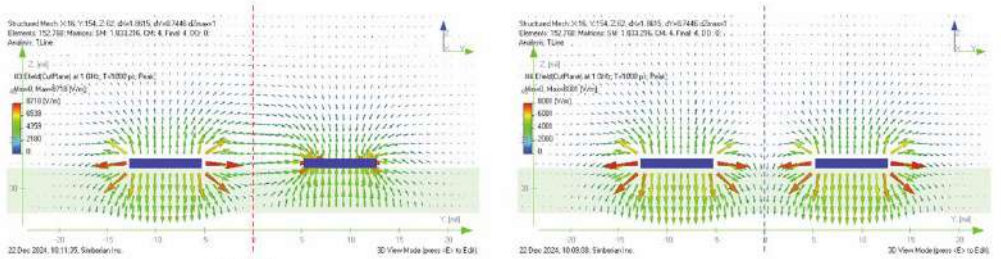
3-44 : How Interconnects Work: Crosstalk Anatomy and Quantification (5/5)

Crosstalk 저감 방법

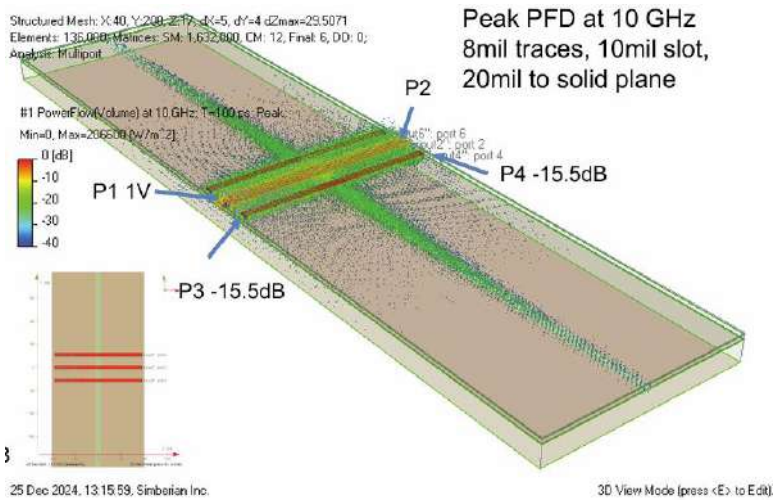
- 차동 신호 사용 및 대칭성 유지로 even/odd mode
- 슬롯, 절개면 회피

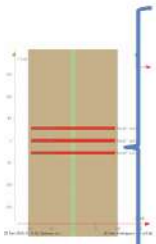
Odd Mode $\left(\frac{+1}{\sqrt{2}} \quad \frac{-1}{\sqrt{2}}\right)$

Even Mode $\left(\frac{+1}{\sqrt{2}} \quad \frac{+1}{\sqrt{2}}\right)$



PEC PMC





a) Increase trace separation? – Nope

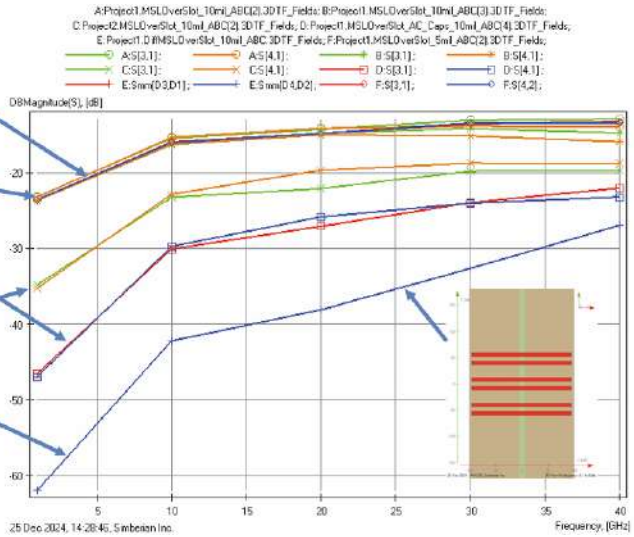
b) Make slot narrower? – Nope

c) "Stitch" planes with AC caps? – Maybe

d) Place solid plane closer? – Yes

e) Switch to differential lines? – Yes

f) Keep plane solid – The Best!



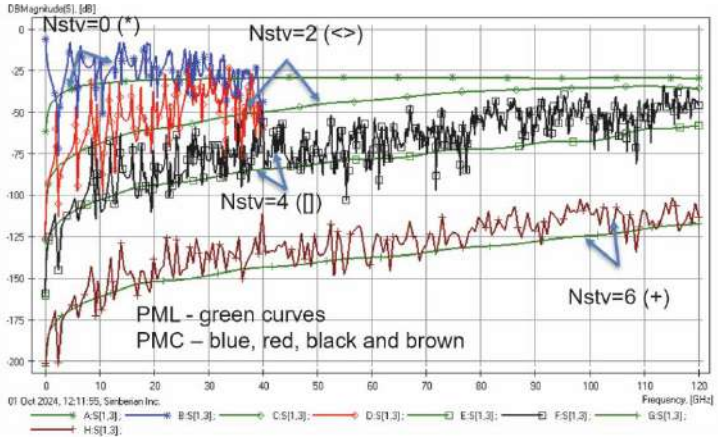
3-45 : Via Design for 112 Gbps and Beyond: Theory and Reality (1/2)

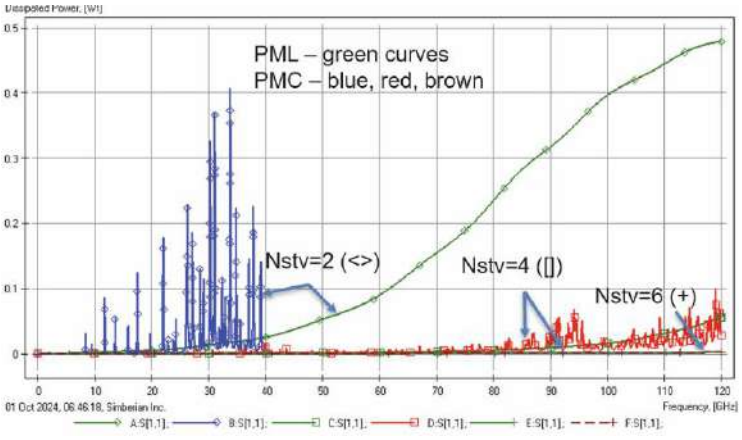
고속환경에서의 via 설계

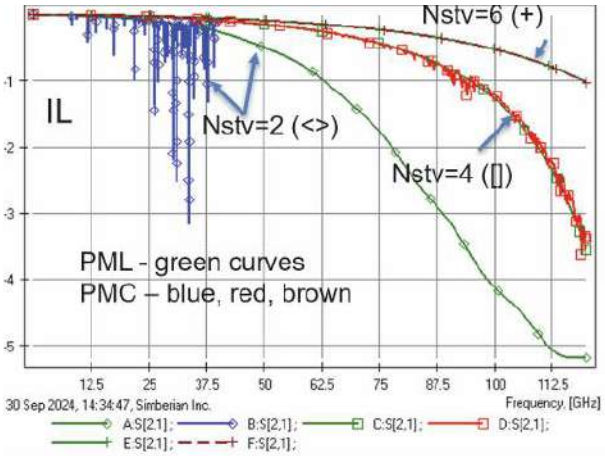
- 112~224Gbps 고속 통신에서는 via가 신호 반사 및 크로스톡의 주요 원인이 됨
- 제조사별 Stack up 변경 시 반사, 손실, 커플링이 증가함
- 기존 비아 설계는 실제 구현시 이상적인 모델과 차이 발생

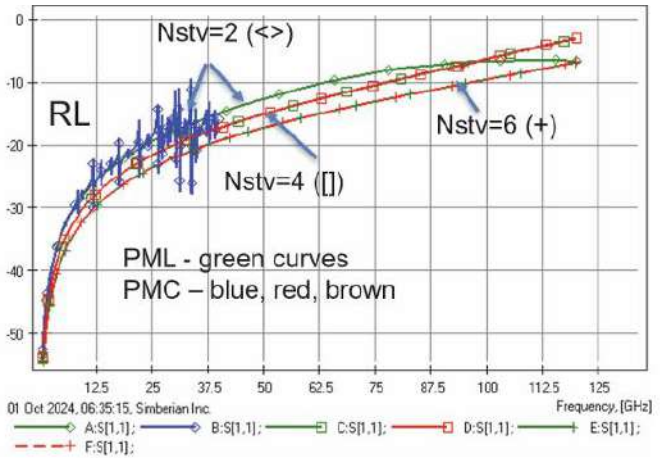
Via 설계 핵심

- Localization
- Dissipated Power를 활용한 누설 전력 평가 – Distant decoupling 방지
- Stitching via 배치
- 반사 손실과 삽입손실 분석을 통한 최적화





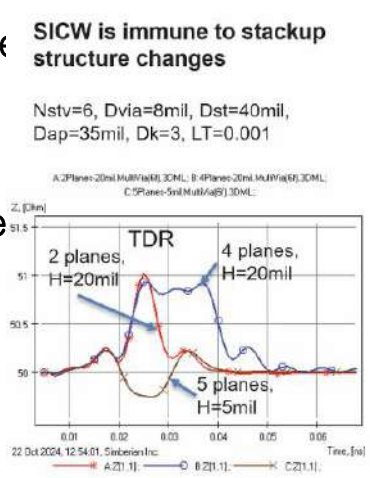


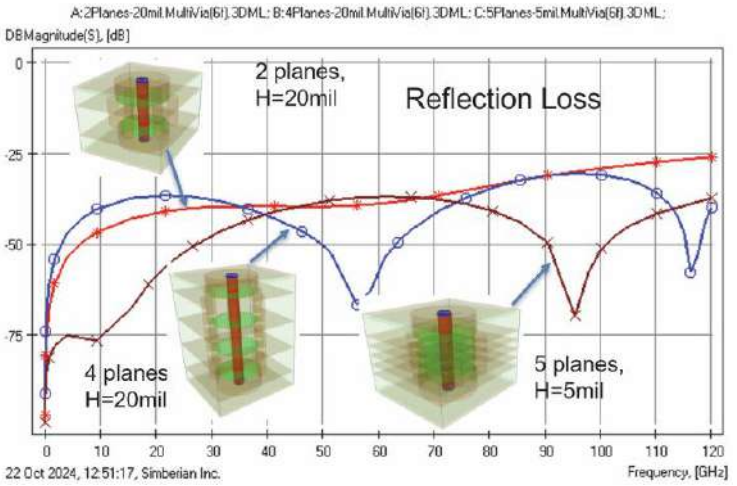


3-45 : Via Design for 112 Gbps and Beyond: Theory and Reality (2/2)

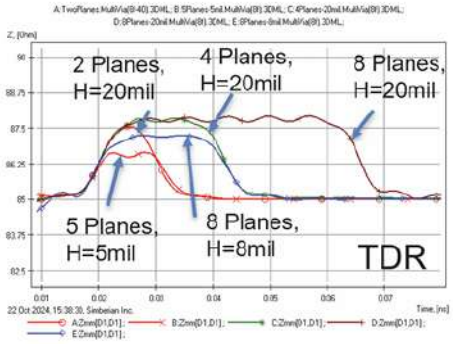
Waveguide 기반 설계 방식

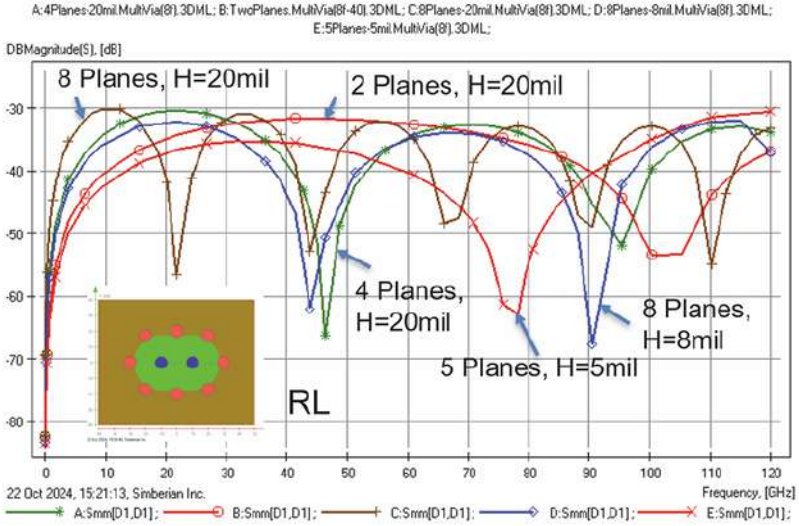
- SICW (Substrate Integrated Coaxial Waveguide
  -Antipad (외곽 원형 구조), 고주파에서 반사 최소화
  - 제조 공차 및 Stackup 변화에 강인함
- SITW (Substrate Integrated Twinax Waveguide
  -Differential 비아에 적용
  -고주파 공진 억제 및 noise에 강인함





Same XY-plane geometry: Dvia=8mil, Dvv=20mil, Hstv=40mil, Hap=35mil, Dk=3, LT=0.001
Simbeor 3DML, ABC





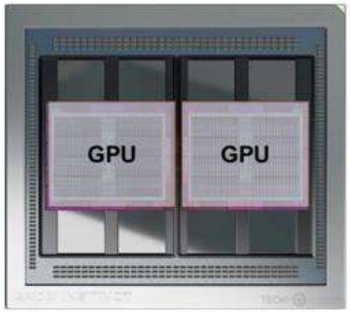
고주파에서도 성능변화가 작으며 Target impedance 85 ohm 인근에서도 안정적으로 유지

3. DesignCon 2025 자료 소개

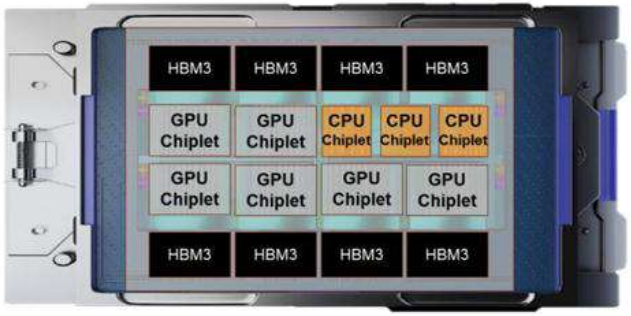
3-46 : Accelerating Chiplet Placement and Routing Optimization with Machine Learning (1/2)

칩렛(Chiplet) 배치 및 배선 최적화의 필요성

- 칩렛 수의 증가 및 HBM 통합 증가는 배치와 배선의 복합성을 증가시킴
- UCIe 인터페이스에서 SI를 유지하면서 최적의 칩렛 배치를 찾아야함

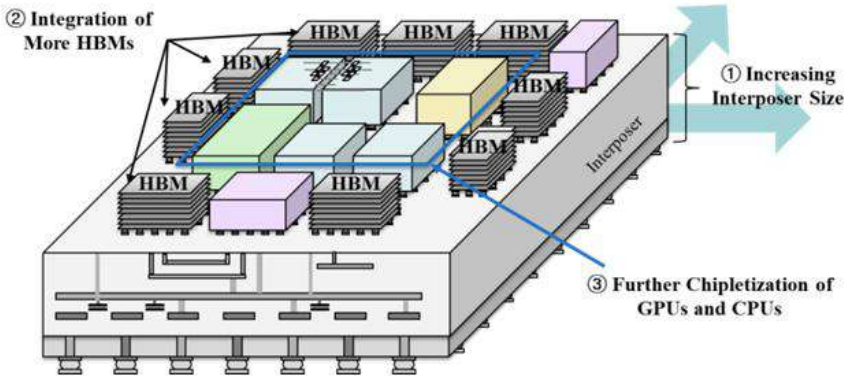


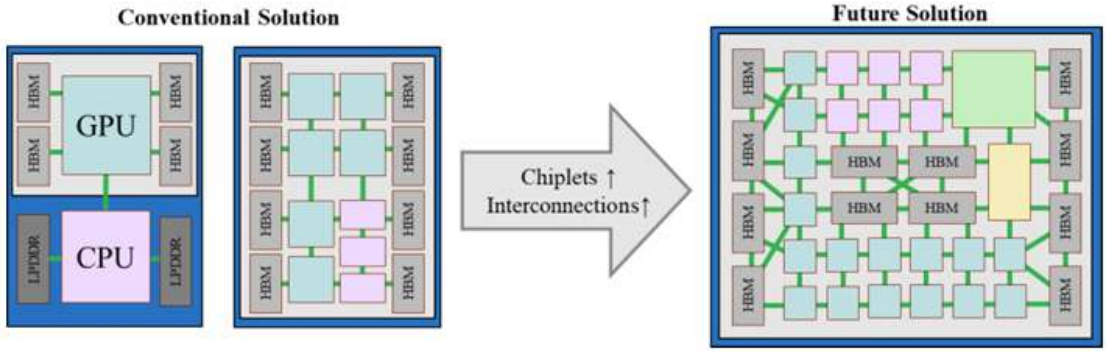
< AMD MI250 Architecture >



< Chiplet-based AMD MI300 Architecture >

Model		P100	V100	A100	H100	B100
Year		2016	2018	2020	2022	2024
Process		16 nm	12 nm	7 nm	4 nm	4nm(4NP)
# of SM		56 EA	80 EA	108 EA	144 EA	192 EA
Core type of SM		FP32, FP64	+ FP16 Tensor	+ FP32/64 Tensor + INT8/4 Tensor	+ FP8 Tensor + Tensor Memory Accelerator	+ FP4 Tensor + FP6 Tensor
Peak Performance	FP32	10.3 TFLOPS	15.7 TFLOPS	19.5 TFLOPS	73 TFLOPS	0.9 PFLOPS
	Tensor FP16	-	125 TFLOPS	312 TFLOPS	1080 TFLOPS	1.8 PFLOPS
	Tensor INT8	-	-	624 TOPS	2160 TOPS	3.5 POPS
	Tensor FP8	-	-	-	2160 TFLOPS	3.5 PFLOPS
	FP6					3.5 PFLOTS
	FP4					7 PFLOPS
L2 Cache		4 MB	6 MB	40 MB	60 MB	N/A
Memory	Capacity	16GB HBM2	32GB HBM2	80GB HBM2E	96GB HBM3	192GB HBM3e
	Bandwidth	720 GB/s	900 GB/s	2039 GB/s	4110 GB/s	8000 GB/s
	# of HBM	4 EA	4 EA	6 EA	6 EA	8 EA
Max Power		300 W	300 W	400 W	700 W	700 W



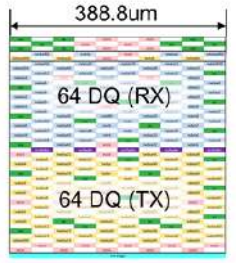


3. DesignCon 2025 자료 소개

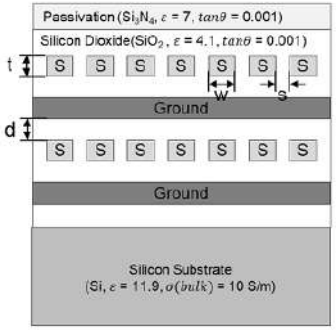
3-46 : Accelerating Chiplet Placement and Routing Optimization with Machine Learning (2/2)

ML 기반 최적화 기법 – heuristic 배치/배선 알고리즘

- Reward Function : 데이터 전송 속도 기반의 SI-aware 보상
- Heuristic Placement : Manhattan 거리 기반 위치 선정
- Routing Optimization : Datarate 우선 순위 고려



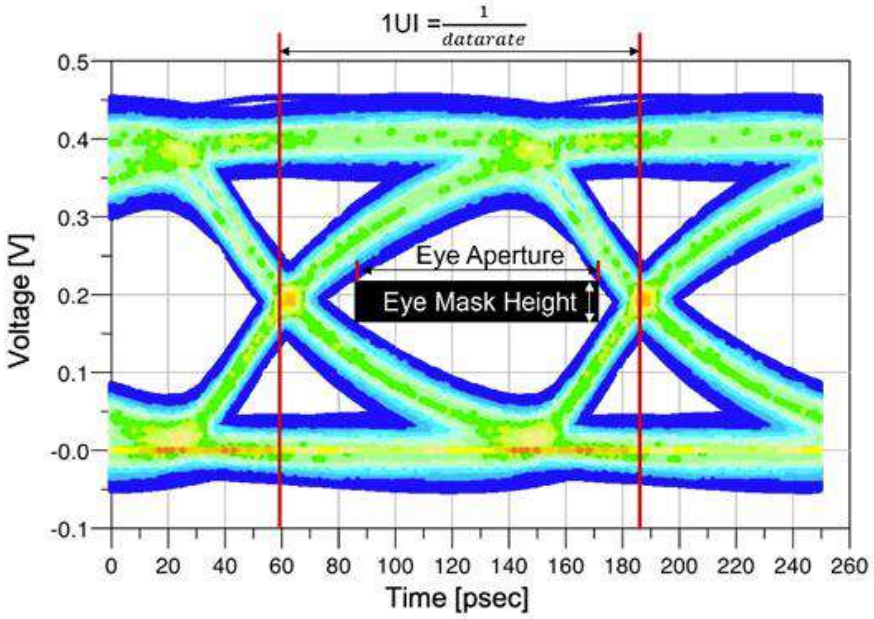
< UCIe Bumpmap >



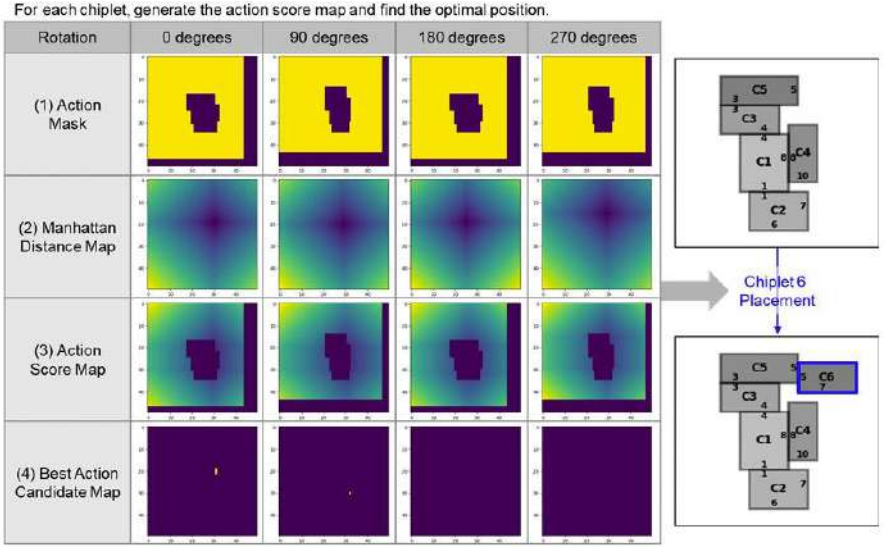
Parameter	Value
# of Metal Layers [EA]	4
# Wire Density [EA/mm]	400
Channel width (w) [um]	2 um
Channel space (s) [um]	2.86 um
Metal thickness (t) [um]	1.5
Dielectric thickness (d) [um]	1.5
Si Substrate thickness [um]	100

< UCIe Advanced Channel Model Stack-up >

[UCIe stacup 구조]



[Eye Aperture, Datarate]



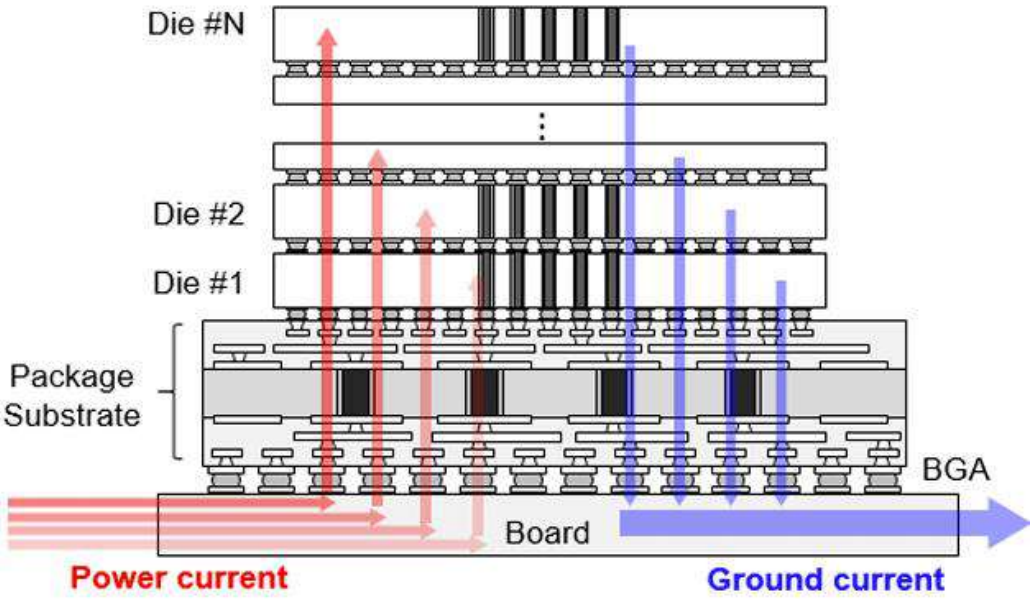
[Manhattan 거리 기반 위치 선택도]

3-47 : Deep Reinforcement Learning Based Design Optimization of Power/Ground Ball Map in BGA Package in 3D ICs Considering Multiple Power Domain Environments (1/2)

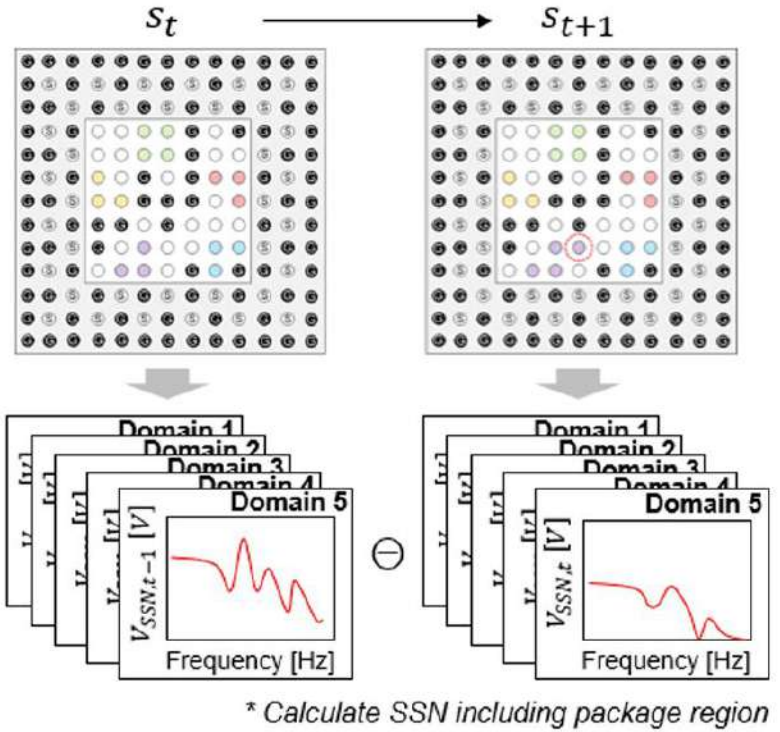
3D-IC 구조에서의 PI문제

- 3D-IC 구조에서의 칩 수직 적층으로 인해 PDN이 복잡해지고, 신호 간섭이 증가
- MPD(Multiple Power Domain)에서 서로 다른 전압 영역이 혼재함으로써 PDN 공진, switching noise 발생
- 전력 및 그라운드 볼 배치의 불균형으로 SSN(Simultaneous Switching Noise) 발생

  -> SSN 중심의 설계 자동화 필요



[3D-IC MPD 구조 및 MPD 환경]

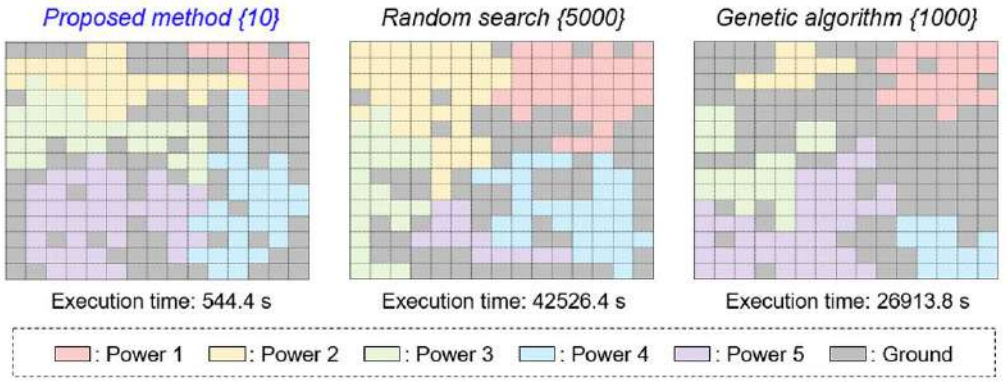


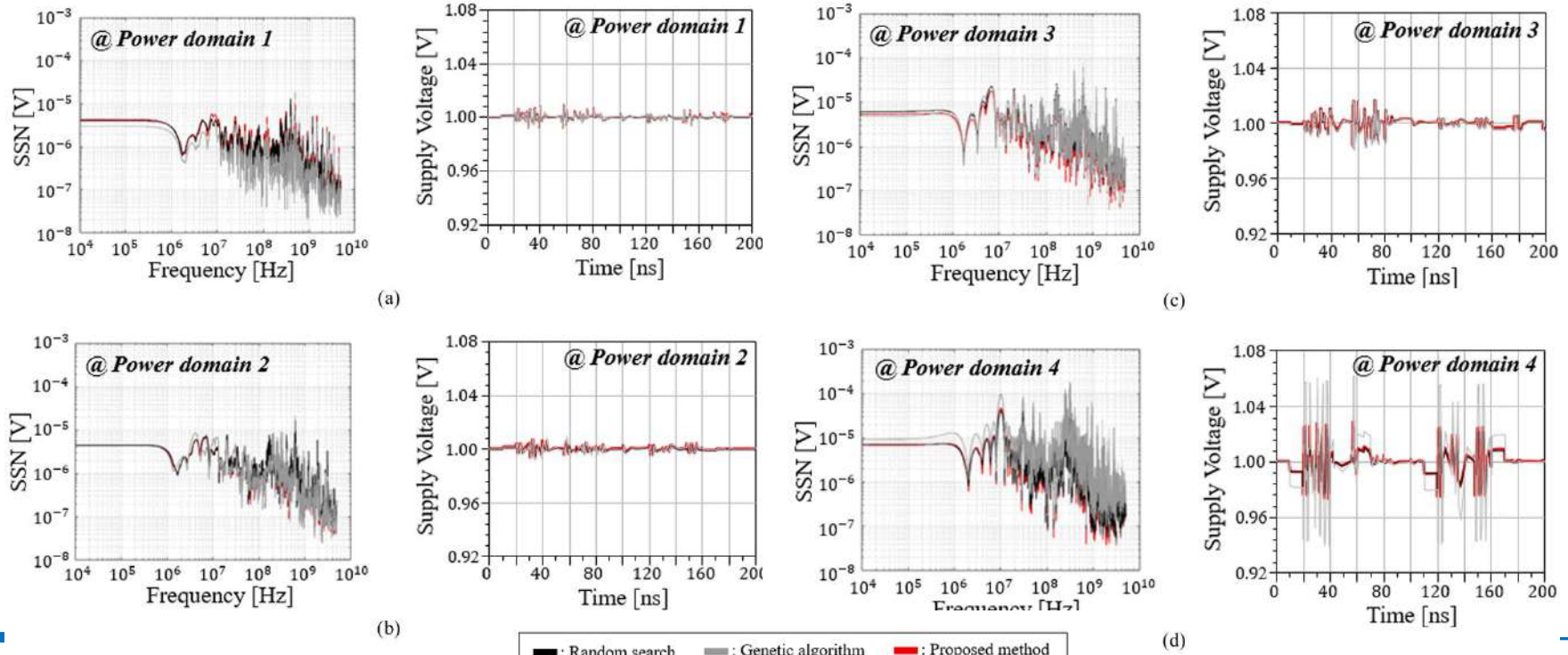
[SSN 계산 방식 및 보상 함수 정의]

3-47 : Deep Reinforcement Learning Based Design Optimization of Power/Ground Ball Map in BGA Package in 3D ICs Considering Multiple Power Domain Environments (2/2)

DRL 기반 최적화

- Power/Ground 볼의 공간 분포 학습을 통해 전력 네트워크 경로 최적화
- SSN 저감을 통항 SI 향상



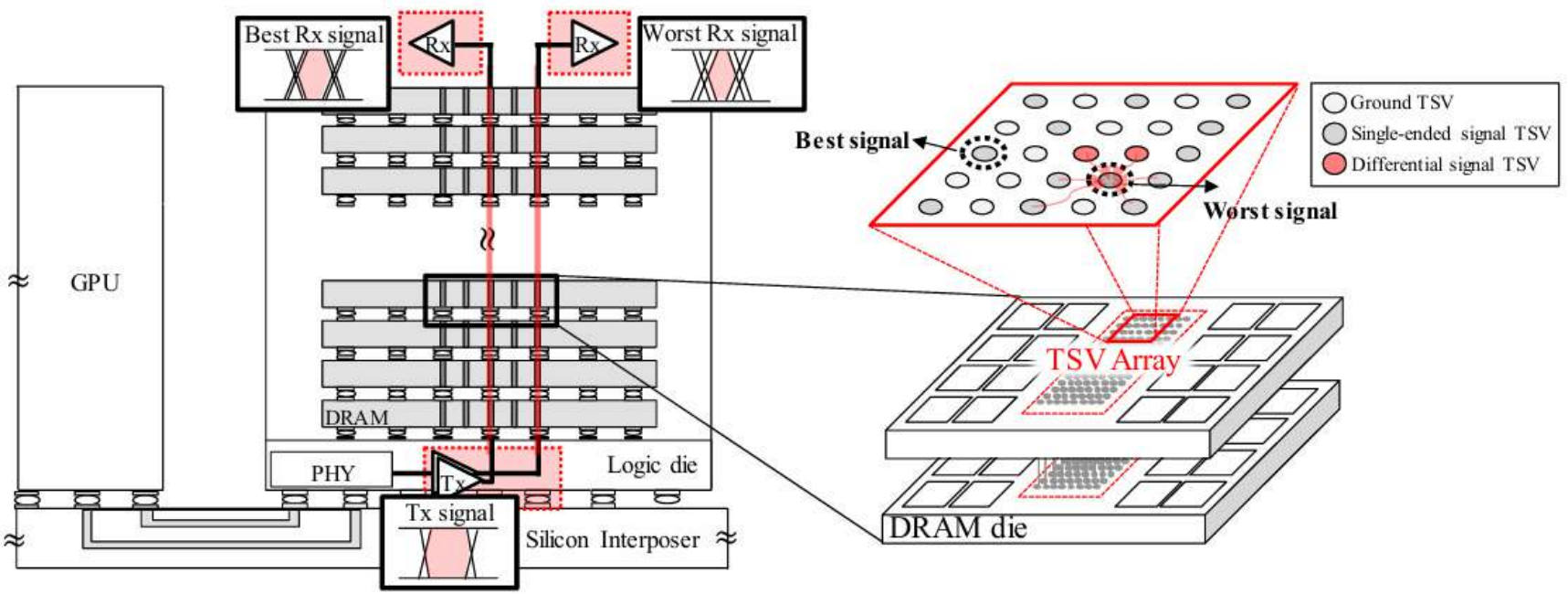


Core 수 증가에도 PI 안정화가 유지됨

3-48 : Flow Model Can Give You Optimal and Diverse Design Guidance for TSV Array Placement in HBM (1/2)

HBM의 TSV 배열 배치를 위한 최적화

- TSV (Through Silicon Vias)는 칩을 수직으로 연결하기 때문에 TSV 간 SI 문제 발생
- 차동 신호와 단일 신호 TSV 간의 간섭이 신호 왜곡 및 Eye Opening 축소로 이어짐
- SI 최적화를 위한 설계 조건
  - TSV 간 최소 간격 확보
  - Ground TSV의 위치와 밀도 조정
  - Return path 최적화



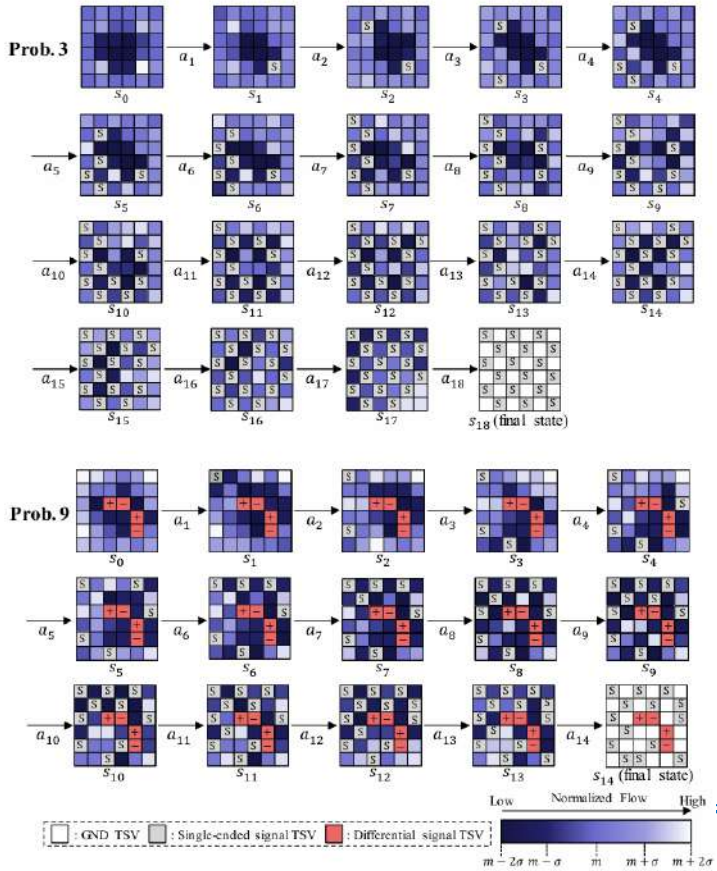
[Signal degradation in different TSV Placement]

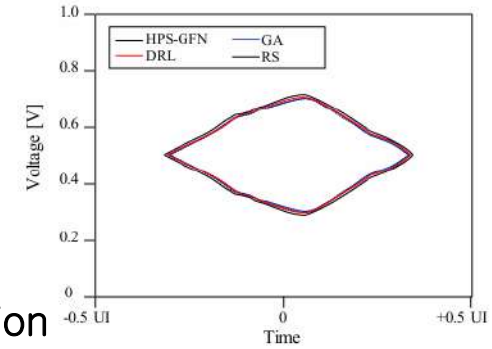
3-48 : Flow Model Can Give You Optimal and Diverse Design Guidance for TSV Array Placement in HBM (2/2)

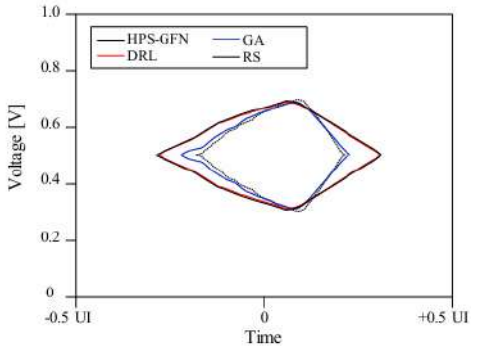
Challenges in TSV Placement Optimization

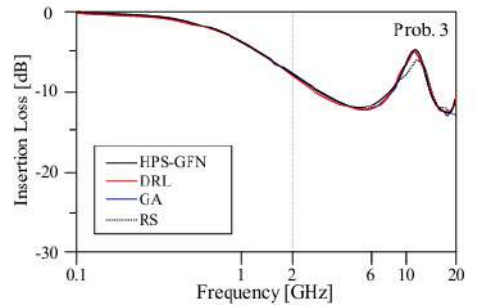
- 기존 AI 기반 최적화 방법 한계
  - Reinforcement Learning (RL)
  - Genetic Algorithms (GA)
  - Random Search (RS)

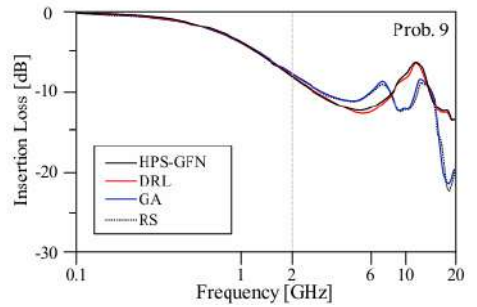
HPS-GFN : Generative Flow Network for TSV Optimization

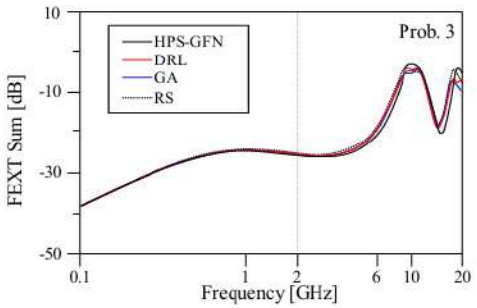


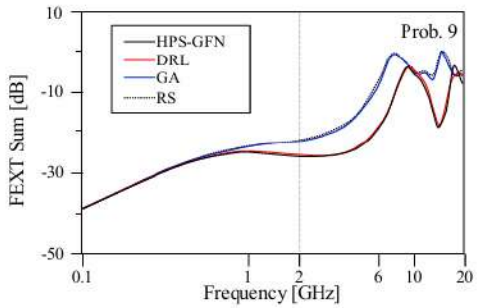












3-49 : Foundational Model Approach for SI/PI Analysis Using Large Language Model Techniques (1/2)

Transformer 기반 SI/PI 해석 모델

- 입력 : 채널의 입출력 파형 / 출력 : 해당 채널의 Impulse Response
- Impulse Response 예측 : Eye Diagram, Ber 분석 기반 확보
- Latent space 분석 : Via 구조를 구분함으로써 물리 구조 반영
- 고속 추론 : EDA 자동화 가능

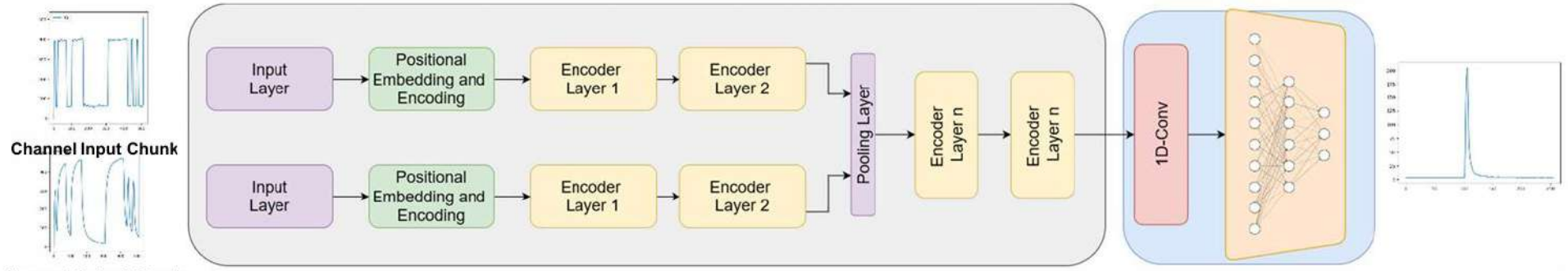
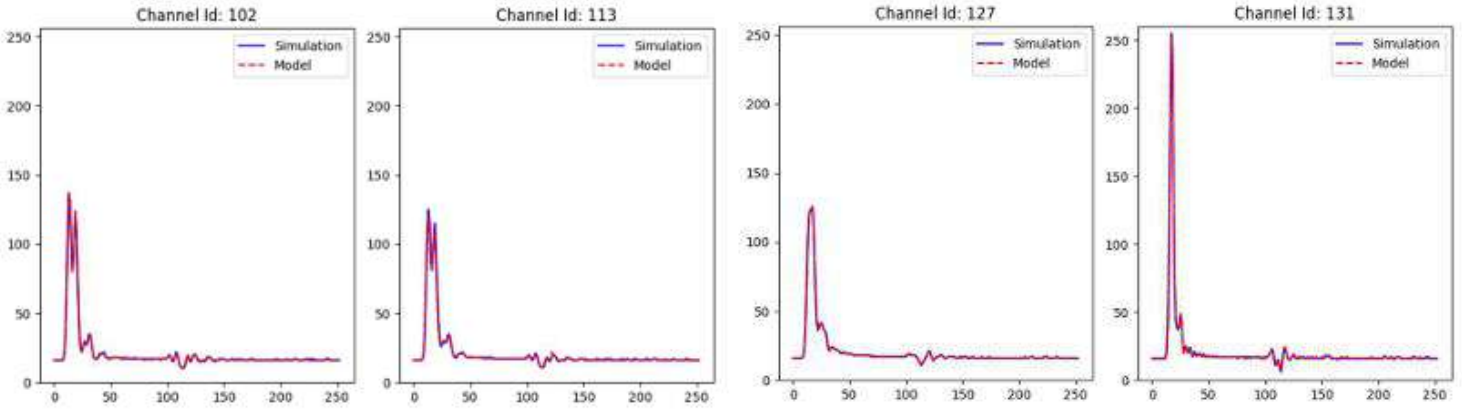


Fig. Base model architecture with a transformer encoder stack (in gray) and a generation head (in blue).

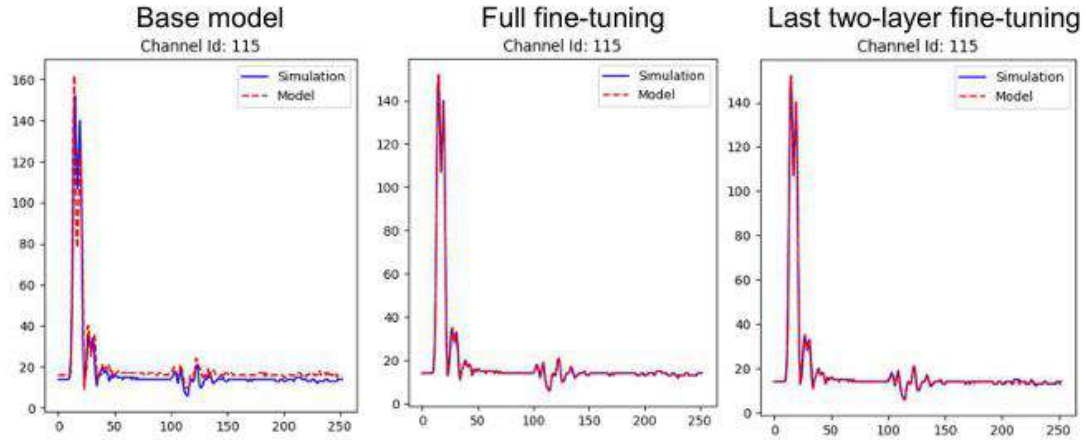


예측과 실측의 Impulse Response 비교

3-49 : Foundational Model Approach for SI/PI Analysis Using Large Language Model Techniques (2/2)

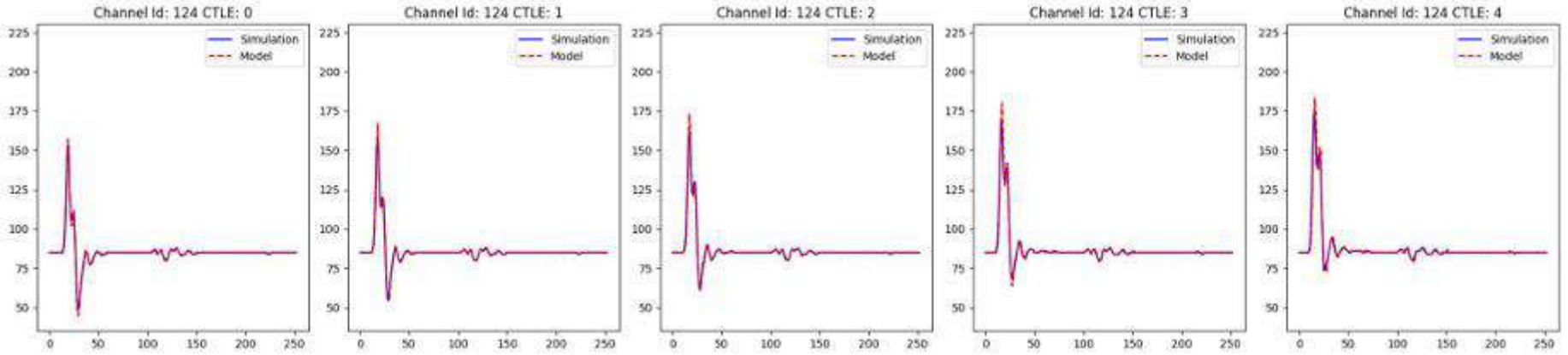
Fine-tuning & Transfer Learning

- Via 구조 변경, 속도 증가, PAM4 변조, CTLE equalization 조건 변화에도 fine tuning만으로 높은 정확도 확보



Via 변경 대응 결과

CTLE 환경에 대한
Transfer Learning 성능



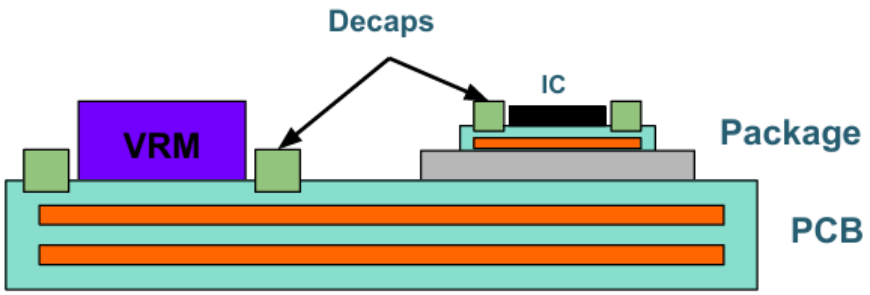
3-50 : Impedance Profile Prediction and Classification for PCB -based PDN Decoupling Using Autoencoders

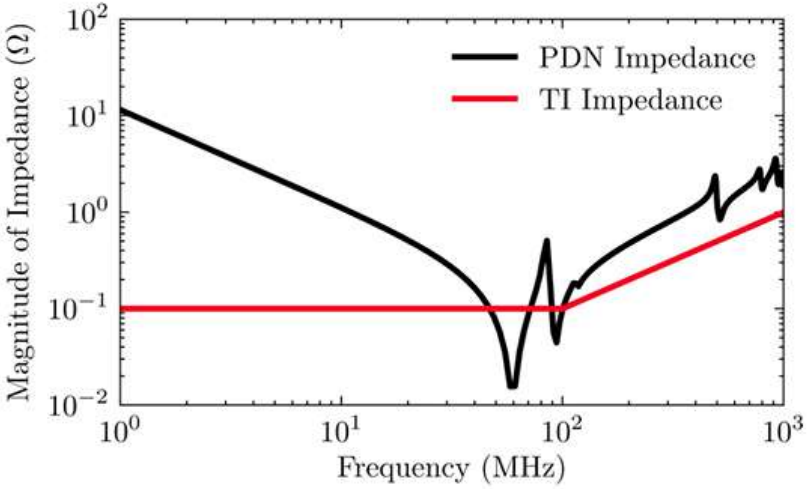
전력 분배 네트워크(PDN) 설계의 중요성

- 고속 IC에서의 PDN은 SI/PI를 유지하는 핵심 요소
- 낮은 임피던스 설계를 위한 전압강하와 노이즈 문제를 최소화
- EM 시뮬레이션의 소요 시간(시뮬레이션 속도가 느림)

PDN의 설계의 문제점

- 높은 연산 비용
  - PDN 임피던스를 예측하기 위해 복잡한 FEM 모델 필요
- 데이터 재사용 및 최적화 부족
  - 각각의 새로운 PCB 디자인에 대해 새로운 EM 시뮬레이션 필요
- 디커플링 커패시터의 배치의 어려움
  - 주파수별 임피던스 특성을 반영한 최적화 필요

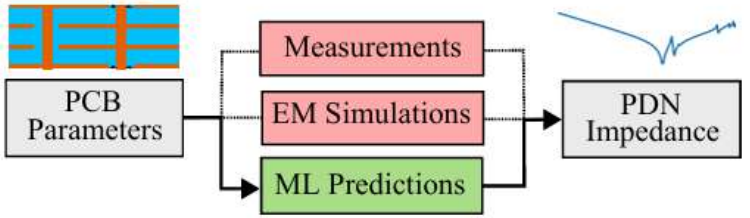




3-50 : Impedance Profile Prediction and Classification for PCB -based PDN Decoupling Using Autoencoders

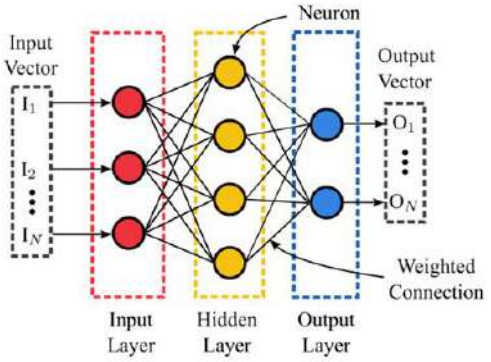
머신 러닝(ML)을 활용한 PDN 설계

- 인공지능 기반으로 PDN 설계 가속화
- 인공 신경망(ANN), 자동 인코더(AE) 활용
  - ANN과 AEs는 은 PCB 파라미터를 기반으로 PDN 임피던스 예측
  - AEs는 latent space를 추출하여 설계 패턴 학습

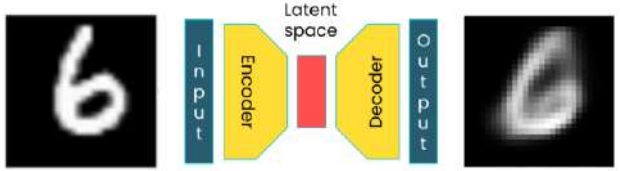


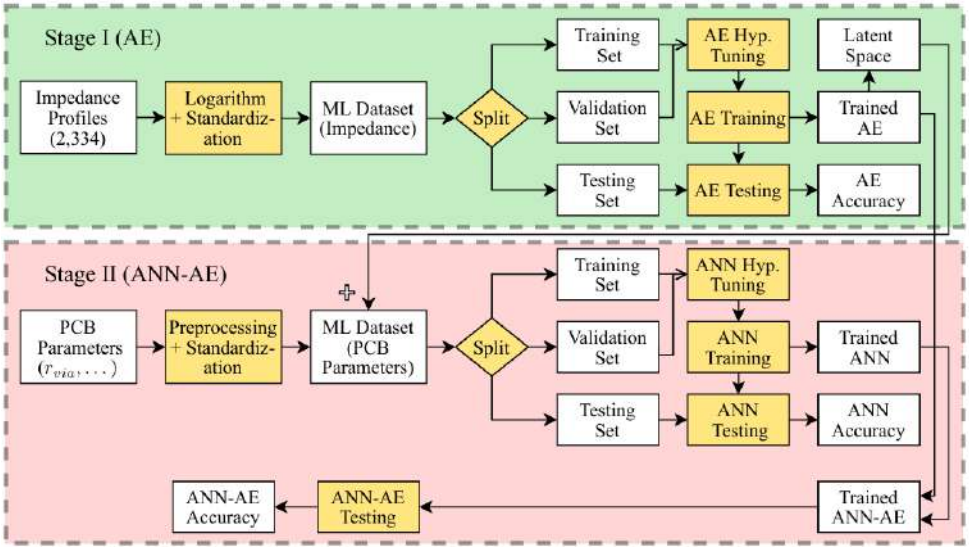
Self-Impedance Prediction

Artificial Neural Networks (ANNs)



Autoencoders (AEs)





PDN Design process Flow chart

3-51 : A Field-based Perspective on High-speed PCB Design

전자기장(EM Fields) 기반의 PCB 설계

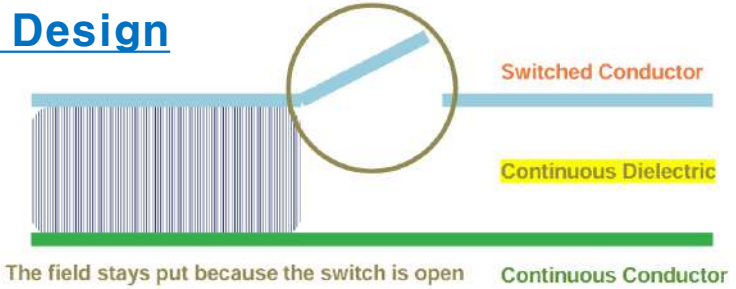
- 기존 회로 설계에서는 전하의 이동에 초점을 맞췄으나, 실제 에너지는 전자기장이 운반
- PCB 설계 시 배선이 아닌 공간을 설계하는 것이 중요

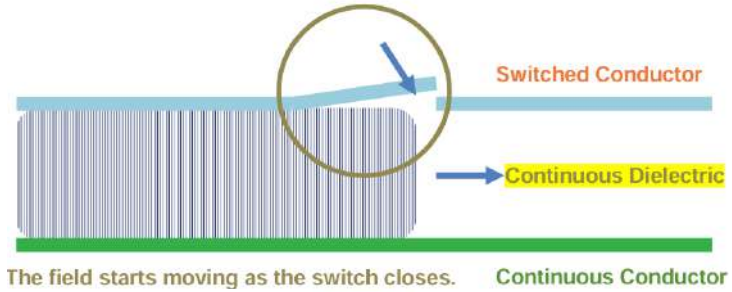
The Rules of Triplets

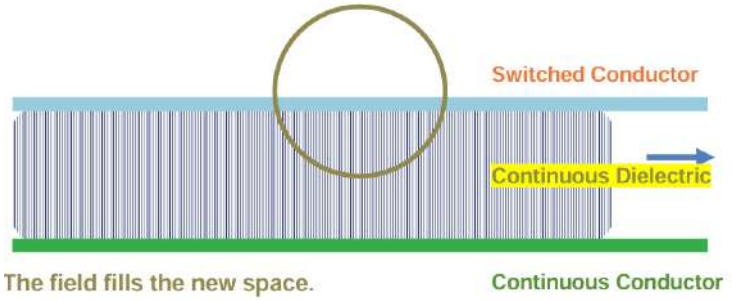
You only need 3 components to use to contain EM energy
- Conductor
- Spaces (dielectric)
- Conductor

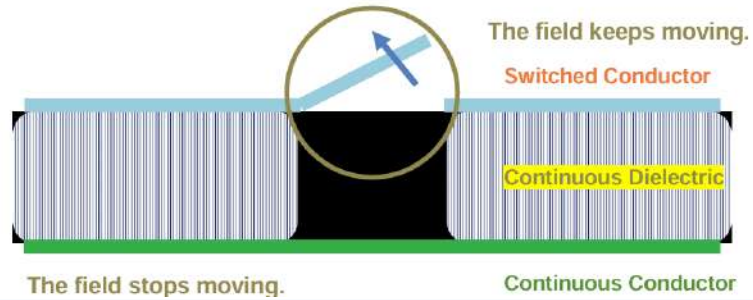
You only get 3 components to use to build electronic systems
- Conductors
- Spaces (dielectric)
- Switches

You can only do 3 things with Electromagnetic Field Energy
- Store it
- Move it
- Convert it to kinetic energy









3-51 : A Field-based Perspective on High-speed PCB Design

설계 최적화를 위한 전력 및 신호 관리

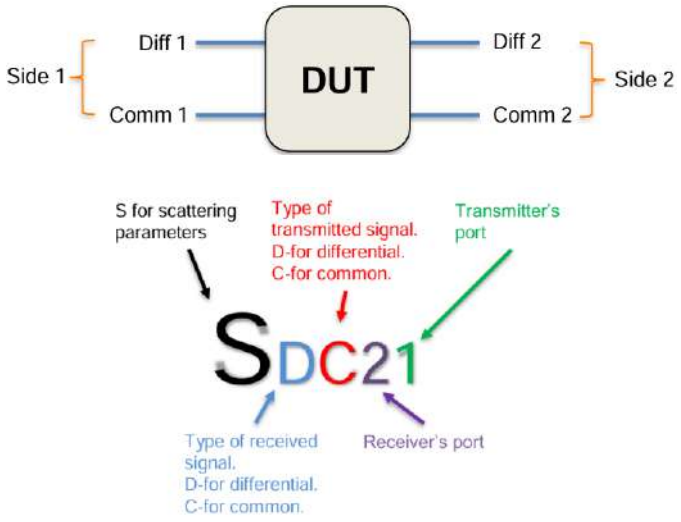
- 신호 무결성 (SI)
  - 신호 경로는 한 개의 유전체를 두고 리턴 경로와 인접해야 함
  - 신호 속도가 증가할수록 PCB 내의 구조물이 안테나 역할을 하게 됨
- 전력 무결성 (PI)
  - PDN 설계 시, 전력 공급에서의 저항과 인덕턴스를 최소화
  - 스위칭 속도가 증가할수록, 에너지원(커패시터)이 신호와 가까워야 함
- 열 관리
  - 발열 문제 해결을 위해 열 전도율이 높은 재료 사용
  - 전력 소비 최소화 및 냉각 시스템과 방열구조 최적화

3-52 : Novel Method for Improving Differential to Common Signal Integrity Results for 112GB/224GB

차동 신호(Differential signaling) 및 모드 변환(Mode conversion)

- 차동 신호는 고속 데이터 전송(112G/224G)에서 신호간섭(EMI) 최소화 BER 감소를 위해 필수
- 모드 변환은 길이 불일치, 임피던스 불균형, PCB 유리섬유 효과, 비대칭적인 VIA 및 커넥터 설계 문제로 발생

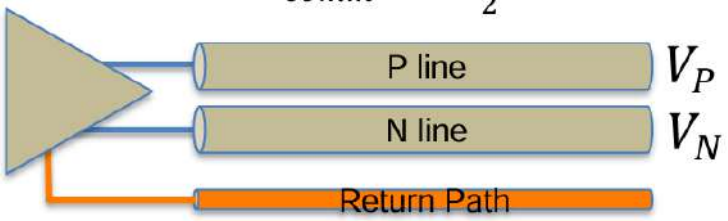
Mixed Mode S-Parameter 및 Differential to Common Mode conversion (D2C) :



Diff In - Diff Out		Comm In - Diff Out	
SDD11	SDD12	SDC11	SDC12
SDD21	SDD22	SDC21	SDC22
Diff In - Comm Out		Comm In -Comm out	
SCD11	SCD12	SCC11	SCC12
SCD21	SCD22	SCC21	SCC21

$$V_{diff} = V_P - V_N$$

$$V_{comm} = \frac{V_P + V_N}{2}$$

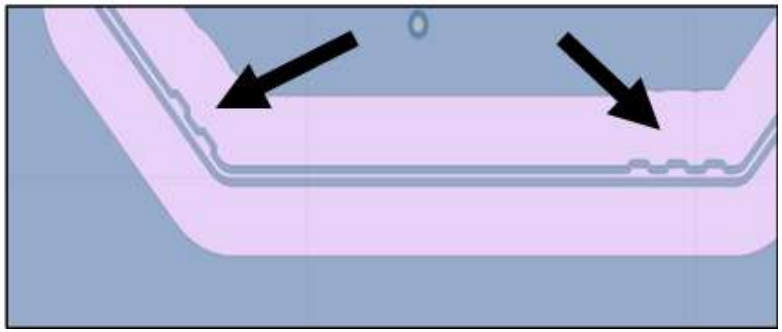


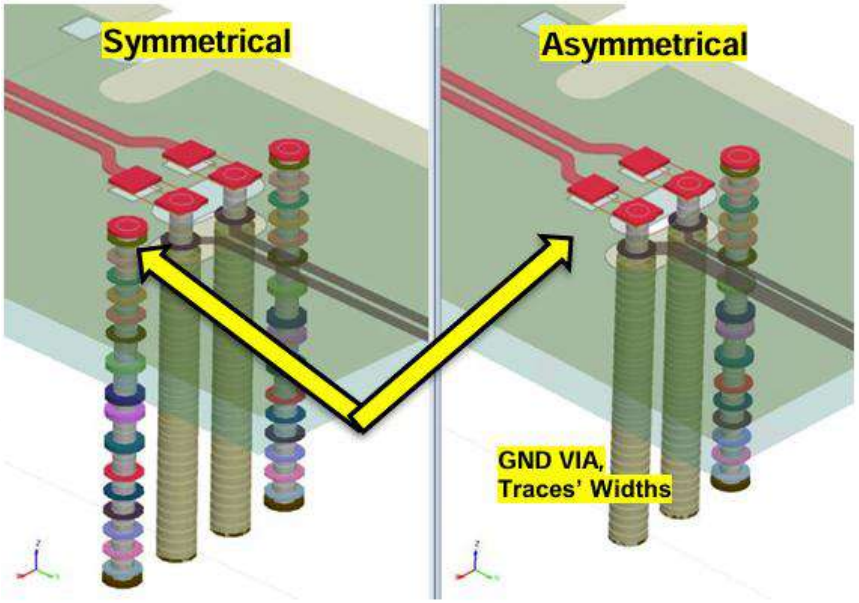
- Any signal on a differential pair has a differential component and a common component.
- The differential component is the voltage difference between the lines.
- The common component is the voltage average of the lines (bias voltage).
- Ideally, for differential signaling, the common component should remain constant.

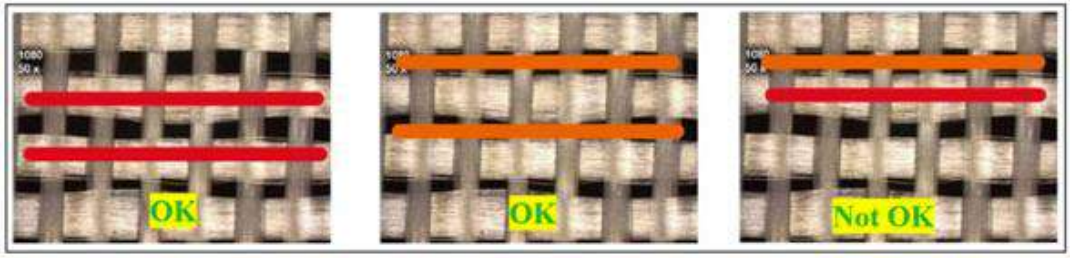
3-52 : Novel Method for Improving Differential to Common Signal Integrity Results for 112GB/224GB

SI 및 Mode Conversion 최소화를 위한 가이드 라인

- Physical length matching
  - Adding length matching segment to compensate length mismatches
  - Many application notes
- Electrical length matching
- Symmetrical design
  - Keep structures symmetrical for both lines; Traces' widths, VIAs, reference planes, voids etc.
- Fiberglass weave:
  - Set pair's geometry to align with the weave's grid
  - PCB rotation (10-15 degrees)







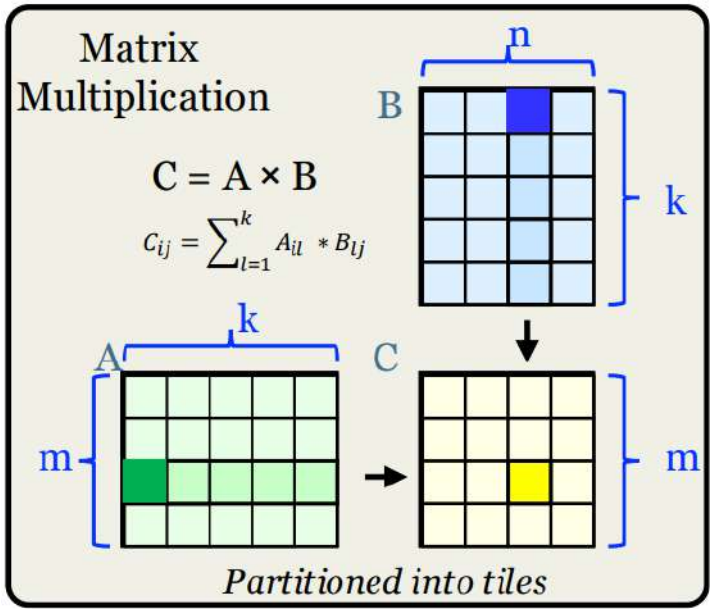
3-53 : Energy Efficient Interfaces for the Next Generation of AI Compute

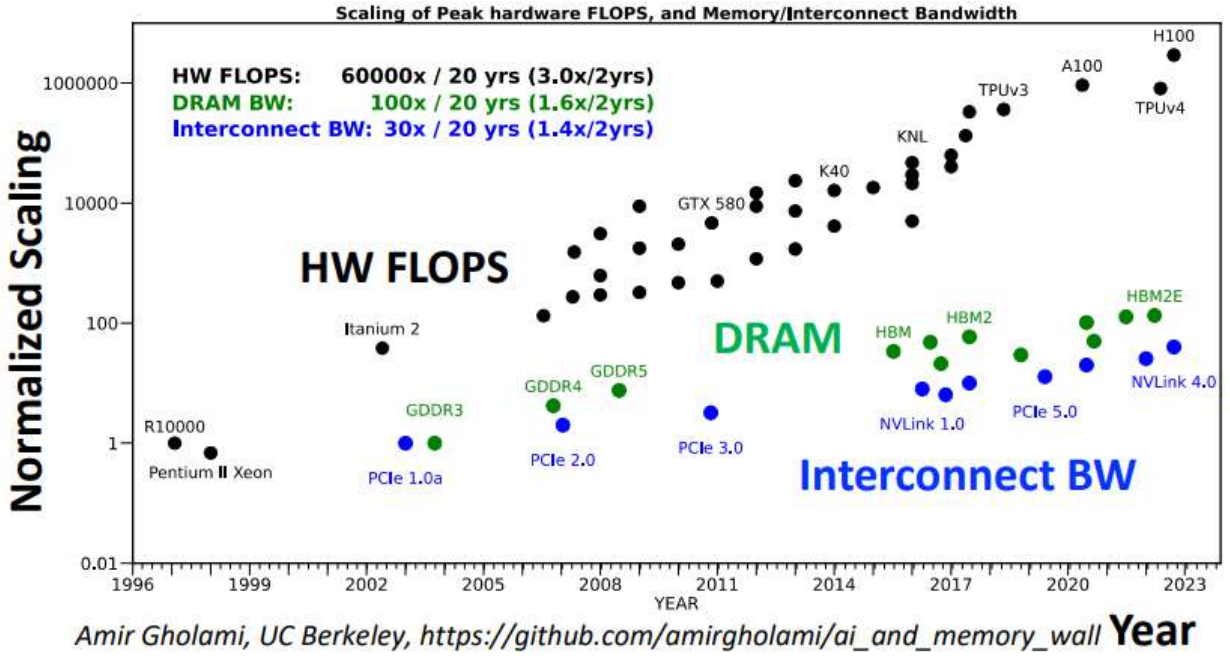
AI 연산

- 대규모 행렬 연산(Matrix Multiplication)을 기반으로 수행됨
- 대형 AI 모델은 연산을 작은 블록(Tile)로 나눔

AI 연산의 효율성 향상 방안

- AI compute 성능 향상 방법
  - Bandwidth & Connectivity 개선 -> 고속 DRAM(HBM2, HBM3) 사용
  - Latency 감소 -> PCIE 5.0, NVLink 4.0
  - 에너지 효율성 향상 -> 타일 기반 연산 최적 분배

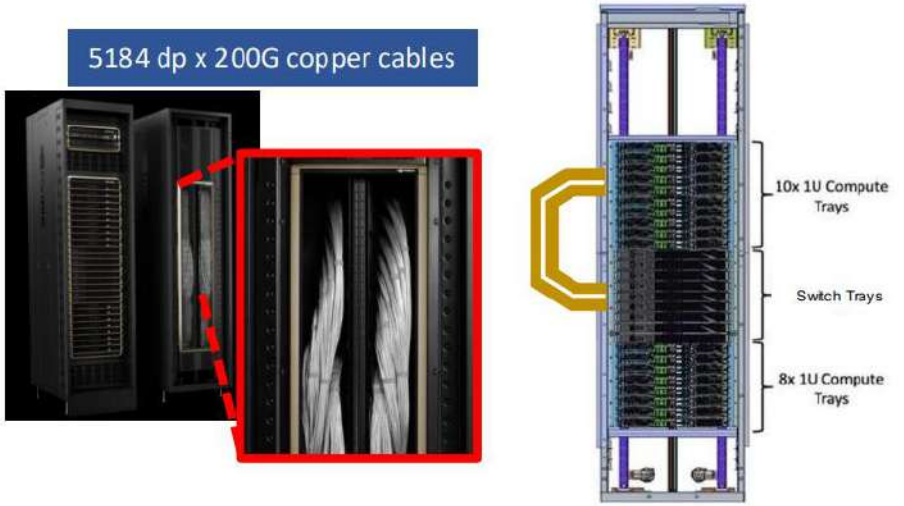




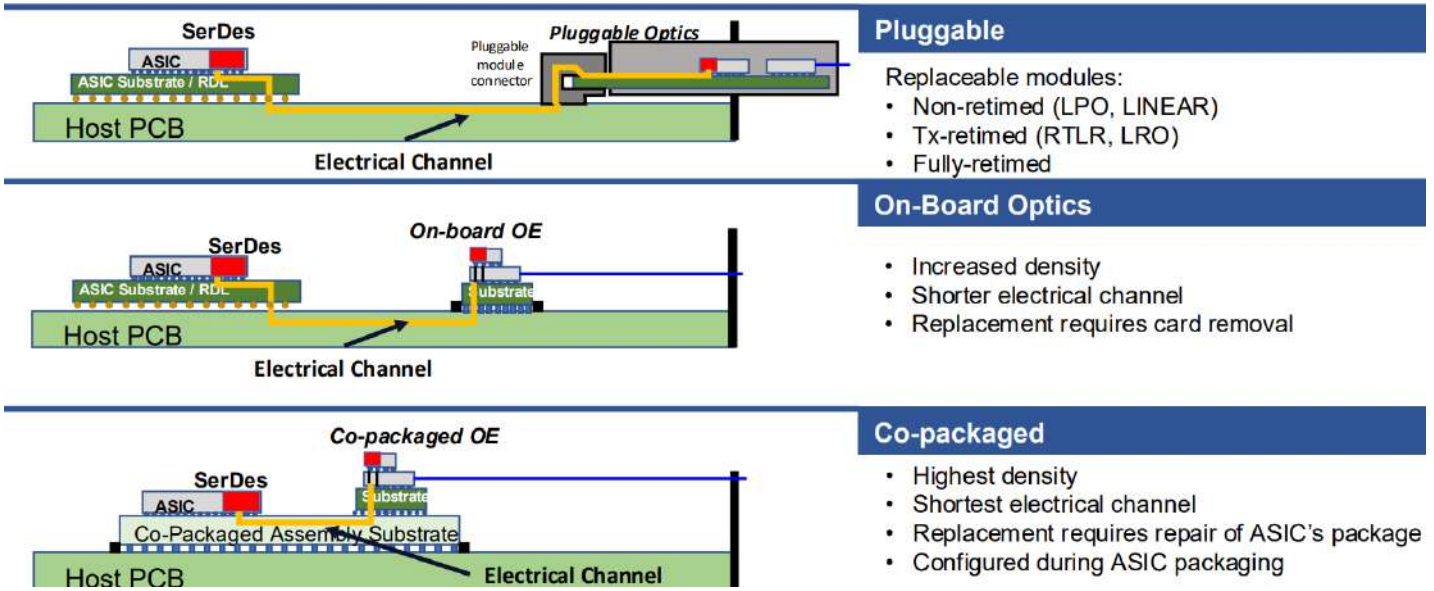
3-53 : Energy Efficient Interfaces for the Next Generation of AI Compute

AI 워크로드를 위한 인터페이스 최적 방안

- 고속 및 저지연 인터페이스 설계
  - 최대 448G 데이터 속도 구현 가능
- 구리 기반 연결에서 광(Optic) 링크로의 전환
  - 광 모듈로 교체시 전력 소모 증가
- 차세대 인터페이스 설계 방향
  - 저전력 소비 (pJ/b 단위에서의 최적화)
  - 짧은 도달거리에서 신호 무결성 유지
  - 모듈화된 설계를 통해 교체가 용이한 구조 개발



Local accelerator link



Pluggable

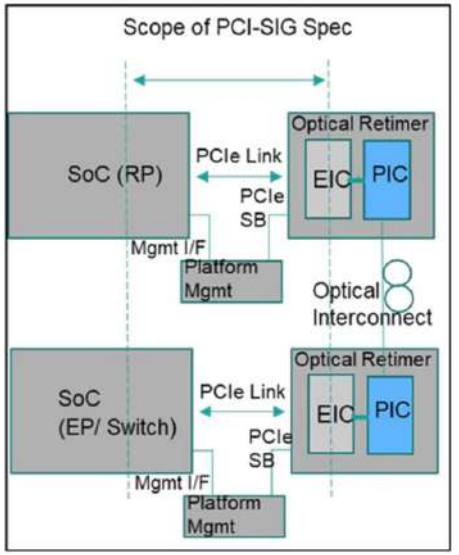
Replaceable modules:
- Non-retimed (LPO, LINEAR)
- Tx-retimed (RTLR, LRO)
- Fully-retimed

On-Board Optics

- Increased density
- Shorter electrical channel
- Replacement requires card removal

Co-packaged

- Highest density
- Shortest electrical channel
- Replacement requires repair of ASIC's package
- Configured during ASIC packaging



3-54 : The Expanded Role of SI/PI in GenAI Data Center Development (1/2)

GenAI의 영향

- GenAI로 인한 변화
  - 대규모 AI 모델 학습을 위한 GPU/ASIC 요구
  - 시스템 소비 전류 급증 -> 2000A 이상 PDN 설계 필요
  - 초고속 인터페이스 및 SoC 간 통신량 증가
- SI 문제
  - 채널 길이 증가 및 데이터 속도 향상 -> 지터/리플 문제 심화
  - SerDes 수 증가 -> 레이아웃 복잡도 증가
- PI 문제
  - 수십~수백 W의 AI 칩 전력 요구
  - IR Drop, dI/dt 손실, 노이즈 커플링 문제 심화

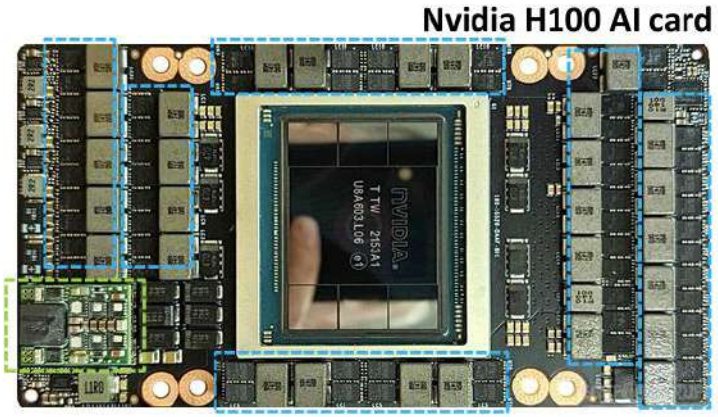
Trend	Cause	Design challenges	Mitigation
SoC IO explosion	High scale-up communication BW	**SI:** longer end-end channel, higher data rate **Layout:** more Serdes to escape & route	Flyover cable, retime, CPO
SoC Power explosion	High power compute chiplet	**dI/dt**: larger transient, bot cap ESL for thicker PCB **Power loss**: IR drop, plane cheesing **Cooling**: high thermal load	VPD, TLVR, embedded caps, liquid cooling
Large multi-chiplet SoC	High SoC perf. Chiplet modularization Reticle size	**SMT & reliability:** PCB & SoC warpage **Power loss:** center chiplet barricaded by neighbors' PTH vias, VR to load distance **Layout**: component fit, routing, SI/PI isolation **Cooling:** SoC-top coplanarity	Lidded package, VPD, embedded caps, liquid cooling
Rack accelerator density explosion	Large scale-up domain	**Smaller/thinner HW:** layout, cooling, structure **Power loss**: smaller power comp **Coexistence**: noise coupling, sim & test	Clamshell SMT, VPD, novel DC:DC, noise isolated stackup/floor plan
Large training cluster	LLM size & training complexity	**Simultaneous switching**: data center power **Silent data corruption**: HW fault detection **Fault tolerant system**: more complex system	Cap trays, power throttle algo., error tolerant AI models, failover/fail-operational HW & SW

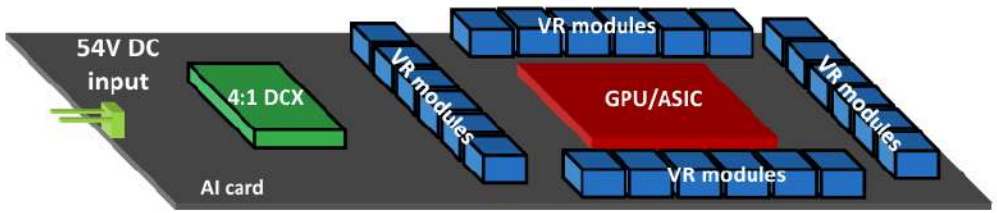
3-54 : The Expanded Role of SI/PI in GenAI Data Center Development (2/2)

전원 아키텍처의 변화

- 전원 아키텍처의 트렌드
  - Two Stage 아키텍처 (54V->DCX->VRM)
  - One Stage 아키텍처

Lateral Two-Stage Architecture: DCX 4:1 → VR





Stage 1: Fixed-Ratio DC transformer (DCX)

- ❑ Fixed ratio voltage conversion, X:1 transfer DC voltage like a transformer (DCX)
- ❑ 4:1 DCX input 40-60V, output 10-15V, typical size: 23mm x 17mm x 8mm (OCP standardized)
- ❑ 5:1, 6:1, 8:1, 10:1, 48:1 are also available
- ❑ Variants of LLC topologies, non-isolated, ZVS soft-switching for high efficiency.

Stage 2: Voltage Regulator (VR)

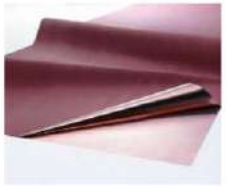
- ❑ High dynamic response requirement: >10A/ns
- ❑ Multi-phase BUCK topology, using coupled or non-coupled inductors
- ❑ DrMOS and multi-phase BUCK controller from the same vendor
- ❑ Trans-Inductor VR (TLVR) BUCK is trending due to better dynamic (but also issues)

3-54 : Use of Thin Film Resistors in Organic Substrates for Modules & Chip Packaging" (1)

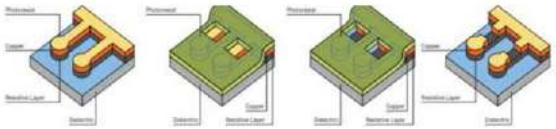
- 기존 IC Packaging 및 Module packaging 방식은 개별 저항 소자와 복잡한 via 구조로 SI 문제와 시스템 성능에 제한
→ mSAP 공정을 활용해 Organic substrate 의 여러 층에 thin film resistor를 직접 내장하는 방법 소개

Manufacturing Process- mSAP Overview

- Seed Layer Preparation Methods:
  - Direct Metallization
  - Etching Down of 9-18 micron Foil
  - Sacrificial Carrier Foil Method (preferred)
- Process Steps:
  - Seed layer creation
  - Photoresist application and patterning
  - Trace plating (12-15 microns)
  - Photoresist stripping
  - Quick etch for seed layer and resistor material removal.
  - 2nd Imaging/etching steps to define resistors
    - *Note: Needed when using embedded resistors*



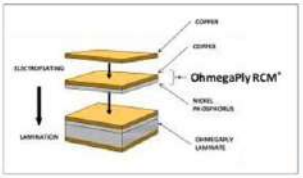
Carrier Foil
- 18 um carrier
- 3 um seed layer

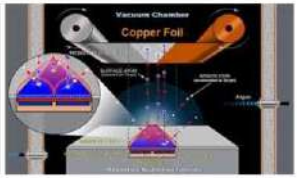


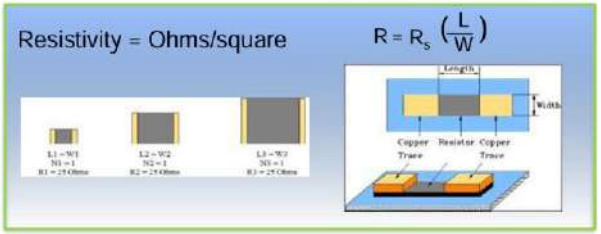
2nd Imaging/Etching steps

Resistor/Conductor Foil Formation

- Resistive Layer Deposition:
  - Electroplating Deposition
  - Sputtering Deposition
- Material Selection:
  - NiCr selected for optimal properties
  - Low temperature coefficient of resistance
- Carrier Foil Method Benefits:
  - Stable, flat surface
  - Precise control
  - Easy handling
  - Sub-micron thickness capability







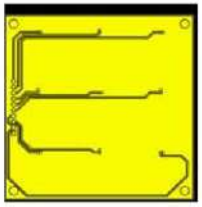
Thin film Resistor를 기판 내 embedding 시 장점
- SMD 타입의 저항 소자 사용을 줄여 소형화 가능
- 기판 표면의 공간 보존
- 기존 생산 방법 (mSAP) 활용 가능
- High-density packaging 가능
- Signal integrity 개선

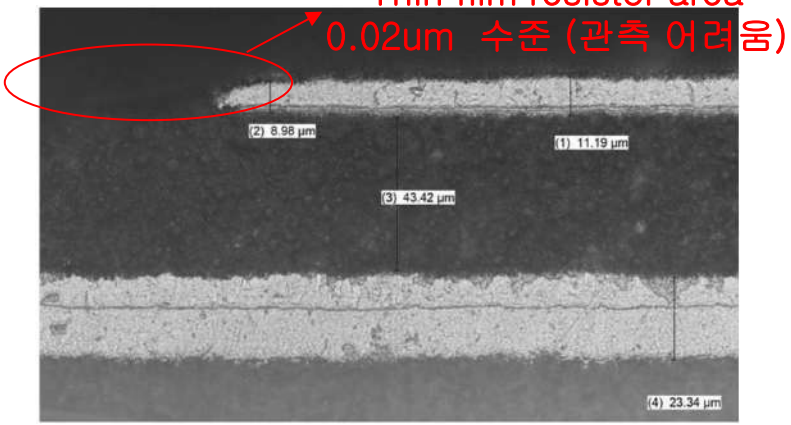
3. DesignCon 2025 자료 소개

3-54 : Use of Thin Film Resistors in Organic Substrates for Modules & Chip Packaging" (2)

[Test Vehicle Design]

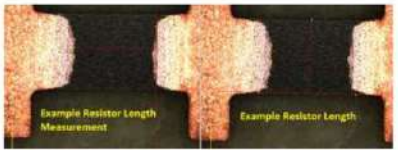
- 6-layer (2+2+2) substrate design
- Materials Used:
  - Core: Panasonic R-1515V (low CTE)
  - Build-up prepreg: AGC fastRise™ HF
  - Copper layers: 18μm, 9μm, and 3μm (after carrier removal) thicknesses
  - Resistor material on layer 2 (100 OPS NiCr)





[Experimental Result]

- Target: 100 ohms resistors
- Key Findings:
  - Successful embedding of resistors
  - Good material adhesion
  - Orientation affects resistance values and tolerance
  - Perpendicular resistors (to etcher direction): better tolerance
  - Overall tolerance: +/- 20-25% (Target- 15%)



Note: For the size resistors used in this study made using the standard subtractive process, the tolerance can be > +/- 30%

시험 결과
- 6층 기판에서 thin film resistor 삽입
- 20~25% 오차범위를 나타냄 (target 15%)
- Orientation에 따라 값 변화 발생

개선이 필요한 사항
- 포괄적인 material characterization
- thermal cycling과 같은 장기 신뢰성 시험
- 40GHz 이상의 고주파에 대한 시험 등